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The Influence of LOCOS-Related oxide etch on thin oxide leakage in memory devices

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The Influence of LOCOS-Related Oxide Etch Backs on Thin Oxide Leakage in Memory Devices

By.

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THE INFLUENCE OF LOCOS-RELATED OXIDE ETCH BACKS ON THIN OXIDE LEAKAGE IN MEMORY DEVICE

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ABSTRACT

The influence of oxide etch backs done in LOCOS based isolation technologies on the low level leakage and reliability of tunnel oxide capacitors has been studied. Tunnel oxide structures are part of nonvolatile memory devices such as Flash EEPROMs and are critical to their overall performance. Locos isolated, area and edge intensive capacitors with 94 Å tunnel oxide have been manufactured and tested. Test results indicate that the extent of the etch back and the use of HF instead of buffered HF as chemical etchants do not adversely affect the low level leakge of the tunnel capacitors. However, oxide endurance analysis based on constant current charge to breakdown tests show a significant degradaton if an aggressive etch back is adopted.

....To my mother, Norma M. Henry, my best friend DaQuetta Lynne Knox, and to the closest man in my life... Jesus Christ my LORD.

I can do all thing through Christ that strengthens me. (Phil 4:13)

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LIST OF SYMBOLS

BOE	**Buffered Oxide Etch**
CHE	**Channel Hot Electrons**
DI	**De-ionized water**
EEPROM	**Electrically Erasable and Programmable Read Only Memory**
F-N	**Fowler-Nordheim Tunneling**
HF	**HydroFlouric Acid**
H_i	**Interstial Hydrogen**
LOCOS	**Local Oxidation of Silicon**
LPCVD	**Low Pressure Chemical Vapor Deposition**
MOSFET	**Metal Oxide Semiconductor Field Effect Transistor**
MOS-C	**Metal oxide Semiconductor Capacitor**
R	**Radius**
RIE	**Reactive Ion Etch**
Si	**Silicon**
Si_o	**Oxide trivalent silicon**
Si_{os}	**Oxide trivalent Silicon close to the surface**
Si_s	**Silicon surface trivalent silicon**
SiO_2	**Silicon Dioxide**
Tun_{ox}	**Tunnel oxide**
TOX	**Oxide thickness**

1.0 INTRODUCTION

Memory devices are a vital part of today's computer technology. Each of these devices stores data in the form of charges, which can be referenced, retrieved, or altered in some way. Many types of memory devices exist today. The most commonly used memory devices are, SRAM's, DRAM's, and Flash EEPROM's. With the high demands placed on these devices, the reliability of these devices has to be extremely good. This will assure that whatever these devices are integrated in, that unit will function as designed.

Memory devices which utilizes a thin oxide layer less than or equal to 100 Å tend to have the most reliability problems associated with it. This is due to the fact that this thin oxide layer is such an integral part of these devices, and can be easily degraded by what is done before, during, and after the formation of this layer. Devices which tend to use these thin oxide layers are DRAM's and Flash EEPROM's.

To adequately report all the issues related to these devices would require more time than is available, therefore I will limit the scope of this report, only issues relating to the Flash EEPROM's.

1.1 Flash EEPROM's

Flash EEPROM's were introduced first by Masuoka in 1984[1]. Since then, the device has been improved from a three polysilicon layered structure, to a two poly layered structure. In the three layer polysilicon structure, the first layer was used as the erase gate, the second polysilicon layer as the floating gate, and the third layer as the control gate. Fig. 1.1-1 shows a schematic of this first EEPROM.

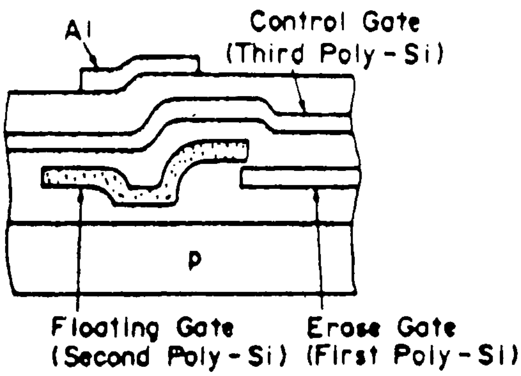


Fig. 1-1.1. A three polysilicon layered EEPROM design[1]

In the improved EEPROM structure (two poly layers), the erase poly layer has been removed. Fig. 1.1-2 is a schematic of the two poly EEPROM structure.

Although only one poly layer has been removed in eleven years, the removal of this layer does reduce the complexity of the fabrication process.

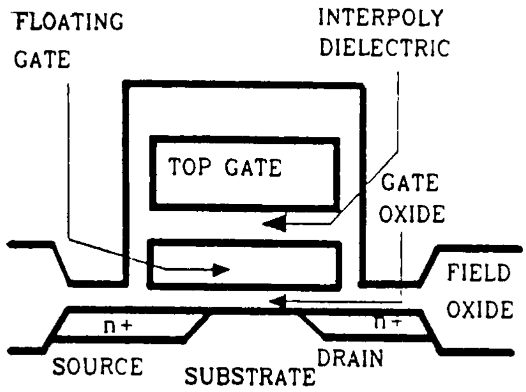


Fig. 1-1.2. A double polysilicon layered EEPROM design[2]

EEPROM's have been traditionally designed as a 1 transistor model cell, as is Fig. 1.1-2. It is referred to as a 1 transistor model because schematically, one MOS transistor can be realized. Improvements in the design of Flash EEPROM's have led to the design of the 1½ transistor cell model as shown in Fig. 1.1-3.

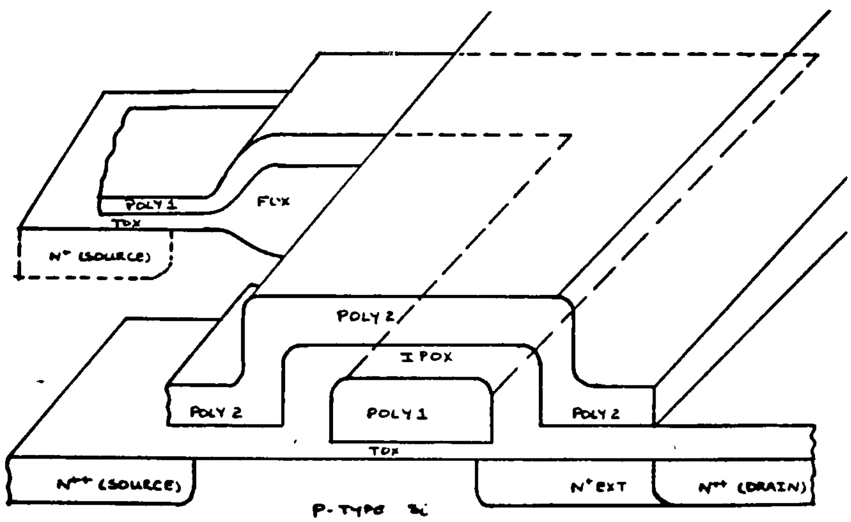


Fig. 1-1.3. 1½ Transistor cell model Flash EEPROM

The main advantage of the 1½ transistor cell model over the 1 transistor cell model is that the ½ cell is used to set the threshold voltage of the entire device. In the 1 transistor cell model, the threshold voltage is not fixed and can vary.

It should be noted, that the term "Flash," associated with this type of EEPROM, is a term which points to the speed at which this device can be erased. An entire row or column of a Flash EEPROM array can be erased at once, or the entire chip in less than a second.

1.2 Cell Programming and Erase Mechanism

Fig 1.2-1a depicts the conditions which must be applied to a cell to facilitate programming. A voltage is applied to the drain of the cell and voltage, larger than the drain voltage, is applied to the control gate. The source of this device is connected to ground during this operation. The result is a channel being formed. At the drain end of this channel, electrons are injected into the Floating gate through the oxide by Channel Hot Electrons.

Erasure of the Flash EEPROM cell is performed by subjecting the cell to a different set of voltage conditions (see Fig. 1.2-1b). The voltage on the source (VPP), is a positive voltage whose magnitude would depend on the thickness of the tunnel oxide. This causes the stored charges on the Floating gate to be removed by a process call Fowler-Nordheim Tunneling.

N.B. : A more detailed explanation of Channel Hot Electrons, and the Fowler-Nordheim process is given in section 2.1 and 2.2, of this work.

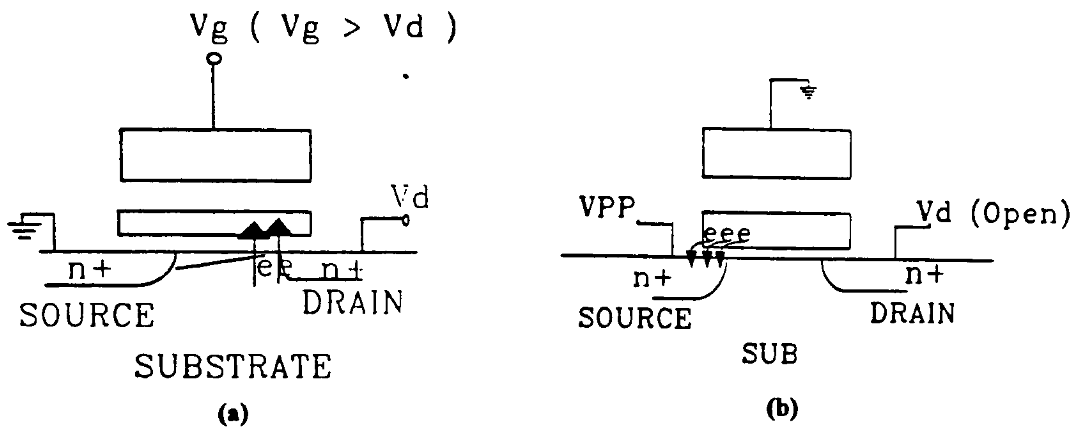


Fig. 1-2.1. (a) Schematic description of Flash memory programming[2]

(b) Schematic description of Flash memory electrical erase

1.3 Inherent Capacitances

In order to determine the threshold shift for a programmed and an unprogrammed cell, an understanding of the inherent capacitances within the cell, as well as their relationship to each other, will be required. Figure 1.3-1 shows the location of the inherent capacitance's for this device.

The capacitances Cg, Cdr, Ctun, and Csce, are the capacitances related to the control gate, drain, bulk, and the source of the EEPROM device.

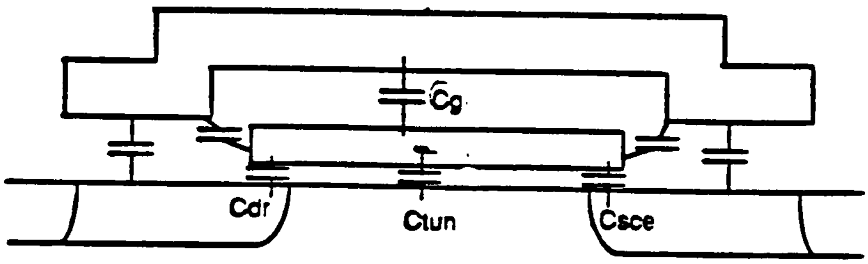


Fig. 1.3-1. A MOS device with the inherent capacitances shown

The total capacitance (C_{TOT}) is:

$$C_{TOT} = C_{CG} + C_S + C_B + C_D \qquad (1.3\text{-}1)$$

where C_{CG} is the capacitance related to the control gate, C_S, the source, C_B, the bulk, and C_D the drain respectively.

The coupling ration of the device can be define as below:

$$\alpha_i = C_i / C_{TOT} \qquad (1.3\text{-}2)$$

where represents the capacitance of any of the regions.

Equation 1 is transformed into:

$$\alpha_{CG} + \alpha_S + \alpha_B + \alpha_D = 1 \qquad (1.3\text{-}3)$$

The values for all α's are determined by, and are directly related to process design. The voltage on the Floating gate is determined by:

$$V_{FG} = \alpha_{CG} V_{CG} + \alpha_S V_S + \alpha_B V_B + \alpha_D V_D + Q/C_{TOT} \qquad (1.3\text{-}4)$$

Q/C_{TOT} is the voltage of the floating gate during the equilibrium conditions, and it is also a negative quantity because Q is negative. V_{FG} is also equal to $-V_t$, where V_t is the threshold voltage of the device. The charge on the Floating gate is given by:

$$Q = Q_i + \int I_g dt \qquad (1.3\text{-}5)$$

where Q_i is the initial charge on the floating gate, and I_g is the current in the gate when being programmed.

$$\Delta Q = \int I_g dt \qquad (1.3\text{-}6)$$

$$\int I_g dt = \Delta V_{FG} \times C_{TOT} \qquad (1.3\text{-}7)$$

During the programming sequence, the change in the floating gate is related to a change in the control gate.

$$\Delta V_{FG} = \Delta V_{CG} \times \alpha_{CG} \qquad (1.3\text{-}8)$$

Substituting equation 8 into equation 7, will result in:

$$\int I_g dt = \Delta V_{CG}(C_{CG}/C_{TOT})C_T \qquad (1.3\text{-}9)$$

$$\int I_g dt = \Delta V_{cg} C_{cg} \qquad (1.3\text{-}10)$$

Substituting equation 10 into equation 6 :

$$\Delta Q = -\Delta V_t C_{cg} \qquad (1.3\text{-}11)$$

1.4 Device Reliability

As more and more EEPROM's find their way integrated in other devices, the reliability of these devices will become of paramount importance. Some of the reliability issue associated with EEPROM's are Disturb Mechanism, Overerasing, Write/Erase cycling endurance, and Data Retention[1]. These issues are discussed below in some detail.

1.4-1 Disturb Mechanisms

The two main cell disturb mechanisms that can occur during the programming of a memory array, are called Gate disturb (DC program), and Drain disturb (program disturb).[1] These disturb mechanisms occur in cells which share the same word or bit line.

Gate disturb occurs in an unprogrammed cell or a group of cells, which have been erased. If these cells are connected to the same word line as a cell which is being programmed, the unprogrammed or erased cells can have an increase in their threshold voltage. In severe cases, the unprogrammed cells can even become programmed. This is due to the fact that a high voltage is placed on the common word line. The resulting electric field which would be across the thin oxide of both the programmed and the unprogrammed cells, may cause electrons to be injected into the floating gate from the substrate.

Drain-disturb occurs in programmed cells, which may have a common word line as a cell or a group of cells being programmed. The high voltage on the drain of the cell being programmed, which is also on the programmed cells, will cause an electric field to be established between the floating gate and the drain.[1] This may cause the charge on the floating gate to tunnel off, resulting in a cell with a lowered threshold voltage than what it should have.

1.4-2 Over-Erasing

The erasing of a cell or a group of cells is not self-limiting. This electrical erase can result in the floating gate being positively charged. The result is that this device now operates like a depletion-mode device. This is called over-erase.[1] The leakage current caused by this depletion-mode device on the bit-line can result in problems during the reading of the cell.

1.4-3 Write/Erase Endurance

This issue has to do with the quality of the tunnel oxide in the device. Both the write and erase cycles involves placing a high electric field across the tunnel oxide (tun_{ox}). This will cause electrons to tunnel either from the substrate to the floating gate, or the reverse. During these cycles, the oxide is being stressed by the applied voltage, and must withstand this condition without breaking down. A more detailed explanation of oxide breakdown and endurance is given in Chapter 2 of this work.

1.4-4 Data Retention

Charges which are stored on the Floating gate, can leak away through the gate oxide or through the interpoly dielectric.[1] The charge leakage, which may be caused by oxide defects, mobile ions, or other mechanisms, may result in a shift in the threshold voltage of the device. Data Retention and the Disturb mechanisms, directly dictate the purity of the data being retrieved or stored.

1.5 Process Reliability

The fabrication process of a EEPROM device involves many steps. Within these steps, films are deposited, etched, thermally grown, and oxidized. To discuss the many issues associated with each step, and their direct implication on the performance of the device is beyond the scope of this work. However, as this work focuses on the degradation of the thin gate oxide within these devices, those processing steps which tend to directly degrade the quality of the tun_{ox} ,will be discussed. The direction which will be followed is from the substrate to the floating gate, with any relevant points in between discussed.

1.5-1 Surface Microroughness

In manufacturing devices with ultra-thin oxides (< 100 Å), surface microstructure and surface cleanliness have increased in importance for device performance and reliability.[3] The standard RCA cleaning method, although effective in removing particulates, organics, and metallic materials, contains an alkaline solution of NH_4OH. Alkaline solutions tend to cause an increase in surface roughness.

Deterioration of the continuity of the surface is directly related to the strength of the alkaline solution. Highly roughened surfaces tend to produce oxides with lower reliability. Constant stress tests on these oxides would produce enhanced fields at the peaks which would cause the oxide to breakdown more quickly than anticipated.

Ohmi, et. al [3] have shown, that the surface roughness is reduced when a lower concentrated alkaline solution is used. Fig. 1.5-1 depicts a silicon surface after being dipped in different concentration of alkaline solutions. The procedure which was suggested by [3], is a ratio of .05:1:5, for the NH_4OH:H_2O_2:H_2O, followed by a DI rinse at room temperature.

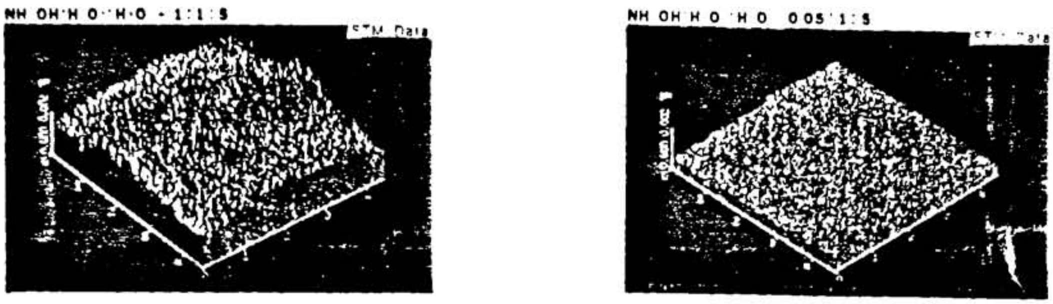


Fig. 1-5.1. SEM photograph of a silicon surface after exposure to different ratio alkaline solutions[3].

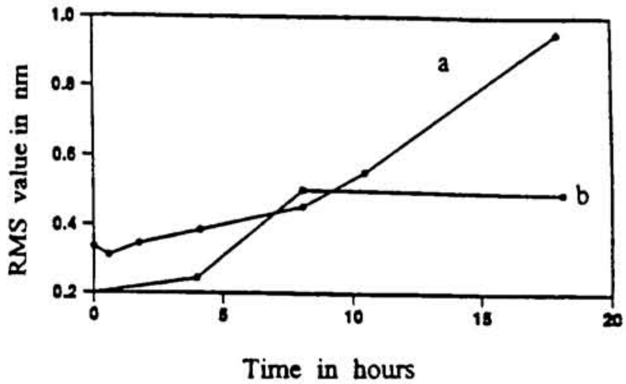


Fig. 1-5.2. Silicon surface roughness variation with rinse times after 50:1 HF (curve a) or after 50:1 BOE (curve b) dip[4].

Chemicals such as BOE and HF, used in the etching of the field oxide before the growth of the ultra-thin gate oxides, have also been linked to cause surface roughness.[4] HF has been reported as an agent which increases the surface roughness. Fig. 1.5-2 shows the roughness variations produced for both BOE and HF at the same concentration.

1.5-2 Thin Oxide Growth Process

The method used to grow a high quality thin oxide does affect the electrical properties of that oxide. Thermally grown oxides contains compressive stress.[5] The magnitude of this stress is dependent upon the oxidation temperature and the growth condition.

Stress within the oxides is relieved by performing an anneal step during the oxide growth. This anneal step allows the oxidation to reaction to reach completion, which will results in denser oxides with lower oxide charges.[6] At present, performing this anneal step is thought best to be done before the final film thickness is reached, as well as after the film thickness is reached. The times and temperature that this anneal is performed is not standardized and does vary, depending on application.

1.5-3 LOCOS ISOLATION

The most dominant isolation technique used in today's semiconductor industry is LOCOS based isolation. LOCOS, which is an abbreviation for LOCal Oxidation of Silicon, involves the use a nitride layer in certain areas of the die. When placed in an oxidizing environment , the nitride prevents the growth of SiO_2 in the areas where it is present. In areas in which the nitride is not present, the field oxide will grow.

Standard processes, especially in complex chips with embedded memory array, may employ several etch backs to remove the sacrificial oxide (Kooi oxide) from the different devices being fabricated on that one die. This etch back occurs before the thin gate oxide is grown. In the transition from the relatively thin oxide to the thick field oxide (the bird's beak), local compressive stress may cause the oxide to grow thinner in the concave peripheral regions than elsewhere.[7] If an aggressive etch back is employed, the oxide thinning problem could be enhanced and the data retention ability of the device compromised.

At the LOCOS isolation edges, positive charges can increase. This increase in positive charges is due to the difference in sign of normal stress between the bird's beak (compressive), and the filed oxide (tensile).[8] These positive charges tend to decrease the reliability of the thin oxide, especially when a gate bias is present. The role of positive charges in thin oxide reliability is explained in detail in Chapter 2.

1.5-4 Issues relating to the Polysilicon Gate Electrode

The floating gate of an EEPROM device is a highly doped polysilicon film. The doping of this film can be done by many methods, all of which can cause indirect damage to the oxide. Within each method, the species used as the dopant, as well as the temperature at which the activation of these dopants are performed, can cause ridges to form on the oxide itself, and bumps to be formed on the polysilicon surface.[9] This may compromise the quality of the oxide gate in the same manner that surface roughness does.

Oxide ridges are formed when dopants, such as phosphorous, segregate at the grain boundaries forming a phosphorous rich oxide (see Fig. 1.5-3). Lowering the dose, and the anneal temperature, does reduce the pronouncement of these ridges.[9]

The "bumps" on the polysilicon film affects the retention of the data in the floating gate. These bumps can form areas of enhanced electric fields, in which electrons from the floating gate can be injected into control gate through the interpoly dielectric. To prevent this, the interpoly dielectric is a combination of oxide/nitride/oxide (ONO).[10] The nitride within this structure provides a higher dielectric constant, and does not allow electron injection easily.

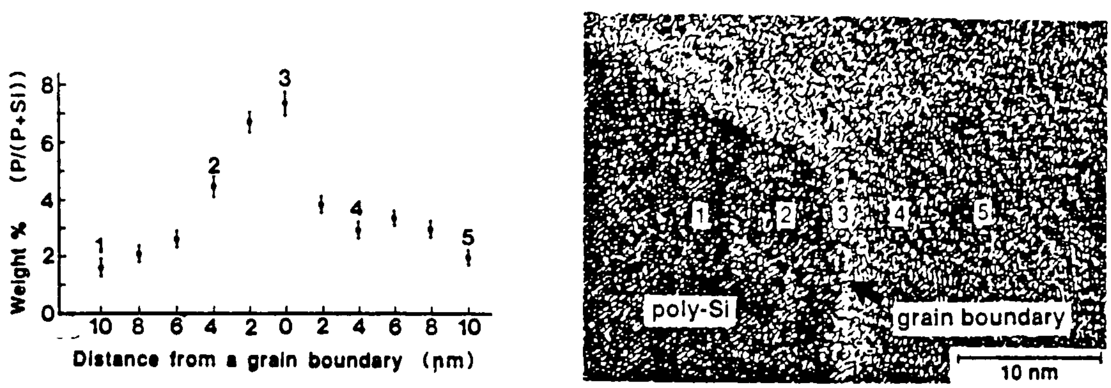


Fig. 1-5.3. Phosphorous segregation at the poly-Si grain boundaries[9]

Summary

The use of Flash EEPROM's have increased since its inception in 1984. Since then it has become less complex in its design and fabrication. However, this device is not problem free.

In this chapter, the problems relating to the function of a Flash EEPROM was discussed. Also, it was outlined that the ultra-thin oxide has been determined to be the part of the device which would most likely fail. Processing steps which directly and indirectly affect the quality of the thin oxide was discussed.

Chapter 2 will contain the theory associated with conduction through an oxide, as well as oxide breakdown. Both topics will be discussed in detail, and will include any and all relevant subjects which enhances or retard the topics being discussed.

2.0 THEORY

2.1 Introduction

The operation of an EEPROM involves the injection of electrons from one area to another, and from one film to another, through the same medium, or through different mediums. The mechanism in which charge is injected from one site to another, is primarily performed by CHE and F-N. In this section, these mechanism will be investigated in some detail. During charge injection through the thin gate oxides, the oxides can fail after a time thus rendering the device useless. The failure or breakdown process, and the models associated with it are also presented in this section.

2.2 Channel Hot Electrons (CHE)

CHE occur in MOSFETs which are strongly biased in inversion. Carriers move from the source end of a MOSFET to the drain end, by means of the lateral field component produced from the drain (see Fig 2.2-1).

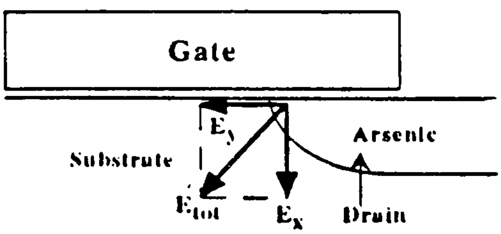


Fig. 2.2-1. Components of the electric field present at the drain of a MOS device

The carriers will remain in the channel due to the large energy barrier between the oxide and the channel. The energy barrier value for an electron is 3.2 eV, while for holes it is 4.5, as shown in Fig 2.2-2. These values are of significance in that it indicates the electron injection is more feasible to than hole injection. This does make a NMOS device more prone to hot carrier injection than a PMOS device.

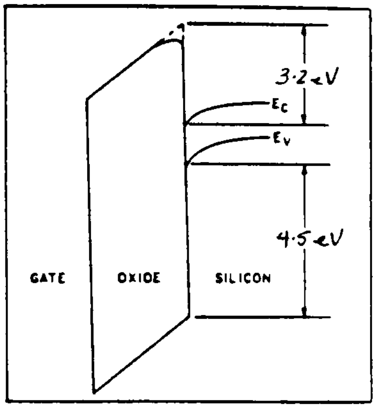


Fig. 2.2-2. Energy band diagram of a MOS device in the direction perpendicular to the surface[11]

With the lateral field, there is also a vertical field, designated as E_x in Fig.2.2-1, in the channel of the MOSFET. This field however, acts only to constrain the carriers to the channel. If these carriers acquire sufficient energy from the lateral field they can surmount the energy barrier and enter the conduction band of the oxide.[11] When this occur, the carriers are said to be "hot" carriers. Once in the conduction band of the oxide, the carriers can move into the gate electrode, in which they represent a gate current. Fig. 2.2-3 depicts the energy band diagram of a MOS device under hot electron injection condition.

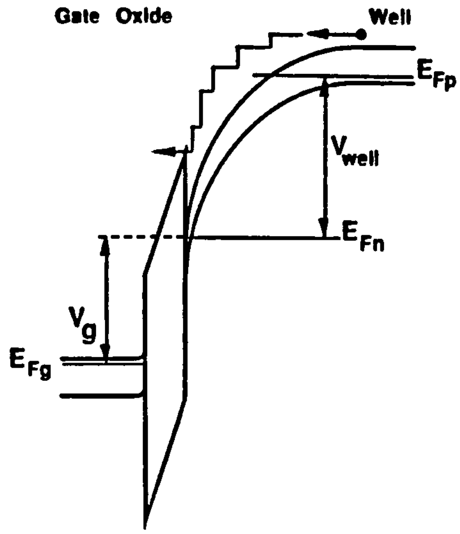


Fig. 2.2-3. Energy band diagram of a MOS device under hot electron injection condition

2.3 Fowler-Nordheim Tunneling

The injection of carriers into or through an oxide, is performed by tunneling. Tunneling is defined as a "cold" process, in that carriers go through the energy barrier instead of over it. F-N tunneling involves the injection of carriers (usually electrons), into the conduction band of an oxide through the triangular-like energy barrier.[11] Once in the conduction band, these electrons are accelerated by the oxide field toward the gate, resulting in a gate current. Equation 1 is the tunneling current expression:

$$J = AE_{ox}^2 \exp(-B/E_{ox}) \qquad (2.3\text{-}1)$$

where A and B are constants which can be calculated as below.

$$A = \frac{q}{8\pi h}\frac{m_o}{m^*}\phi_b^{-1} \qquad (2.3\text{-}2)$$

$$B = \frac{4}{3hq}\sqrt{2m^*}\,\phi_b^{\frac{3}{2}} \qquad (2.3\text{-}3)$$

$\frac{m_o}{m^*} = .42$ and ϕ_b is the Si/SiO_2 energy barrier.

At this point it must be noted that the field across the oxide is not simply the voltage applied to the gate divided by the oxide thickness. If this procedure is used to calculate the value of E_{ox}, and this value is used in equation 1, the result would be incorrect. This is because the procedure does not account for the voltage drops across the poly gate, the silicon substrate, as well as the Flatband voltage. Keeping all of this in mind, the true voltage across the oxide can be determined by equations 2.3-4a and 2.3-4b. The corrected voltage which would be applied to the oxide is V_{ox2}.

$$V_{ox1} = V_g - R_s I_g \qquad (2.3\text{-}4a)$$

$$V_{ox2} = V_{ox1} - V_{FB} - V_{poly} - V_{Si} \qquad (2.3\text{-}4b)$$

The location of these voltages on an Energy band diagram is shown in Fig. 2.3-1.

From the energy band diagram, it can be seen that the n^+ poly gate would be in strong inversion, and the n-type substrate in strong accumulation, during a positive voltage applied to the gate. In the strongly inverted poly gate, V_{poly} would be the equivalent surface potential, applied if the substrate was taken to be the gate of this device. Likewise, in the strongly accumulated substrate, V_{Si} would be the equivalent surface potential, with normal conditions. Determination of these voltage are difficult especially for the polysil:con gate.

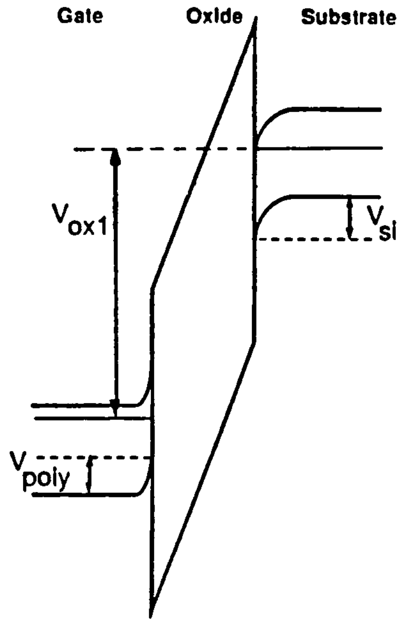


Fig. 2.3-1. Energy band diagram of a MOS device under a constant voltage stress

Approximations for the different regions of operations, have been put forth by models associated with their respective regions. In the strong inversion region, a common assumption is that Ψ_S is pinned to a constant value[9]:

$$\Psi_S=\phi_B \qquad (2.3\text{-}4c)$$

A rough estimation of the value of ϕ_B is that it is equal to $2\phi_F + 8\phi_t$, where ϕ_F is the Fermi voltage, and ϕ_t is the thermal voltage. This estimation is an average which takes into account various processing parameters.[12]

The value of ϕ_F for a substrate with a dopant gradient profile, also bring about another estimation. Since the value of ϕ_F is determined by using the substrate doping, only an average value of the doping concentration near the poly/oxide interface can be used. For the substrate in strong accumulation, the value of Ψ_S is approximately $8\phi_t$.

The value of the flatband voltage is determined by equation 2.3-4d:

$$V_{FB} = \Phi_{MS} - \frac{Q_o'}{C_{ox}'} \qquad (2.3\text{-}4d)$$

where Q_o' is the oxide charge per unit area, and C_{ox}' is the capacitance per unit area.

Since the value of C_{ox}' is very large in this work, Q_o'/C_{ox}' will be very small and is negligible.

This reduces equation 2.3-4d to:

$$V_{FB} = \Phi_{MS} \qquad (2.3\text{-}4e)$$

The value of Φ_{MS} is the contact potential between the high/lo (substrate/back implant) junction.

2.4 Direct Tunneling

As the thickness of the gate oxide reduces further, the Tunneling phenomenon will move from F-N, to Direct Tunneling. The energy band diagram for direct tunneling is trapezoidal (triangular for F-N), as shown in Fig. 2.4-1. The differences between F-N and Direct tunneling lie in the amount of applied voltage (V_{ox}), compared to the barrier height ϕ_b, that would cause conduction It is shown in Fig. 2.4-2 the theoretical transition point between F-N and Direct tunneling. The transition point is thought to be about 60 Å.

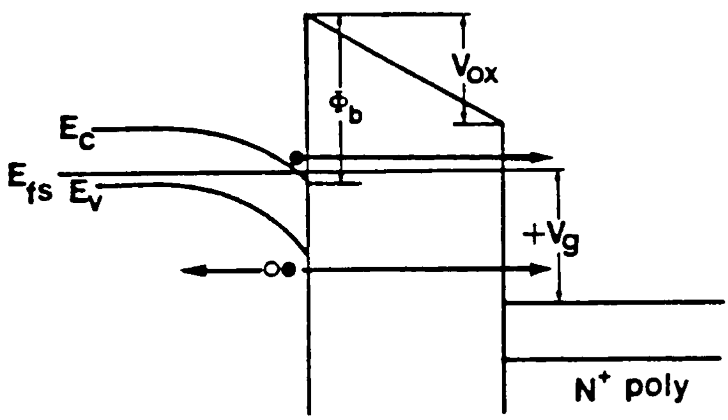


Fig. 2.4-1. Energy band diagram showing Direct tunneling (trapezoidal barrier, $V_{OX} < \phi_B$)[13]

The current associate with this type of tunneling, shows a weaker dependence on the oxide field.[14] This has been attributed to the electrons tunneling through the Forbidden gap of the oxide, to the gate.

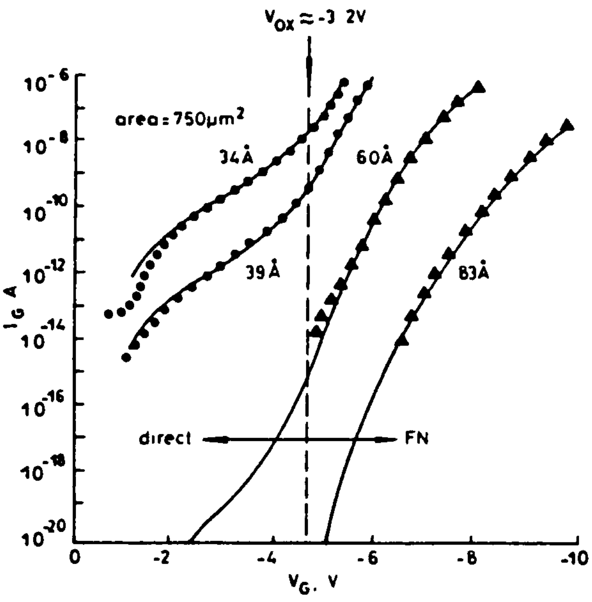


Fig. 2.4-2. Theoretical and experimental I-V curves for F-N and Direct Tunneling.[14]

2.5 Electric Field Enhancement in an Oxide

Charge is injected into and through an oxide after the establishment of an electric field. The established field (E_{ox}), across the oxide may not uniform. This may be due to oxides grown on Si-substrates which have been roughened, or ridges formed on the oxide due to poly dopant activation. The surface irregularities may cause, in some areas, field enhancements which will lead to most of the gate current to flow through those areas only.[15] Fig. 2.5-1 represents a schematical view of an oxide interface with asperities or bumps.

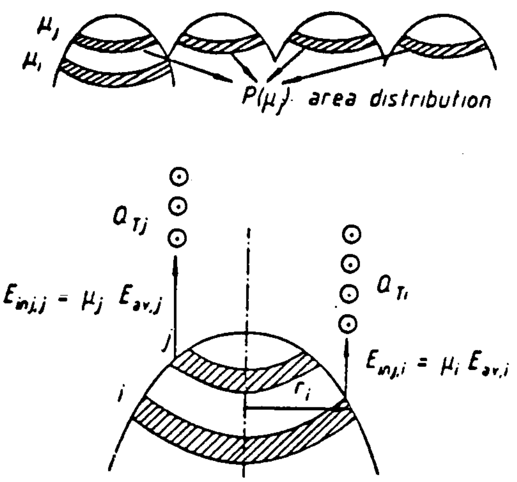


Fig. 2.5-1. Schematical representation of bumps on a silicon surface.[16]

Variations in the size and shape of these bumps can also contribute to a non-uniformity in the field. Randomly sharp protrusions and large bumps can cause high field enhancements which will result in a large conduction current at much smaller fields than for a smaller bump.

In taking a closer look at the bumps on which the oxide is grown, it can be seen that each bump will posses a particular field enhancement factor, μ. Also, if the view is limited to only one bump, it can been seen that the enhancement factor is a maximum at the top of the bump and decreases as you move done the bump. These field enhancements necessitates the modification of the F-N equation (Equations 2.3-1a through 2.3-3).

If one assumes a charge free oxide, the electric field lines should be continuous across the oxide. A uniformly thick oxide grown over a hemispherical bump with a radius of curvature R, would imply a $1/r^2$ decrease in the electric field strength as the coordinate r (Spherical coordinates), changes from r=R, at the bottom of the bump, to r=R+tox, at the top of the bump.[17] Integrating E(r) across the oxide gives:

$$V_{ox} = E_{ox}Rtox/(R + tox)) \qquad (2.5\text{-}1)$$

In terms of the electric field across the oxide, E_{ox} , equation 2.5-1 can be rewritten as:

$$E_{ox} = E_p(1 + (tox/R)) \qquad (2.5\text{-}2)$$

The term E_p represents the planar field, and equates to the expression

$$E_{ox}=V_{ox}/tox \qquad (2.5\text{-}2a)$$

It is important to note that the expression (1+(Tox/R)), represents the field enhancement factor μ, and is dependent on the upon the curvature of the bump.

Rewriting equation 2.5-1

$$E_{ox} = \mu V_{ox}/tox \qquad (2.5\text{-}3)$$

which can be then substituted into the F-N equation. If the oxide conduction model above were to included the presence of trapped charges then equation 2.5-1 would have to be modified.

Let us assume that electrons are injected from one interface to another, and that some of these electrons will be trapped in the oxide. This build up of negative charges will oppose the field at the cathode end, reducing the current level of the oxide. The resulting voltage reduction ΔV, is due to the trapping voltage V_q.[16]

$$V_q = \frac{Q_T X'}{\varepsilon_{ox}} \tag{2.5-4}$$

Where Q_T is the integrated trapped charge which is represented below:

$$Q_T = q\int_0^{tox} n_t(x)dx \tag{2.5-5}$$

and X' is the centroid of the trapped charge calculated below:

$$X' = \frac{q}{Q_T}\int_0^{tox} x n_t(x)dx \tag{2.5-6}$$

The effective voltage across the oxide is then

$$V' = \mu(V_{ox} - V_q) \qquad \text{Eqn 2.5-7}$$

which can be then factored into the F-N equation.

2.6 Electrical Conduction and Breakdown of oxides

2.6-1 Introduction

Conceptually, an oxide represents an impenetrable barrier for any injection of charge (electron) through it. This becomes especially true if the kinetic energy associated with these charges is below 3.2 eV. Conduction can however take place due to the wave like nature of an electron. This wave like nature allows for a finite probability that an electron can pass through, or cross the barrier even if the electron does not posses the necessary energy to pass over the barrier. The probability that an electron can pass through the barrier increases as the field across the barrier increases or the barrier becomes thinner. This begins the process of conduction through an oxide.

With the application of a gate bias, the established field across the oxide is not uniform. This non-uniformity of the electric field is caused by irregular interfaces at the poly-gate/SiO_2 and the SiO_2/Si regions. If one adds to the non-uniform field microdefects in the oxide caused by oxide decomposition, trapped charges at the interfaces and within the bulk oxide, then a recipe would be defined for a catastrophic breakdown of the oxide.[16, 18, 19]

Oxide break down appears to occur in two stages. First, the oxide is weakened by gate current passing through it. At some point in this stage a conductive path is established in the oxide. The energy stored by this capacitor is quickly dissipated through this conductive path. In some cases, the energy discharge is enough that the weakened areas, the gate material and the oxide, can be vaporized. Fig 2.6-1 illustrates the results of this energy dissipation.

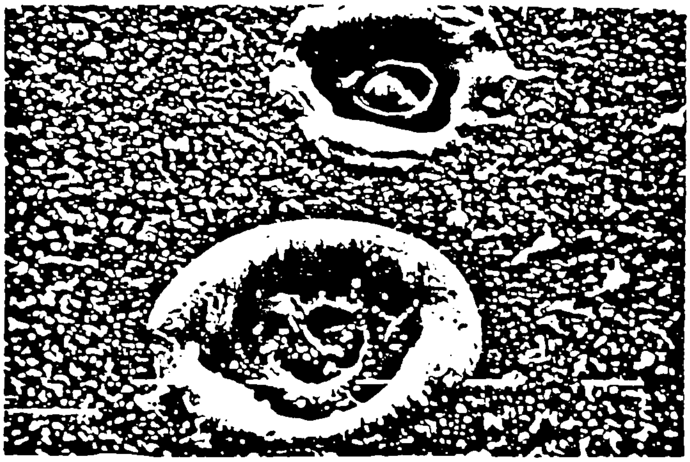


Fig. 2.6-1. SEM photograph of two breakdown spots[20]

2.6-2 Oxide Breakdown

The physical origin of oxide breakdown has yet to be completely understood. Many models have been proposed to explain this process but none has been proven to be dominant over another. Although no one model unanimously provides the answer for oxide breakdown, all follow a basic format. This format is that electrons are injected which could generate electron-hole pairs as they travel through the oxide. Charges are trapped which result in a change in the voltage across the oxide, and also localized changes in the electric field in the oxide. A positive feedback will be established which causes more electrons to be injected and more of these electrons to produce electron-hole pairs which get trapped. Eventually a critical current will be established which will cause the capacitor to break.

The role, if any, of these trapped charges in the process of breakdown has been debated.[18, 21] Some believe that it is the trapped electrons which facilitates the oxide to breakdown, while other believe that it is the presence of trapped holes. Both types of trapping are likely to occur at any given time.

Electron and Hole Traps

The location of the traps for holes and electrons are not in the same vicinity. Hole traps are located near the Si-SiO_2 interface, while electron traps a distributed throughout the oxide. The areas which are trap centers are either formed by the injection of electrons and the damage that can occur, or it is the present in the oxide due to defects.

Hole Traps

Hole traps near the Si/SiO_2 interface have been postulated to be trivalent silicon.[22] Three forms of this trivalent silicon are proposed: silicon surface trivalent silicon, Si_s, oxide trivalent silicon, Si_o, and oxide trivalent silicon located close to the surface, Si_{os}. The location of these trivalent silicons are depicted in Fig 2.6-2.

Silicon surface trivalent silicon are silicon atoms which are bonded to three other silicon atom. Oxide trivalent silicon are silicon atoms which are bonded to three other oxygen atoms.

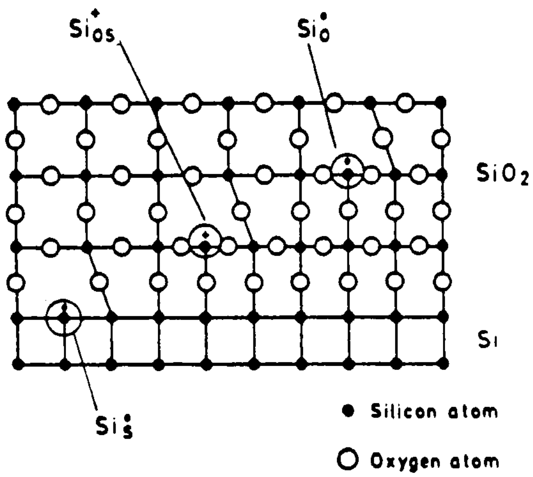


Fig 2.6-2. The Si-SiO_2 interface with the three forms of Si. defects[22]

Si_s is thought to be a surface trap, Si_o a deep hole trap, and Si_{os} a very deep hole trap far deeper than Si_o, because of its interaction with the silicon surface.[22] Each of these trivalent silicon have the ability to form compounds with Hydrogen.

$$\equiv Si + H_i \rightleftharpoons SiH \qquad (2.6\text{-}1)$$

Temperature and Hydrogen concentration will determine the direction which this reaction will undergo. The result of Equation. 2.6-1 for Si_s is an electrically inactive site. Si_sH is not considered to be a trap site. Si_oH and $Si_{os}H$, in their ionized form are unstable which enables these sites to be to trap holes. For the Si_{∞} sites however, once the hole is trapped, it remains trapped, which results in these sites becoming a fixed charge sites.

Another trap site are the weak Si-O bonds located in different areas of the oxide. When a hole is captured at these sites, oxygen vacancies are formed. This leads to the formation of dangling bonds, as well as the SiO_2 network being modified (see Fig. 2.6-3).

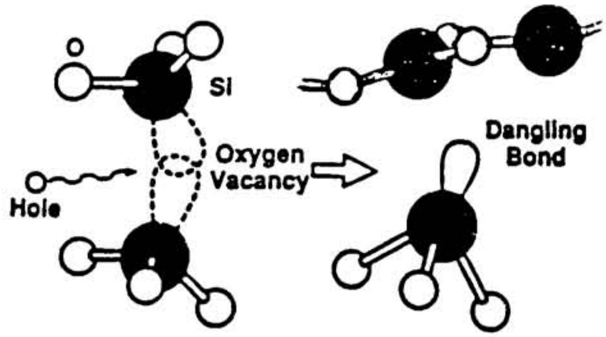


Fig. 2.6-3. A schematic picture of structural change in Si-O bonds caused by a trapped hole.[23]

<u>**Electron Traps**</u>

The two known electron trap sites which are present within an oxide are, water-related traps, and sodium related traps.[24] Water-related traps are formed when water vapor reacts with the Si-lattice. The result of this reaction is a Si-OH structure. The oxygen within this compound is what traps the electron due to its strong electron affinity. If an electron is captured, the result would be an interstitial hydrogen.

Sodium-related traps are caused because of contamination in the oxide. These traps initially are neutral, and possesses a large capture cross-section. The capture cross-section is thought to be a coulombic center.[24] It should be noted that sodium ions do not trap electrons. However, the presence of sodium seems to cause these traps to be formed. These traps are easily eliminated if the oxidation environment is contamination free.

Oxide Breakdown Mechanism

When a bias is applied to the gate of a MOS device, electrons are injected into the oxide. These electrons can be captured by the oxygen in the silanol group (Si-OH), releasing an interstitial Hydrogen. This Hydrogen can move through the SiO_2 lattice to the Si-SiO_2 interface where it can react with a SiH compound forming H_2(g). A dangling bond will also be formed from his reaction which is a hole trap site. If a hole is trapped, then this positive charge will add to the overall charge on the oxide.

As the electrons are being injected into the oxide, some of these electrons can acquire sufficient energy to cause impact ionization. From this impact ionization, electron-hole pairs can be generated which can be trapped by their respective site, or aid in the creation of more trap sites, which may increase the field across the oxide, or change the field within the oxide.

If more and more positive charges are formed, more electrons will be injected into the oxide. A positive feedback would be established which at some point would cause a critical amount of charge to be in the oxide. This critical charge when reached would discharge thus breakdown the oxide.

The oxide interface quality can be checked by making the interface either injecting or collecting the electrons. The interface that is injecting the electrons would be the interface being tested. On another device, if the reverse bias was applied, then the relative time to breakdown would be determined. The interface with the most trap sites, or that has more roughness would breakdown the quickest.

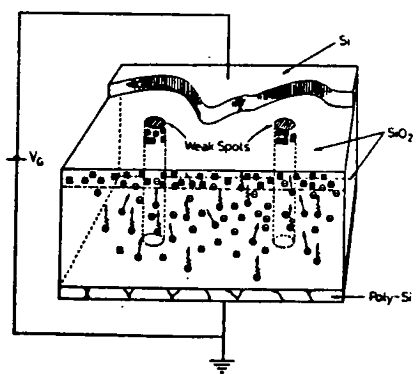


Fig. 2.6-4. A theoretical model showing electron trapping, positive charge generation, weak spots and robust areas.[21]

Oxide Breakdown Model

The oxide may be looked at as having two areas connected in parallel. These areas maybe termed as the weak and the robust areas. Fig. 2.6-4 illustrates these two areas. The weak areas are small and more prone to localized hole trapping. The robust areas on the other hand, are larger and are not prone to hole trapping. Fig. 2.6-5 and 6-6 illustrates the energy diagram of these areas with their respective trapped charge.

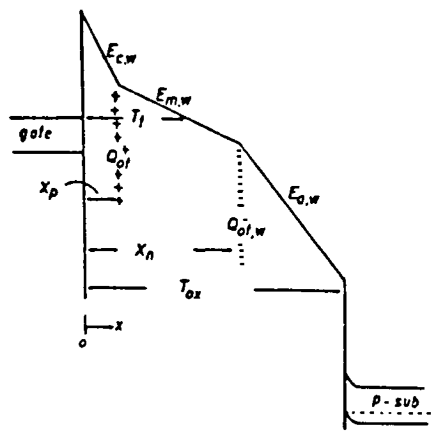


Fig. 2.6-5. SiO_2 energy diagram showing trapped holes Q^+_{ot} and trapped electrons Q^-_{ot} (weak area)[18]

The equations associate with the weak areas electric field are given below:

$$E_{c,W} = \frac{V_{ox}}{tox} - \left(1 - \frac{X_n}{tox}\right)\frac{Q^-_{o,t,W}}{\varepsilon_{ox}} + \left(1 - \frac{X_p}{tox}\right)\frac{Q^+_{ot}}{\varepsilon_{ox}} \quad (2.6\text{-}2)$$

$$E_{m,W} = E_{c,W} - \frac{Q^+_{ot}}{\varepsilon_{ox}} \quad (2.6\text{-}3)$$

$$E_{a,W} = E_{m,W} + \frac{Q^-_{ot,W}}{\varepsilon_{ox}} \quad (2.6\text{-}4)$$

Determining the correct electric field across the oxide will be useful as the F-N equation cannot be used directly without the corrected field value. For the robust areas, equations 2.6-2 through 2.6-4, are the same except that Q^{+}_{α} is set to zero.

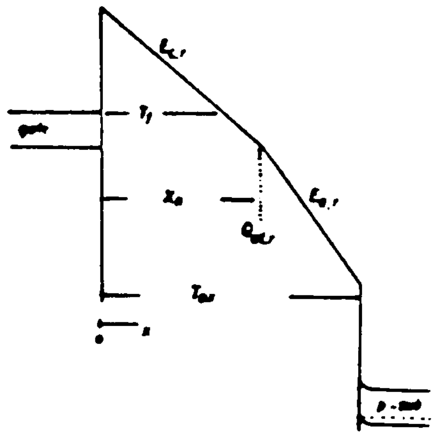


Fig. 2.6-6. Energy band diagram for the region without localized cathode hole trapping (robust area)[18]

2.7 Dielectric Strength of An Oxide

The dielectric strength of an oxide is the maximum electric field that can be applied to that oxide before it breaks. The electric field is determined by dividing the maximum voltage applied, by the thickness of the oxide. Voltages are applied in a linear manner, changing in a specified time (ramp voltage), until the oxide breaks.

There are three modes, or categories in which an oxide can be placed, based on the results of the test for dielectric strength. These modes are A-mode, B-mode, and C-mode. Fig 2.7-1 show a histogram plot of the different modes, and the corresponding voltages.

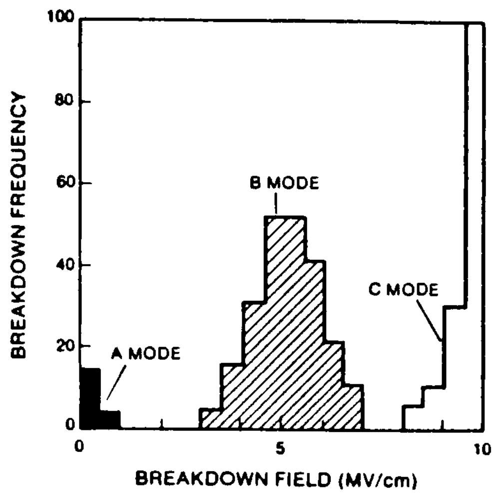


Fig. 2.7-1. Histogram plot of the different modes of dielectric breakdown[25]

A-mode oxides are those which fail almost instantly or, at very low fields. These have been related to poor conditions (low quality gases, contaminated furnace, or cleaning solutions etc.), in which the oxide was grown.

B-mode failures have been related to defects in the oxide. Some of these defects are sodium contamination, substrate metal contamination, surface roughness, localized regions where the oxide is thinner and crystalline defects in the substrate. Most of these issues have already been discussed. The ones which have not been discussed are described briefly below

Any oxide that falls into the category of C-mode, contains little or no contamination in the oxide.

Substrate Metal Contamination

Substrate metal contamination arise prior or during the growth of the oxide. Metals such as Al, Fe, and Ca, are some of the metals which can be present. Also, heavy precipitates (due to contaminated cleaning solutions, or poor handling conditions), can also be present in the substrate. All of the above metals tend to weaken the oxide lattice formation, or cause electric field irregularities at the interface.

Crystalline Defects

Crystalline defects in the substrate such as SiO_2 precipitates near the surface are mainly a problem in the CZ-grown wafers that contain oxygen which is dissolve in the lattice. If the surface of the wafer is not completely denuded of the oxygen, the formation a poor SiO_2 compound will be formed. As the thin gate oxide is grown, this poor oxide would become incorporated in the gate oxide leading to a lower dielectric strength.

Summary

This chapter outline the mechanisms involved in the conduction of charges (electrons), through an oxide. A breakdown model and was also discussed in detail. Electric field enhancements, when present, increases the conduction current through an oxide at the point where the enhancement occurs. However, the reliability of such an oxide is poor, especially when the oxide is stressed by a constant current or voltage. In order to compare an oxide with these field enhancements, modification to the F-N equation must be done. The modification was also outlined. The mechanisms outline in this chapter will assist in the understanding of what is occurring, as the tests which are performed in this work are done (see Chapter 4).

In chapter 3, the experiment performed is outlined, and details are given for the fabrication of the test structures.

3.0 Experiment and Simulation

3.1 Introduction

In the processing of complex dies with embedded memory arrays, several etch backs could be incorporated in the processing steps over the memory array. This aggressive etch back could degrade the quality of the thin oxide, and could also increase the leakage current of the device. This experiment focused on two distinct areas of the EEPROM: the Erase area of the 1½ transistor model (see Fig. 1.1-3), and the Program/Erase area of the 1 transistor model (see Fig. 1.1-2).

In the Erase area of the 1½ transistor model, the thin oxide (tunnel oxide), is grown over a heavy implanted region, while in the Program/Erase areas of the 1 transistor model , the tunnel oxide is grown over the substrate. Both of these areas involve the transition from a thin oxide to a thick field oxide, which, if multiple etch backs occur, could become sites of enhanced leakage. These areas will thus become the point of study.

Oxide etch backs can be performed by using BOE or HF, both of which are standard wet chemical oxide etchants. As described in Chapter 1, the chemical etchants can roughen the surface of the substrate on which the tunnel oxide would be grown. The effects of these etchants will also be investigated.

Varying the amount of oxide etched away (etch back), is the final consideration for this work. Etch backs of 1500, 2500, 3500, 4500, 5500 Å were utilized, all of which are possible in complex embedded die fabrication.

All of the above consideration was incorporated into a LOCOS type MOS-C, which became the test vehicle for this experiment.

3.1-2 Mask Design

Fig 3-1 shows the completed chip design. The dimensions of this chip were 1.2 cm x .89 cm. Contained in this design are gate-surrounded and field surrounded capacitors, large field surrounded array capacitors, Van der Pauws structures, as well as Field-Active area leakage structures.

Gate and Field Surrounded Capacitors

Gate surrounded and Field surrounded capacitors were designed. Gate surrounded capacitors are capacitors in which the gate material is exclusively in the active area. In the Field surrounded devices, the gate material extends over the field oxide, covering the entire active area.

Both the Gate surrounded and the field surrounded capacitors were designed with the same sizes. The sizes designed were 50 K, 75 K, 100 K, 125 K, 150 Kμm^2. These capacitors served two purposes: 1. To determine the oxide reliability, and (2.) To determine the low leakage value associated with the different groups of study, by using the ramp voltage test. Fig 3-2a and 3-2b show these two kinds of capacitors

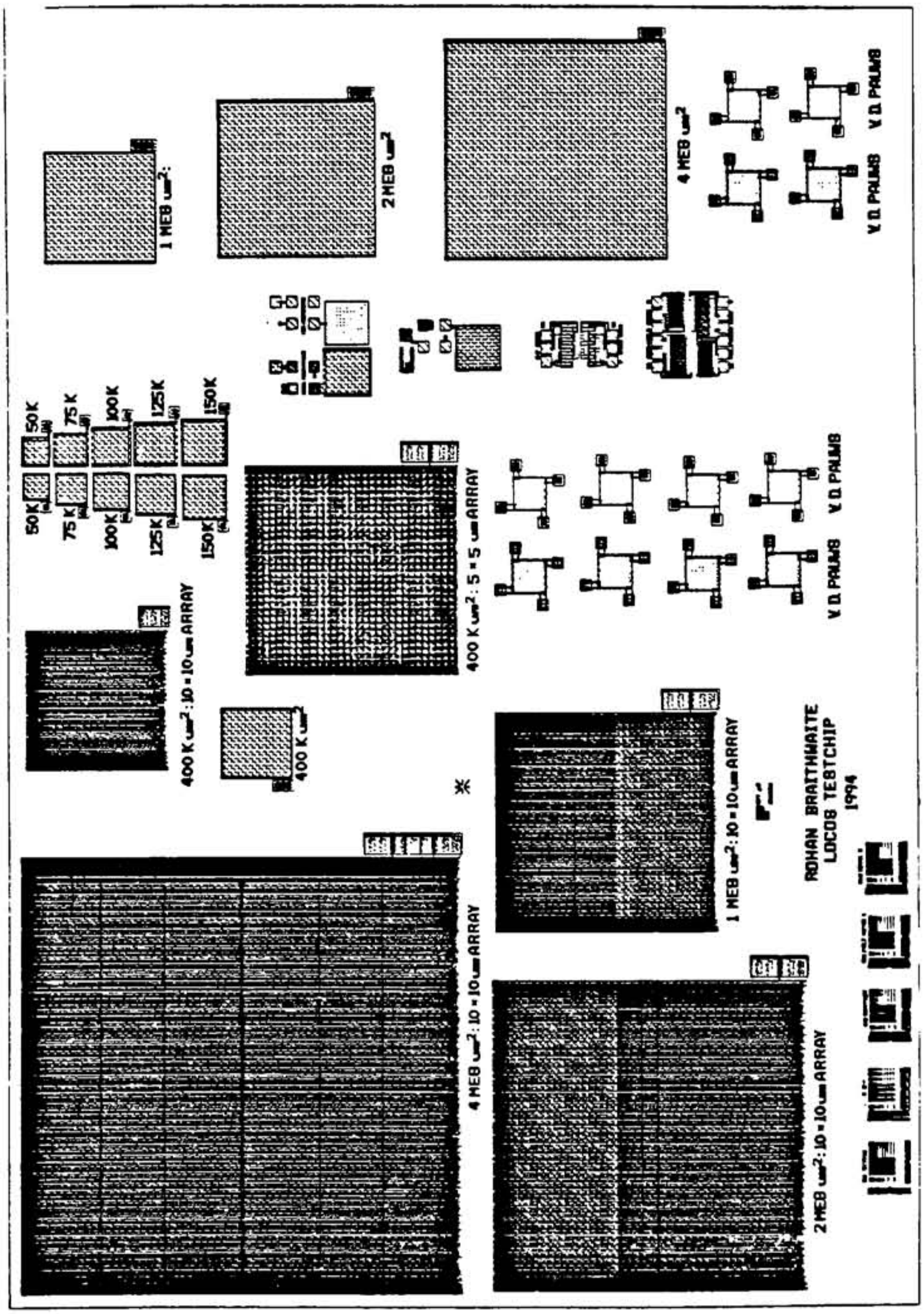


Fig. 3-1. Layout of the Test Chip design

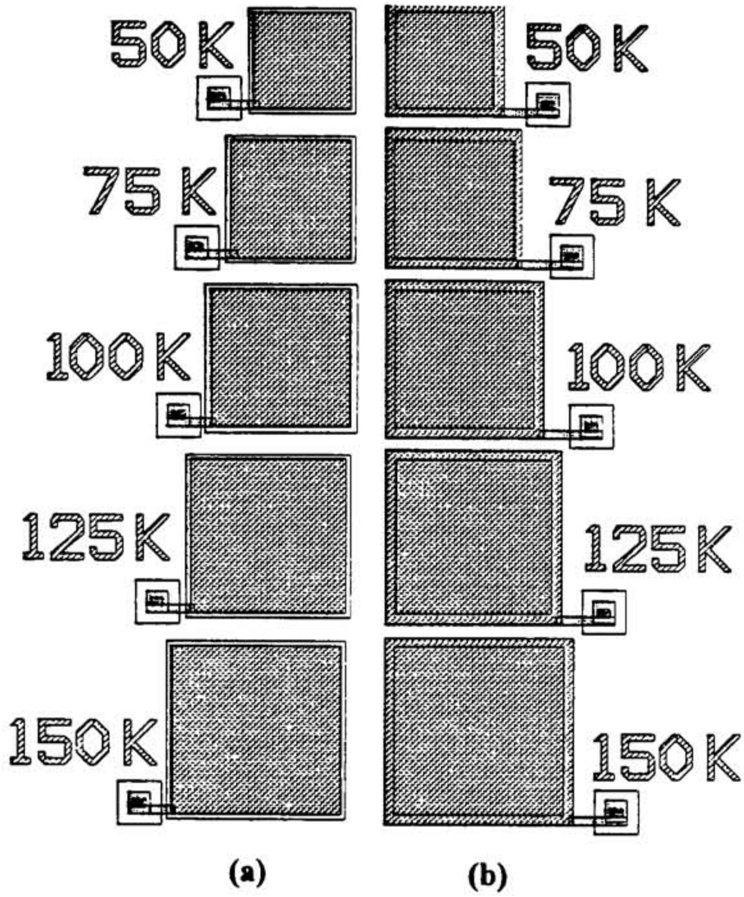


Fig. 3-2. (a) Layout of Gate surround devices, (b) Layout of Field surround devices

One thing to note on the gate surrounded capacitors is the connection of aluminum to the poly gate. The connection was taken over the field oxide instead of over the active areas. This was done to prevent the diffusion of aluminum along the grain boundaries of the poly gate and through the thin oxide, which would short out the device.

Large Field Surrounded Arrayed Capacitors

This type of capacitors was designed to amplify any leakage currents that may be associated with any etch backs. The sizes that were designed were 400 K, 1 M, 2 M, and 4 Mμm^2. Each element consisted of a 10 x 10 μm^2 active area separated by 10 μm spaces.

With the active area dimensions established, the total array could be defined which would equal the desired sizes. The area dimensions are listed below in Table 1.

Table 1

Capacitor Sizes (μm^2)	Array Dimensions	Ratio of the Edge Area to the Total Area
400 K	63 x 63	158:1
1 M	100 x 100	250:1
2 M	141 x 141	353:1
4 M	200 x 200	500:1

Fig 3-3 illustrates these structures.

Van der Pauw

Van Der Pauw structures are standard test structures for the determination of the sheet resistance of a doped layer. Structures were included in this design to achieve values for the N^+ implant in the substrate as well as the gate electrode. These structures are shown in Fig 3-4.

Field oxide-Active Area leakage Structures

These structures were taken from the RIT P-Well CMOS Test chip. Their purpose is to test for leakage associated with the active area/Field oxide areas. This is done by increasing the Field oxide-Active area edges, to amplify any effects that might be associated with these areas. Fig 3-5 illustrates these devices.

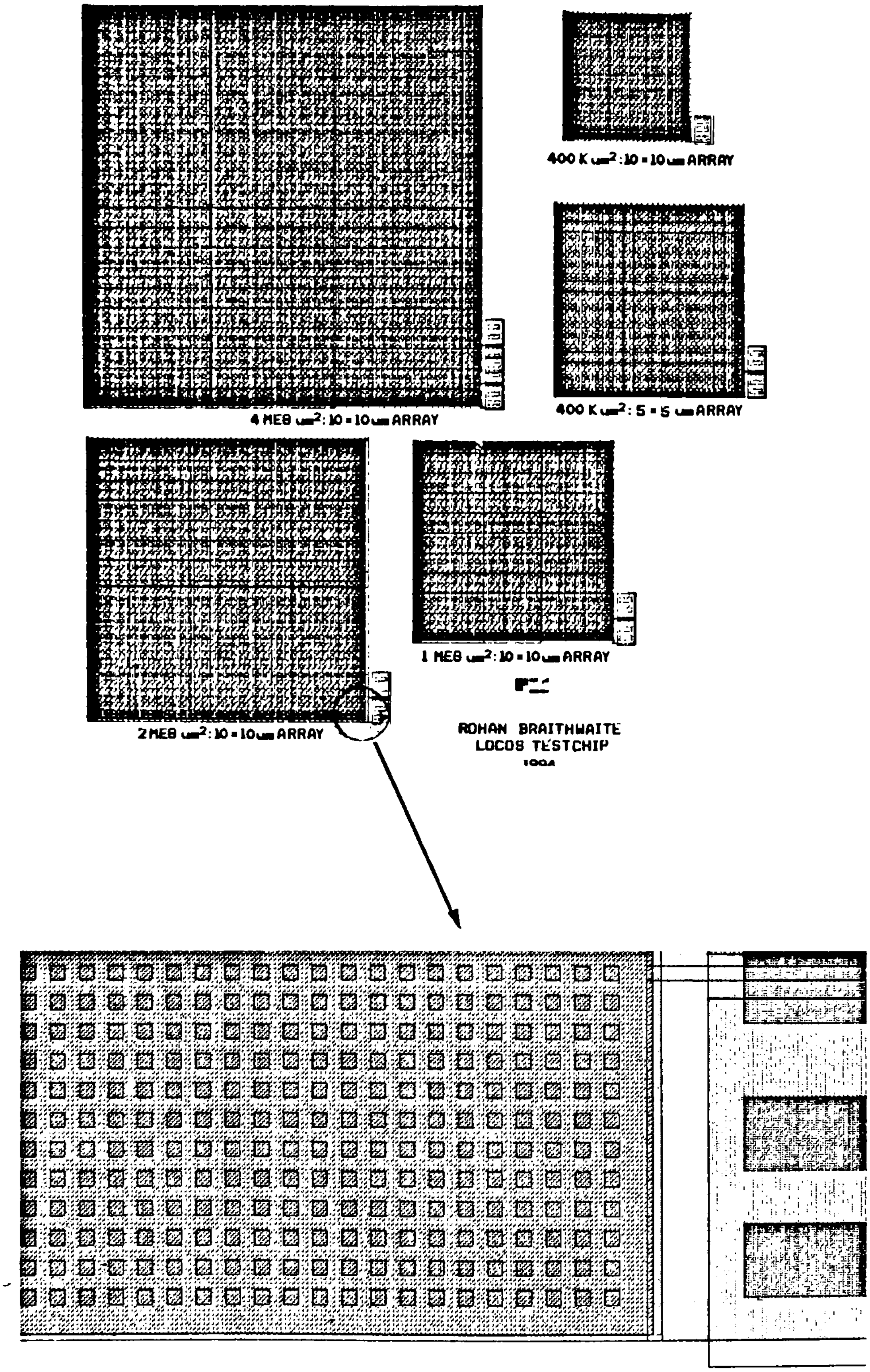


Fig. 3-3. Layout of large array type devices

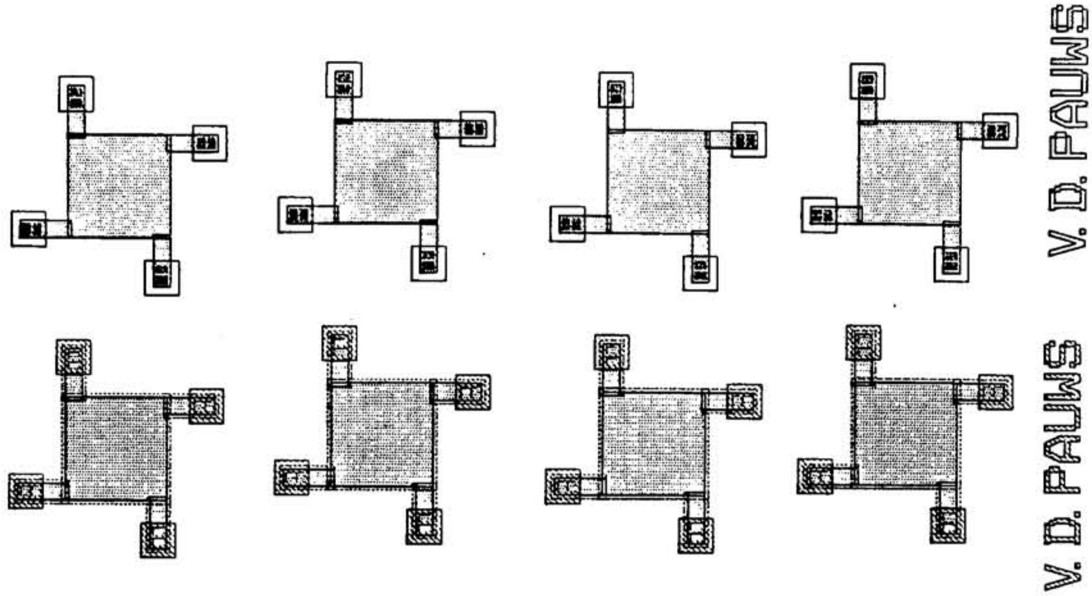


Fig. 3-4. Layout of Van der Pauws structures

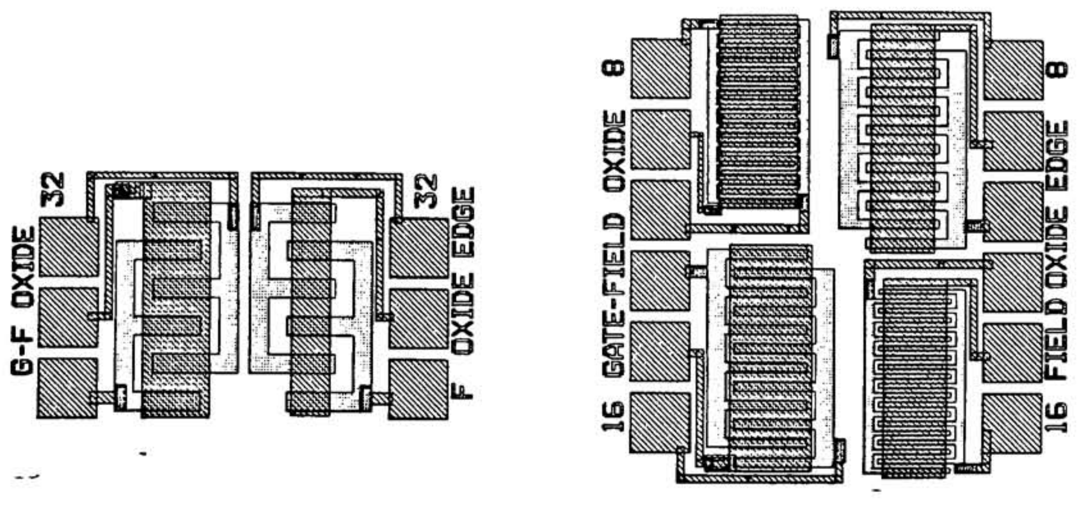


Fig. 3-5. Layout of Field oxide-Active area leakage structures

3.2 Process Description

The starting wafers were <100>, 100 mm, 10 Ω-cm, n-type Si-wafers. The backs of the wafers received a phosphorous implanted. The implant dose and energy was $1\text{x}10^{15}/\text{cm}^2$ and 110 KeV respectively. This step provides for a good ohmic contact to the back aluminum layer at the end of the process. After the back implant, the pad oxide was grown on the wafers. The thermal oxidation step was performed at 1100 C for 15 min. in a dry oxygen ambient. Following this step, a LPCVD nitride layer was deposited on the pad oxide. The nitride which was on the back of the wafers was dry etched in the RIE.

Patterning of the nitride followed the removal of the nitride from the back of the wafer. Selective etching of the nitride and the pad oxide were done in the RIE and in BOE respectively. The wet BOE also removed the pad oxide that was also on the back of the wafers.

Standard LOCOS was carried out at 1100 C for 210 min. in a wet oxygen ambient. After the field oxide growth, the remaining nitride was dry etched and the pad oxide removed in wet BOE. The next step was the growth of the Kooi oxide. This was done at 900 C in a wet oxygen ambient for 45 min..

After the growth of the Kooi oxide, the first lot split occurred. This split was between implanted and non-implanted wafers. The implanted wafers received a P^{31} implant, at a dose of $4\text{x}10^{15}$ /cm ^{2} with an energy of 120 KeV. Following this step, another split took place within the two groups. This split accounted for the different etch backs that would be performed. The etch backs were 1500 Å (group 1), 2500 Å (group2), 3500 Å (group 3), 4500 Å (group 4), 5500 Å (group 5). In all of the listed etch backs, the Kooi oxide was completely removed.

With each of the etch back groups, another split took place. This split accounted for the influence of the type of etchants used, on the device performance. Some wafers were etched in a 3.3:1 DI water: BOE mixture, while other were etched in a 7:1 DI water: HF mixture.

After the etch backs were performed, the wafers were cleaned and then taken directly to the furnace for the Tunnel oxide growth. A two-step tunnel oxide growth was performed on all wafers (for a detailed description of the tunnel oxide process, please see Appendix A). In-line analysis of the tunnel oxide using a SemiTest Surface Charge Analyzer, revealed an average interface trap density of 5.13×10^{10} /cm^2, and an average oxide charge of -4.7×10^{11} /cm^2. At the completion of the tunnel oxide growth process, the wafers were transferred to the LPCVD furnace for gate electrode deposition. A stacked gate was deposited of polysilicon and amorphous silicon (α-Si). The thin film stack and the field oxide were removed from the back of the wafers by wet poly etch and BOE respectively.

After the stacked gate formation, the gate was doped by a 4×10^{15} /cm^2, 50 KeV, P^{31} implant. Definition of the gate electrode followed the implant step. This was a dry etch process, performed in the RIE. The dopants were activated during a 900 C, 12 min. dry oxidation step.

From the activation of the gate implant, contact cuts were made in the thin polyoxide layer. 8000 Å of aluminum were then sputtered on the front and on the back side of the wafers. The front metal was then patterned and the entire lot sintered in forming gas (10% H_2, 90% N_2), for 15 min.. at 425 C. In Table-2, the in-line process measurements are listed.

Table 2

Films	Average Thickness (Å)
Pad Oxide	550
Nitride	1,550
FOX (before nitride/pad oxide removal)	10,500
FOX (after nitride/pad oxide removal)	8,800
Kooi Oxide	950
Tunnel Oxide (non-Implanted)	94 +/- 3Å
Tunnel Oxide (Implanted)	157 +/- 3Å
Amorphous Silicon	2,000
Polysilicon	4,800
Polyoxide thickness	171

A more detailed description of the processing steps are included in Appendix A.

A more detailed description of the processing steps are included in Appendix A.

3.2-1 Processing Considerations

Polyoxide Thickness

After the performance of the poly oxidation step, an oxide of unknown thickness would be formed on top of the polysilicon. Because this oxide is on the polysilicon surface, it is extremely hard to get a direct measurement of the thickness of the oxide. It was suggested by Dr. Turkman, to include a bare silicon wafer with the device. From this wafer, an oxide thickness can be obtained by means of ellipsometry. The resulting thickness would then be multiplied by 1.6 (the rate of oxidation of polysilicon to a single crystal substrate). The value would be a close estimation of the polyoxide thickness.

Poly/α-Si Stacked Gate

A stacked gate was used to take advantage of the α-Si film's irregular grain boundaries. The grain boundaries would be regions in which the dopants would tend to segregate, which would result in the dopant becoming trapped or diffusion of the dopant slowed. Another advantage of the stacked film is that the poly/α-Si interface would be an area which would slow the diffusion of dopants.

The α-Si film was deposited first at 550 C., then remove from the furnace while the polysilicon deposition temperature is reached. When the temperature is reached and stabilization has also been achieved, then the wafer were replace back into the furnace and the last stage of the stacked gate was formed. Processing the stacked gate in this manner removing the wafers from the furnace until the polysilicon deposition temperature is achieved, would reduce the possibility of the grain boundaries in the α-Si film realigning themselves and transforming the film into a polysilicon film.

3-3 Supreme IV Simulations

Supreme IV simulations were performed to see what effects the etch backs would have on the compressive stress located at the bird's beak. Fig 3-6 shows the stress localized at the transition region between the Kooi oxide and the FOX. In Figs. 3-8, 3-10, 3-12, 3-14, and 3-16, it can be seen that the stress gradient, at the transition region between the thin oxide and the FOX, increases as the etch back increases.

Fig 3-7 show the pressure contours associated with Si substrate and the Field oxide before the growth of the tunnel oxide. It can be seen that the pressures within the oxide before the tunnel oxide growth is reduced when the tunnel oxide is grown. This would indicate that the anneal steps, incorporated in the tunnel oxide growth procedures, did relieve the built up pressures in the Si substrate and the oxide film.

In Fig. 3-9, 3-11, 3-13, 3-15 and 3-17, it is shown that as the etch backs increases, the position of the bird's beak tip of the LOCOS structure, moves closer to a region of maximum stress. This can result in thinner oxides grown at those points which would result in an oxide with low reliability as discussed in Chapter 1.

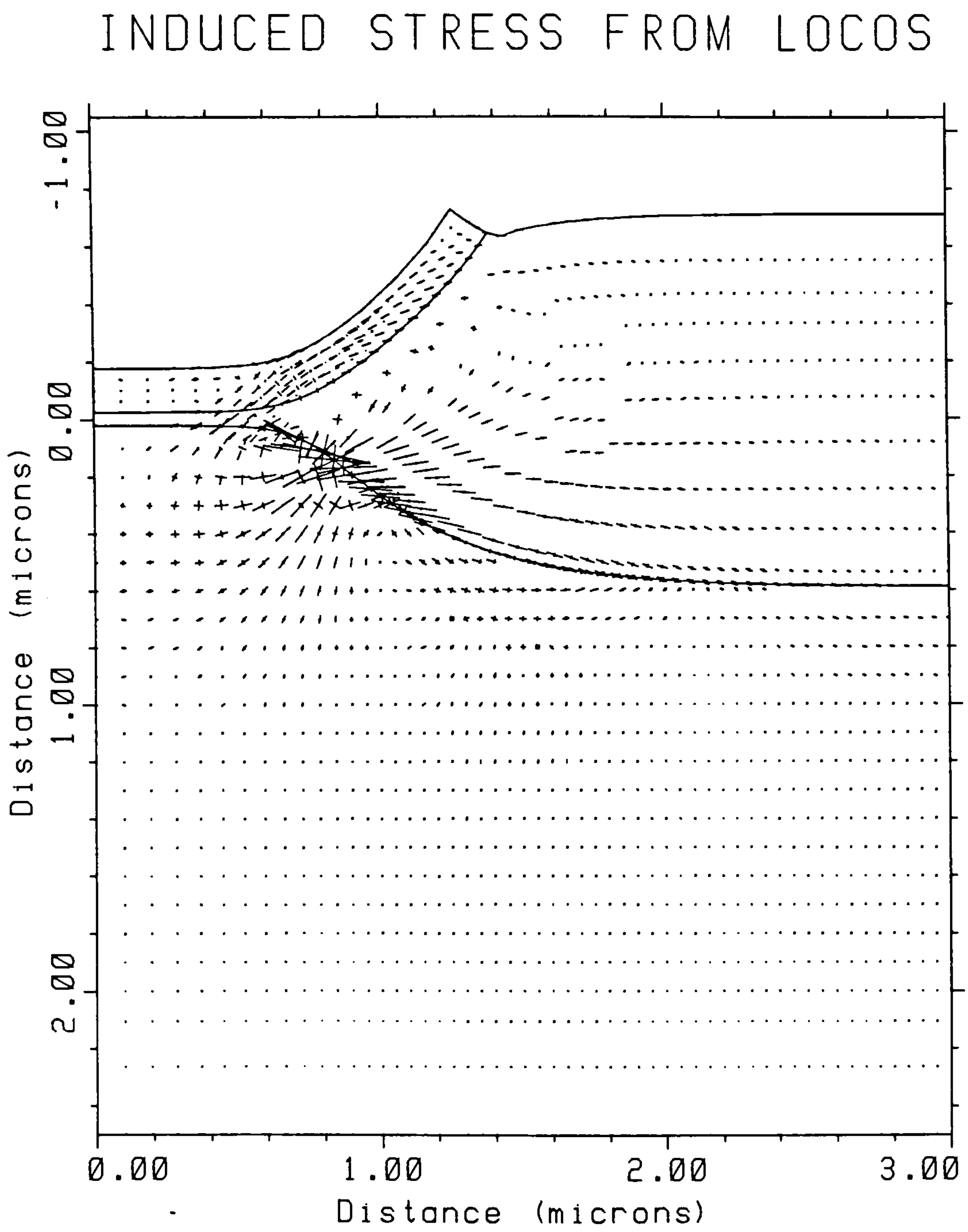


Fig. 3-6. Supreme IV output plot showing stress gradients before tunnel oxide growth

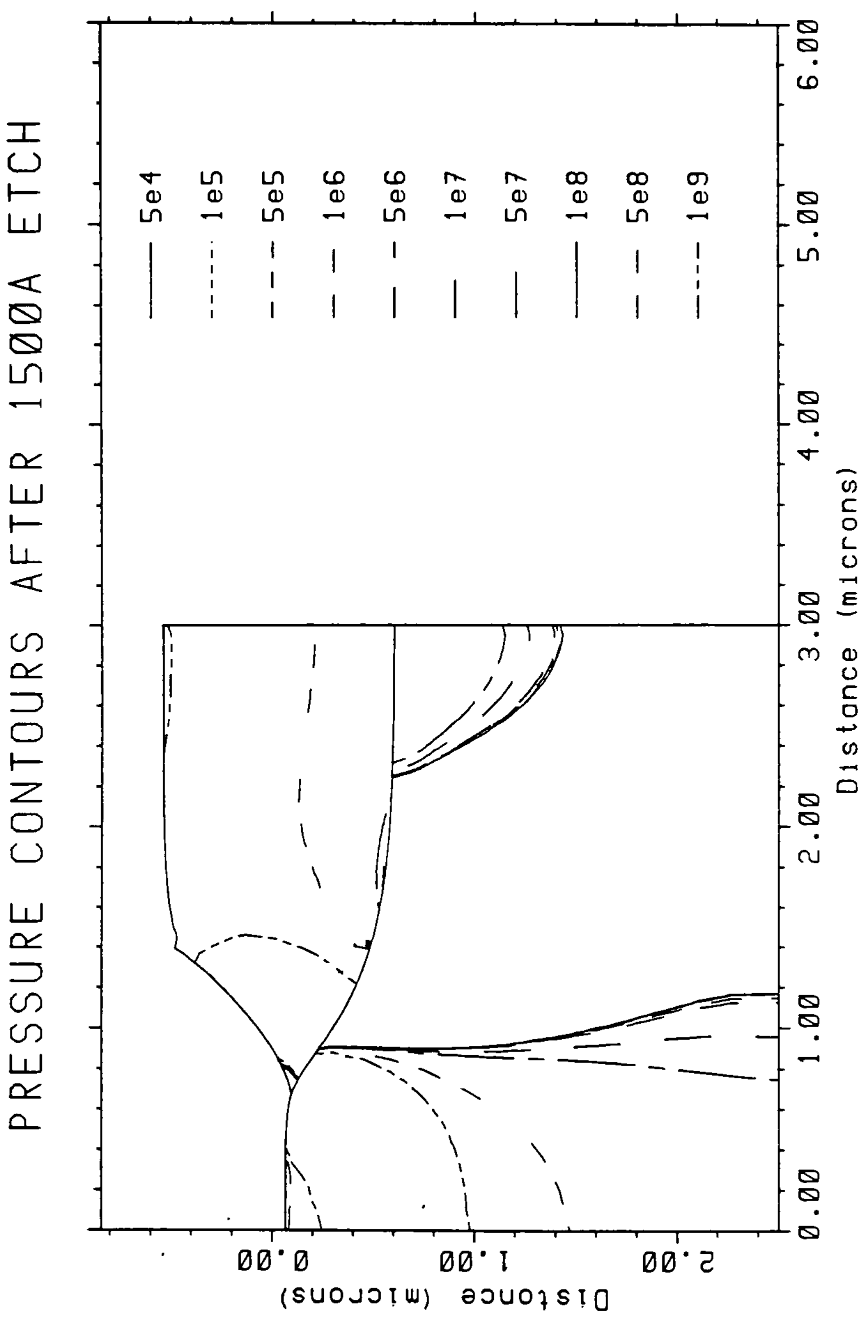


Fig. 3-7. Supreme IV output plot showing pressure contours before tunnel oxide growth

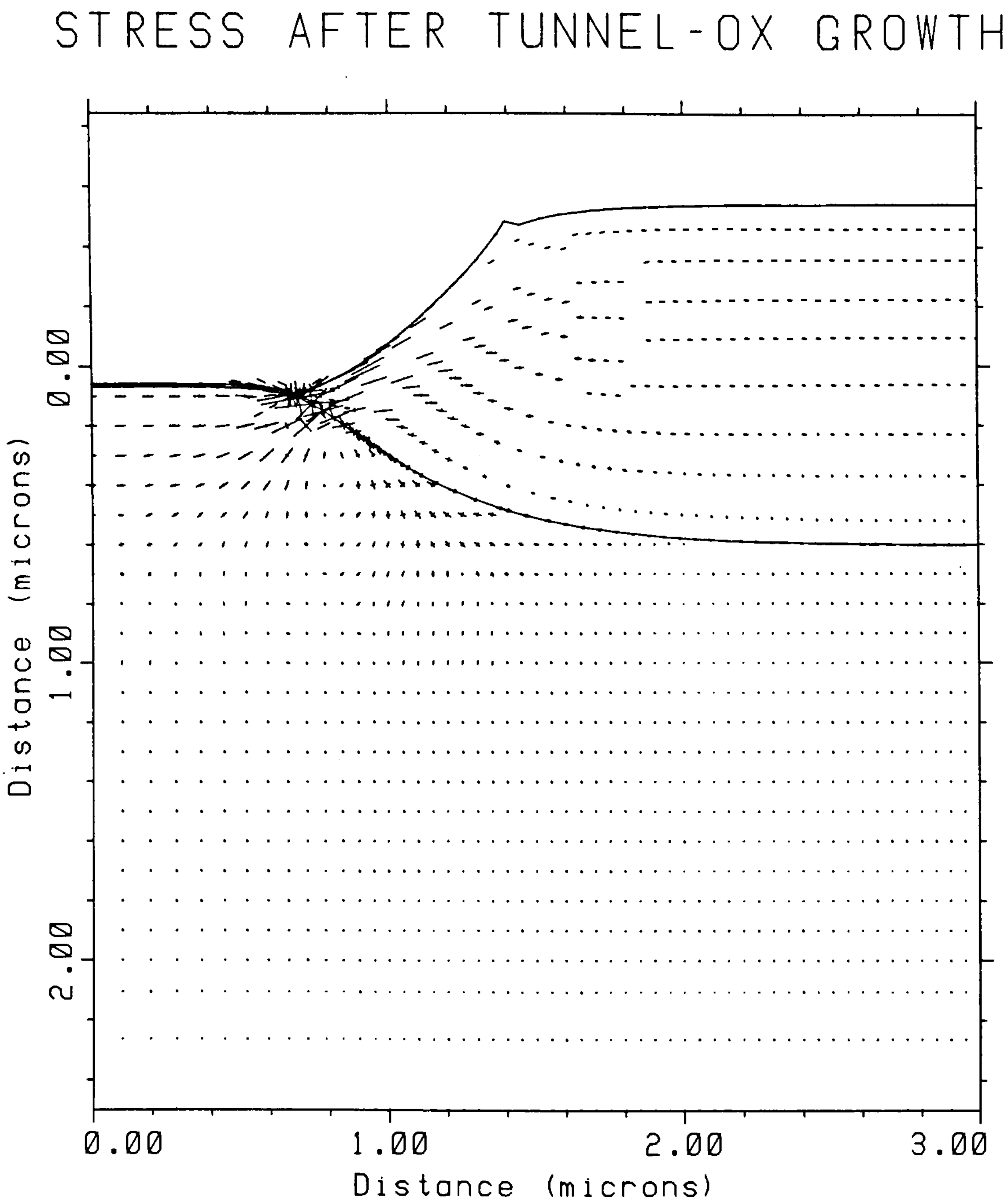


Fig. 3-8. Supreme IV output plot showing stress gradient for 1500 Å etch back after tunnel oxide growth.

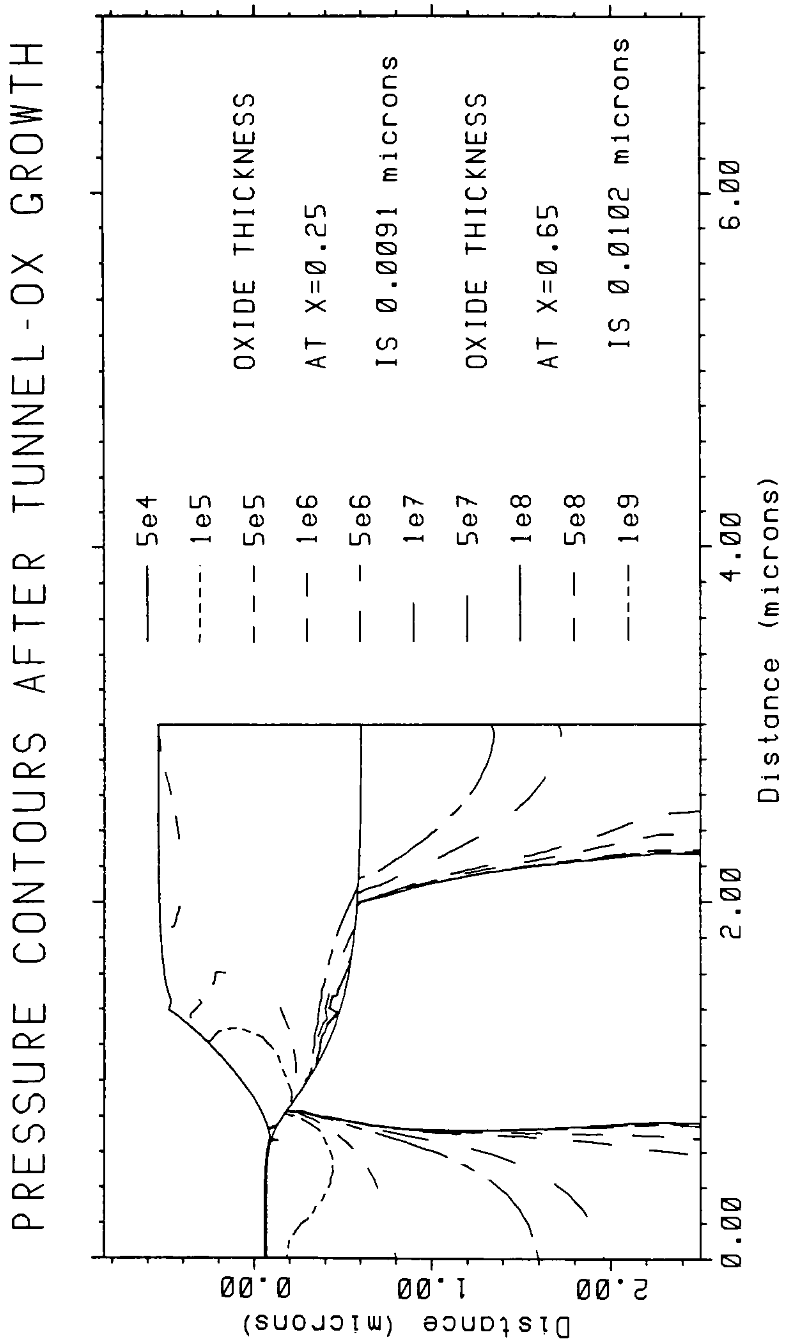


Fig. 3-9. Supreme IV output plot showing pressure contours for 1500 Å etch back after tunnel oxide growth.

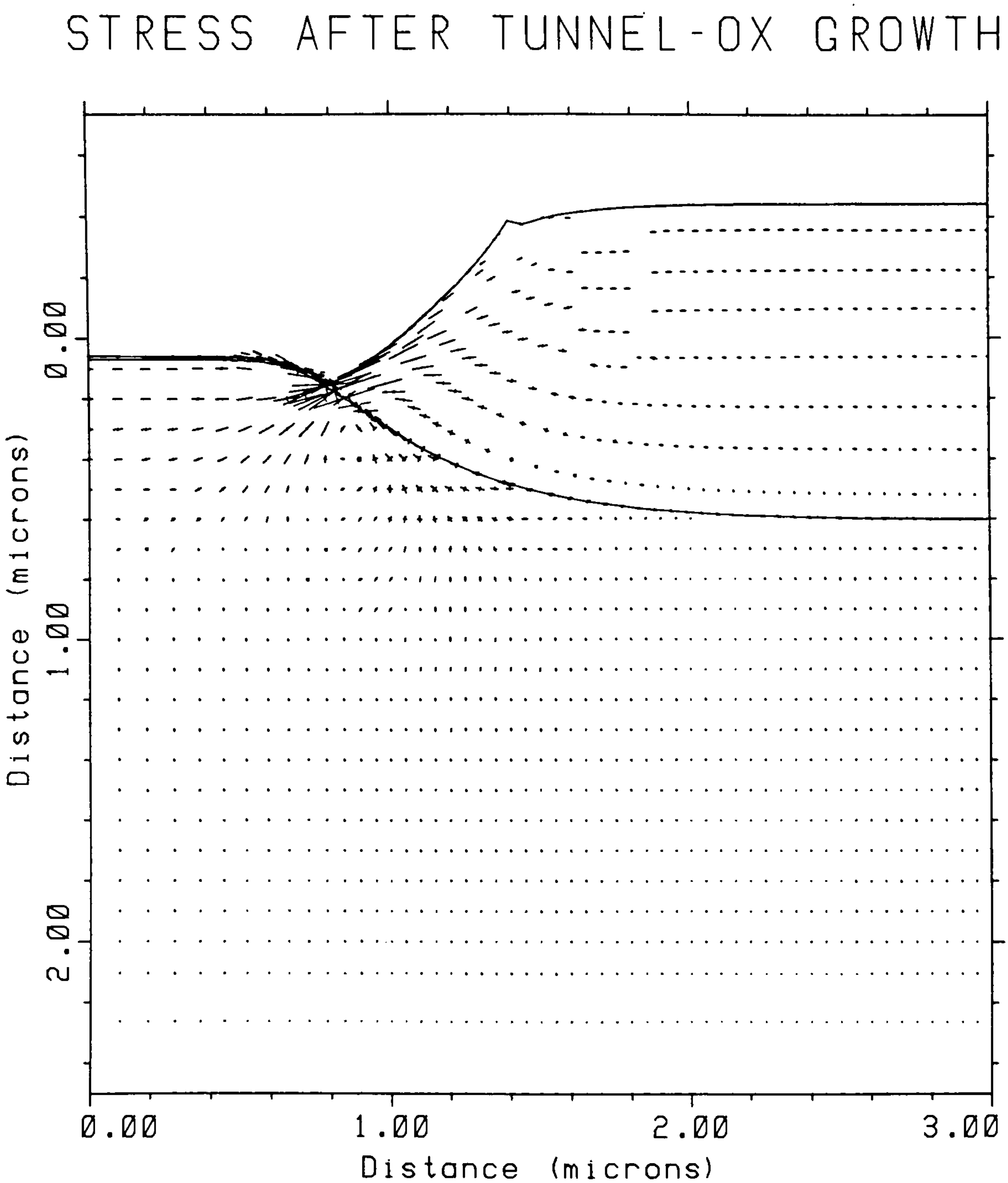


Fig. 3-10. Supreme IV output plot showing stress gradient for 2500 Å etch back after tunnel oxide growth.

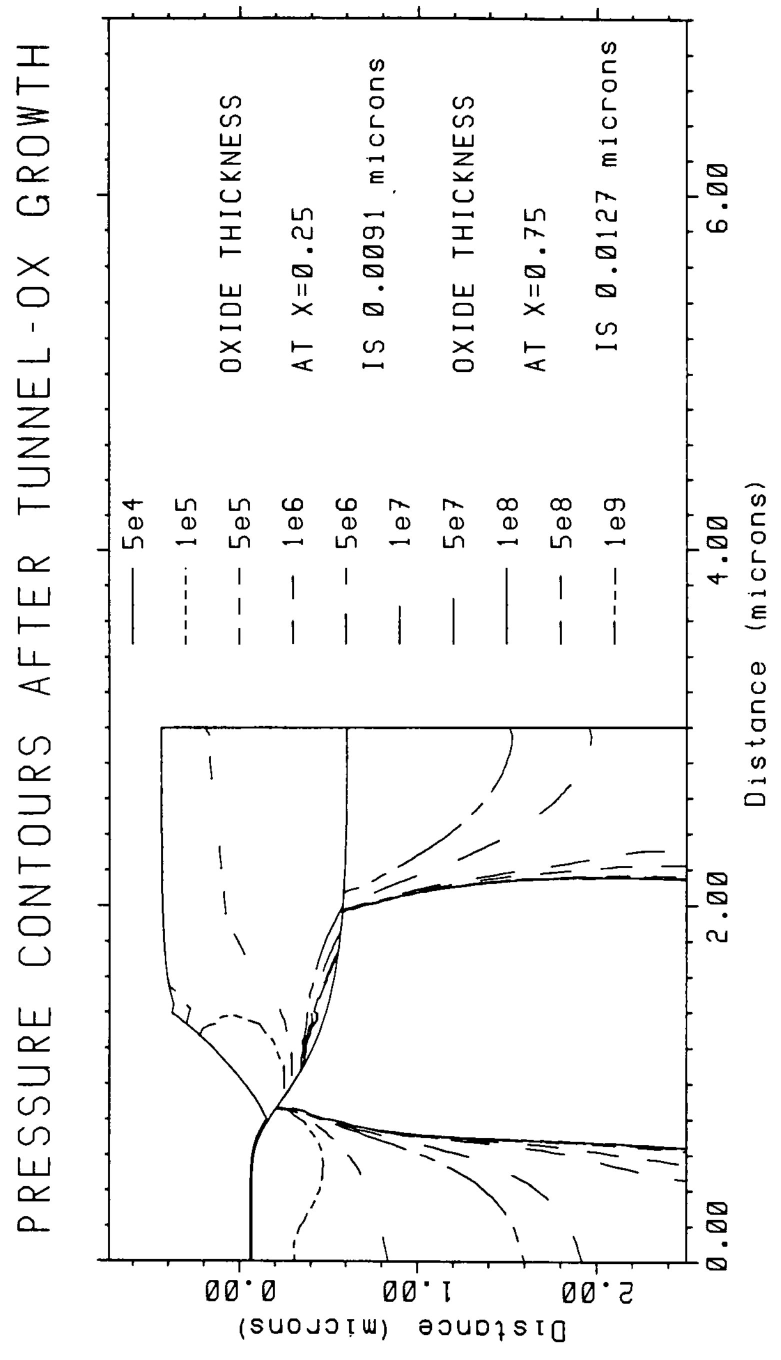


Fig. 3-11. Supreme IV output plot showing pressure contours for 2500 Å etch back after tunnel oxide growth.

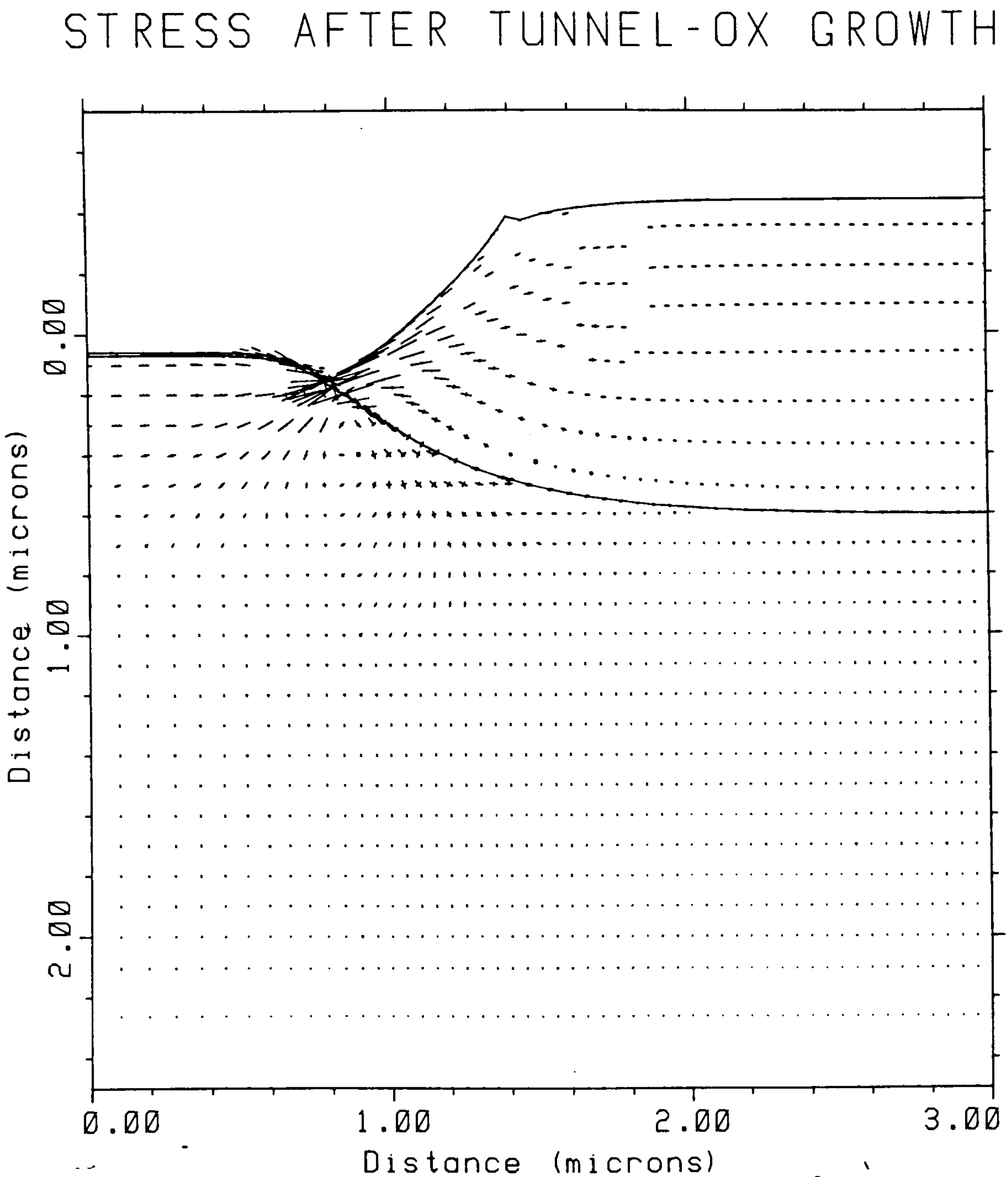


Fig. 3-12. Supreme IV output plot showing stress gradient for 3500 Å etch back after tunnel oxide growth.

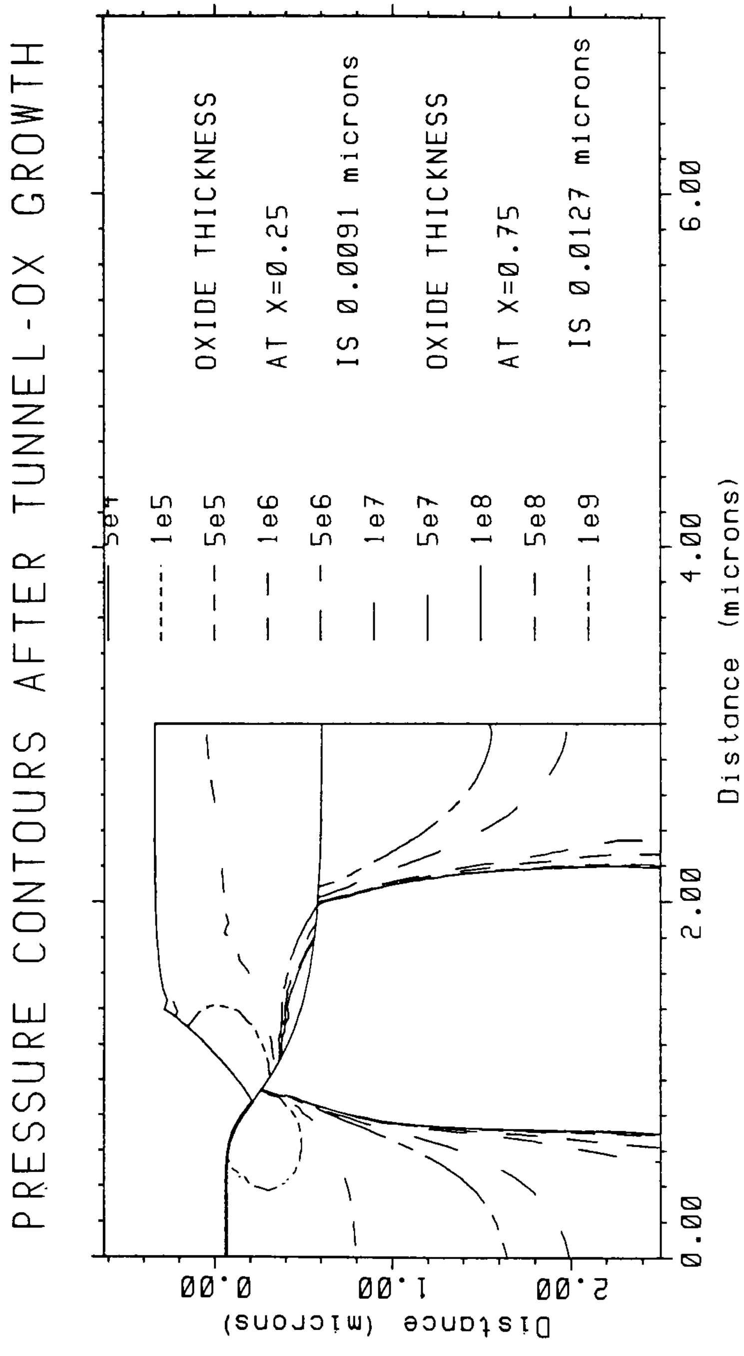


Fig. 3-13. Supreme IV output plot showing pressure contours for 3500 Å etch back after tunnel oxide growth.

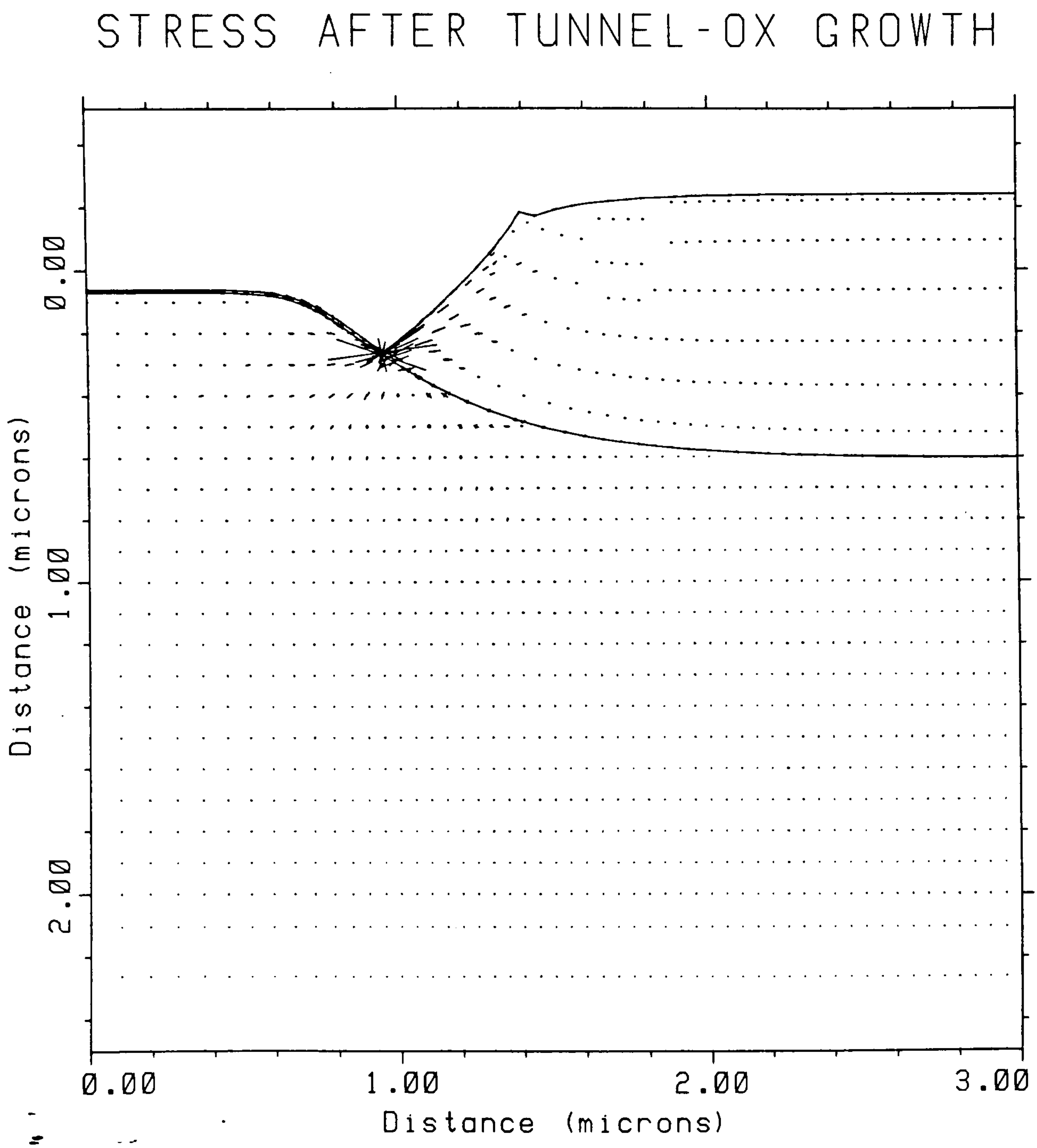


Fig. 3-14. Supreme IV output plot showing stress gradient for 4500 Å etch back after tunnel oxide growth.

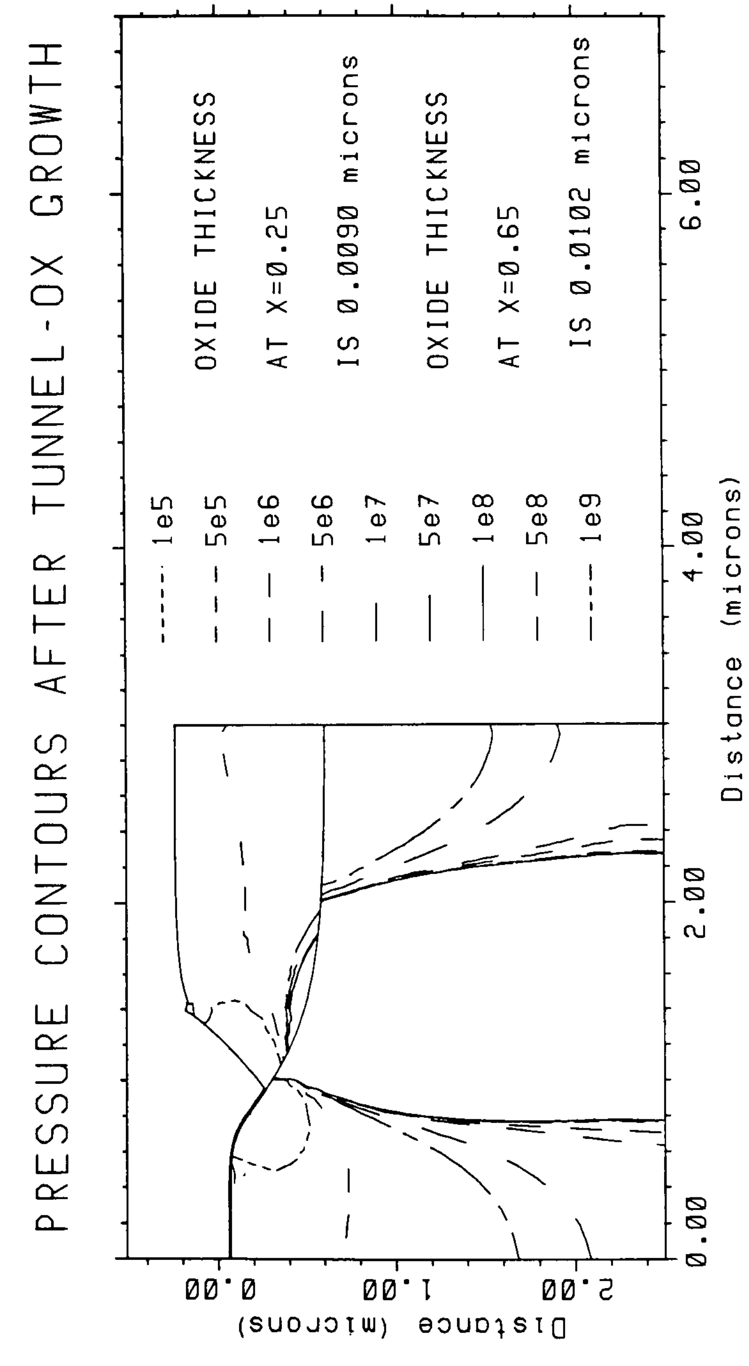


Fig. 3-15. Supreme IV output plot showing pressure contours for 4500 Å etch back after tunnel oxide growth.

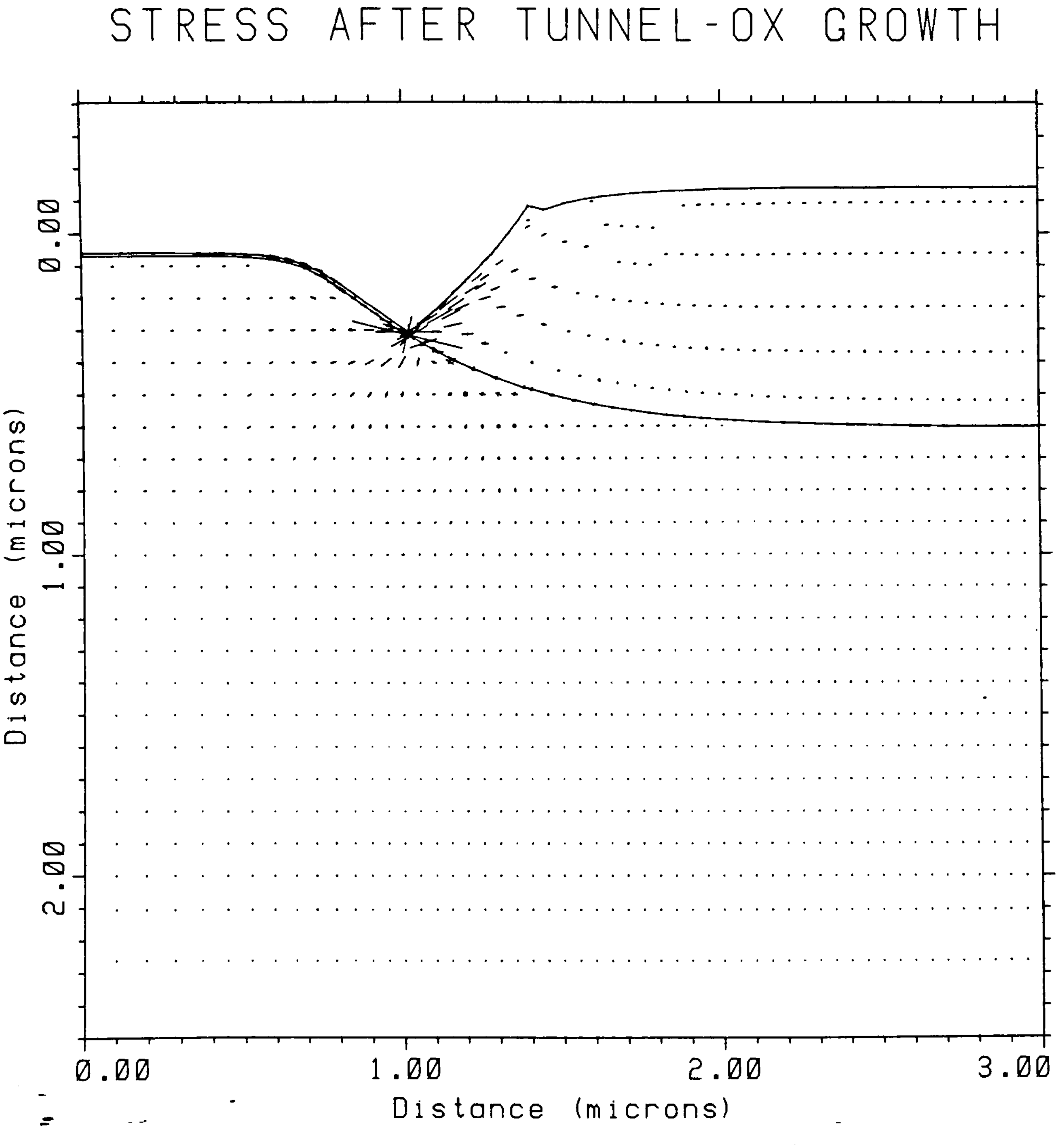


Fig. 3-16. Supreme IV output plot showing stress gradient for 5500 Å etch back after tunnel oxide growth.

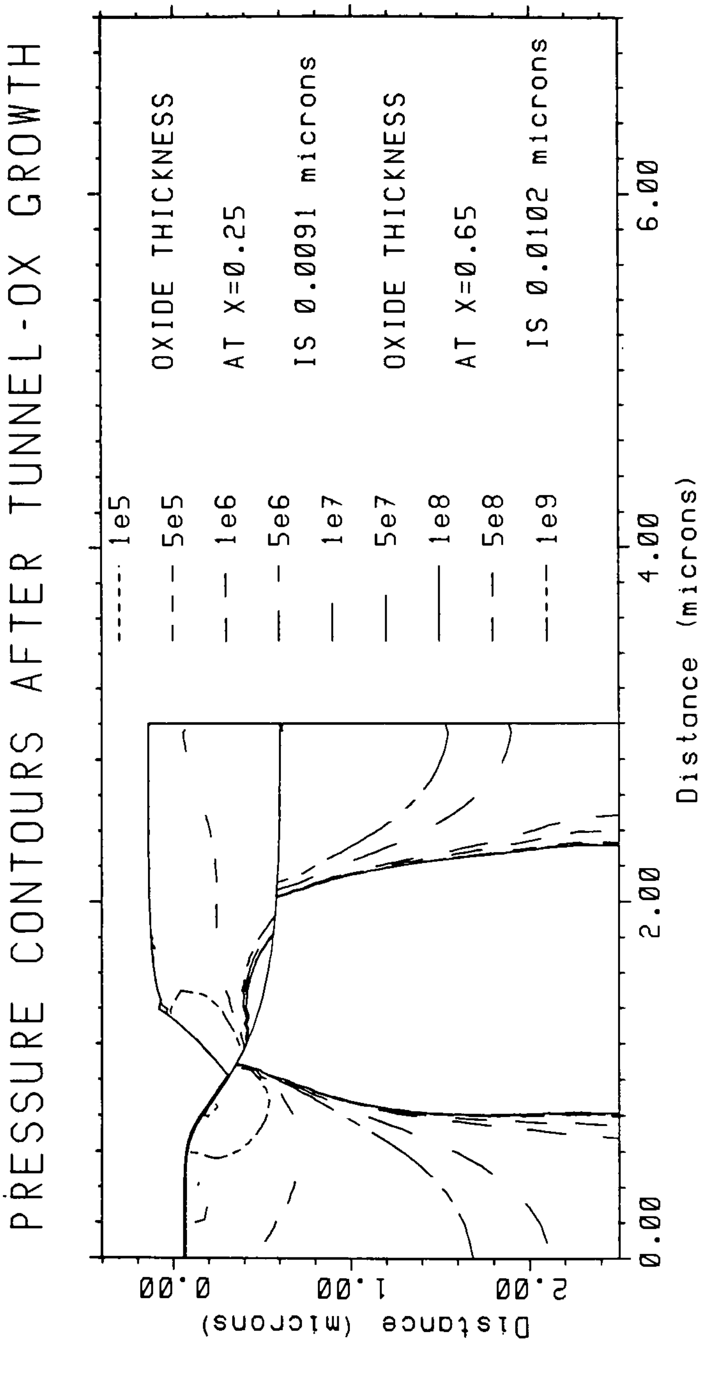


Fig. 3-17. Supreme IV output plot showing pressure contours for 5500 Å etch back after tunnel oxide growth.

4.0 Results and Discussion

4.1 Activation of the Stacked Gate

The activation time of the stacked gate used in this work was 12 min. in a dry oxygen ambient. The resulting sheet resistance profile of the gate is shown in Fig 4-1. From SUPREM III simulation however, this time may be increase by 5 mins, without the dopant going through the oxide. However, the formation of oxide ridges are possible for the higher activation times, and should therefore be considered cautiously (see Appendix C for Supreme III results)

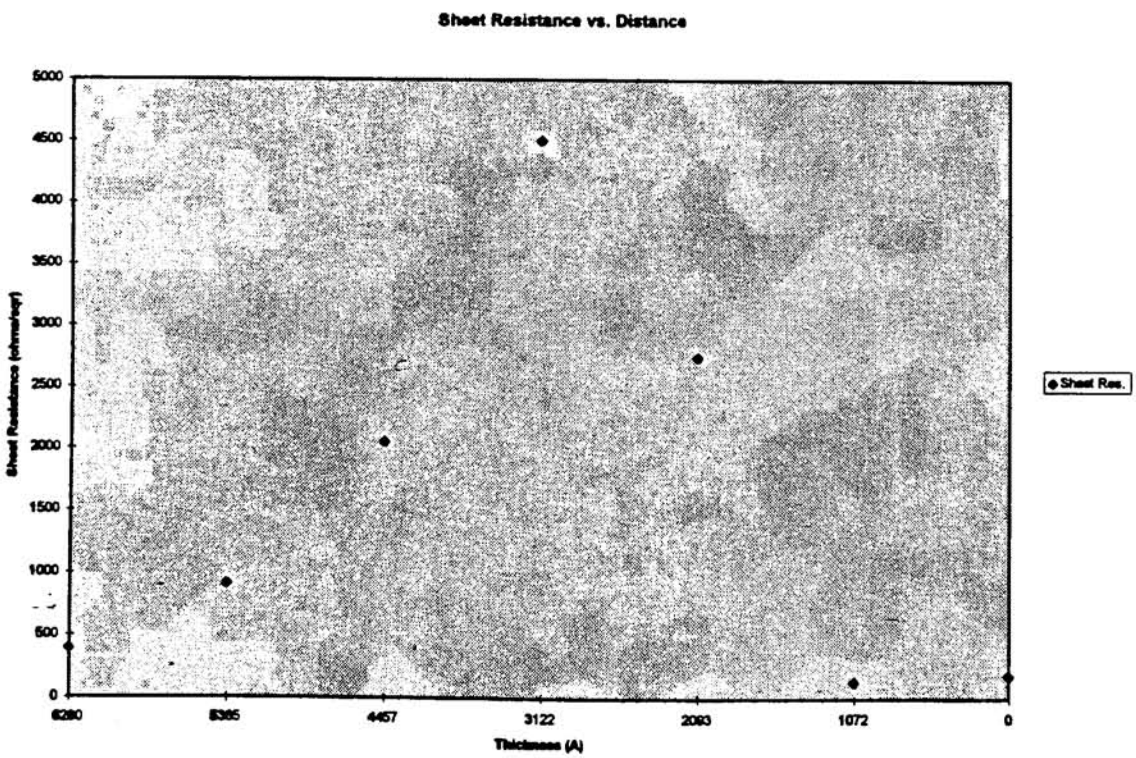


Fig. 4-1. Sheet resistance profile of the stacked gate.

4.2 Electrical Testing of the Capacitors

4.2-1 Dielectric Strength of the Oxide

The dielectric strength of the oxide was determine using the ramp voltage test as described in Section 2-5.3. The value of the series resistance was obtained from Fig. 4-2, and is being reported as 7.4 KΩ for the 50 Kμm^2 capacitor. The series resistance for the 100 Kμm^2 devices would be approximately 3.7 KΩ. Using all the appropriate approximations as described in Section 2-5.2, the resulting voltage on the oxide was 12.8 V for the unimplanted samples, and 12.6 V, for the implanted samples. The resulting dielectric strength of the was 13.6 MV/cm, and 8 MV/cm, for the unimplanted and the implanted samples respectively (see Appendix B for calculations). It is thus assumed that the intrinsic quality of the oxide is very good and categorizes this project's tunnel oxide as C-mode.

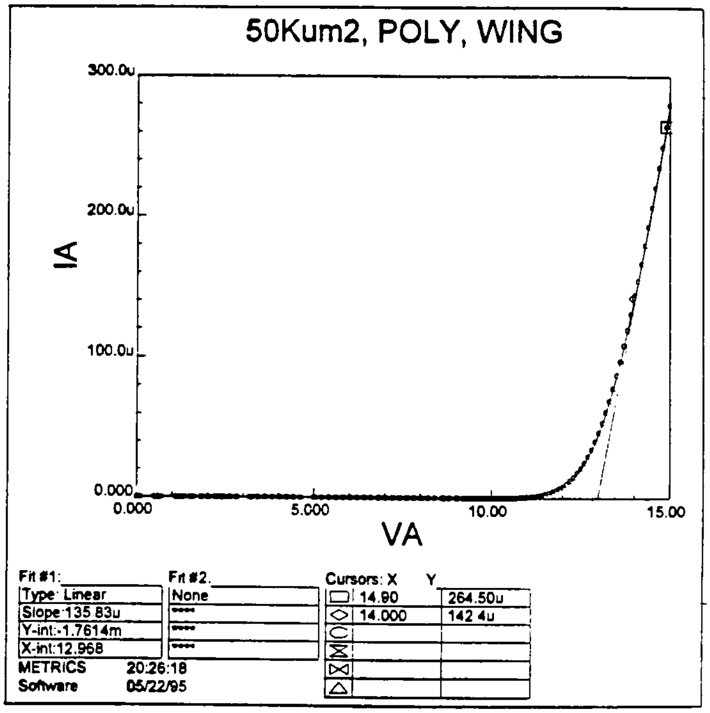


Fig. 4-2. I-V curve of 50 Kμm^2 test structure

4.2-2 C-V Analysis

Using a Keithley 595 Quasistatic CV meter, C-V measurements were taken. The characteristic High and Low frequency plots could not be obtained due to the overwhelming influence of stray capacitance associated with the set up. These stray capacitance were focused in the Signatone wafer holding assembly associated with the overall system. Many attempts were made to nullify the stray capacitances. The best acquired plot is shown in Fig 4-3. The Keithley system did however provide an encouraging result. As a part of its programming, the equivalent oxide thickness is calculated. This value provided by the system did verify the optically obtained result of 94 Å.

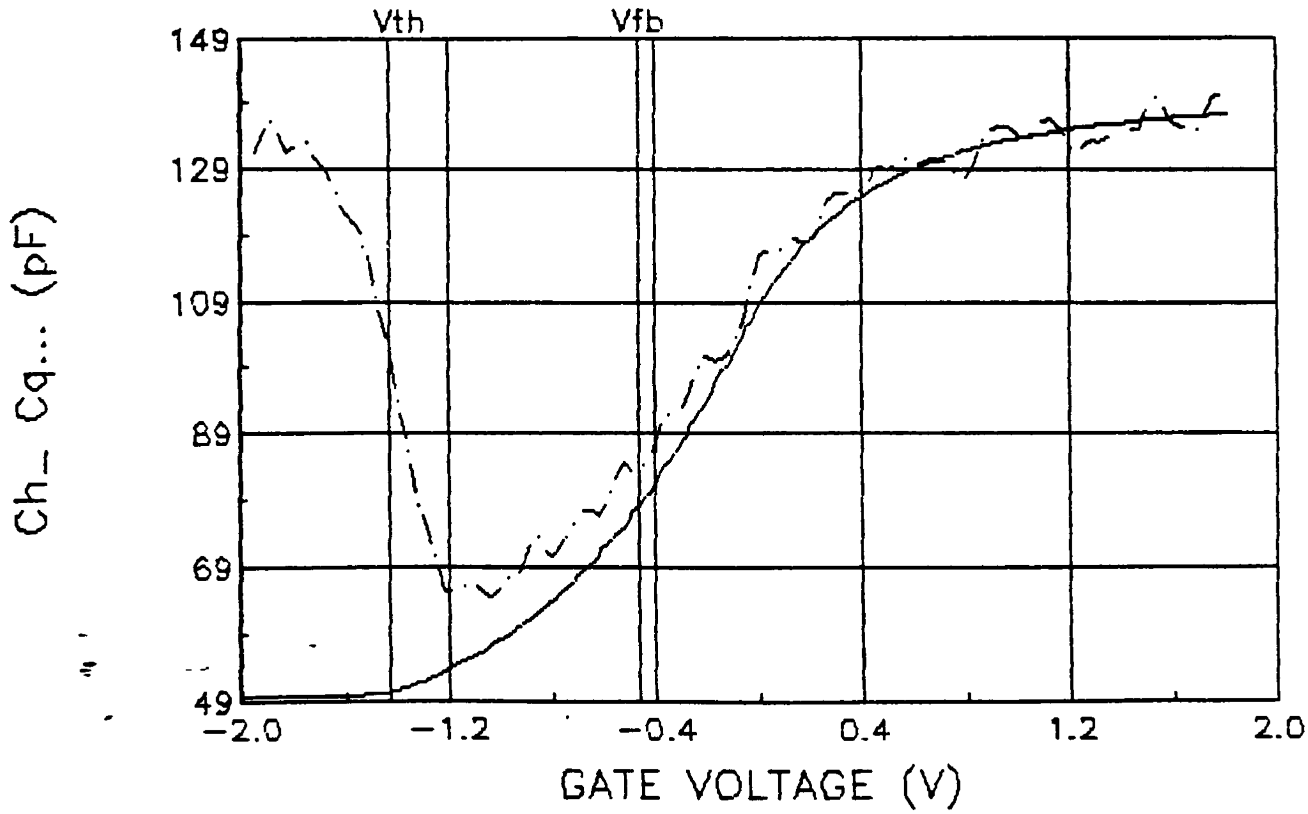


Fig. 4-3. Low and High frequency C-V plots

4.2-3 Capacitor leakage test results at low level injection

In order to obtain the low level injection leakage current, a ramp voltage test was utilize.

Current-voltage (I-V) curves were obtained while limiting the oxide leakage current density to 1 $\mu A/cm^2$. For all samples tested, the conduction current was noticeable .1 $\mu A/cm^2$. The voltage corresponding to a current density of 1 $\mu A/cm^2$ was recorded. This was the criterior which was used so that the samples could be compared.

Samples in which the conduction current density of 1 $\mu A/cm^2$ occurred at low voltages were categorized as mode A samples. If devices conducted this current density at higher voltages, they would be classified as C mode samples. Any sample who's voltage corresponding to this conduction current, was in between the A and the C mode samples, would be classified as B mode samples.

Mode C samples were limited to the those that required an applied gate voltage no less than 85% of the highest voltage obtained in that sample. It should be noted that the A and B mode samples, reflects the defects and the weak spot distribution across the wafer respectively. Group comparison was based on the C-mode samples. This is due to the fact that this study focuses on the intrinsic correlation between the oxide etch back and each sample leakage and reliability. The A, B, and C mode distinction made in this section is not the same distinction as those for the dielectric strength distribution. These modes are specific to the categories defined.

In Fig. 4-4a tc 4-4d, the distribution of the oxide voltage needed to cause 1 nA (1 $\mu A/cm^2$ current density), of conduction current to occur among the C-mode capacitors of 100 Kμ

m^2 area. The distribution was obtained by calculating the percentage of the samples as a function of the applied voltage resulting in a 1 nA current density. Distribution for group 1, group 3, group 4, and group 5 are presented as Fig 4-4a, Fig 4-4b, Fig 4-4c, and Fig 4.4d respectively. From these figures, it can be inferred that there is no oxide degradation for the etch back ranging from 1500 Å to 4500 Å. For the samples which received the 5500 Å etch back however, significantly higher leakage was shown.

Similar tests were performed on the arrayed type capacitors. Any edge related effects which might be present would be magnified. Only the 400 Kμm^2, and the 1 Mμm^2 arrayed capacitors were tested. This was chosen in this manner so that any defect related effects which are more probably with the large area devices would not be included. Amplification of any edge-related effects in the 400 Kμm^2 and 1 Mμm^2, were 50 and 100 times more edge intensive compare to the 100 Kμm^2 single blocked Field-surrounded devices. Fig. 4-5a to 4.5d illustrates the distribution of the oxide voltage required for 10 nA conduction current in the 1 Mμm^2 area arrays. The current level was increased for the different areas so that the 1 A/cm^2 current density can be maintained

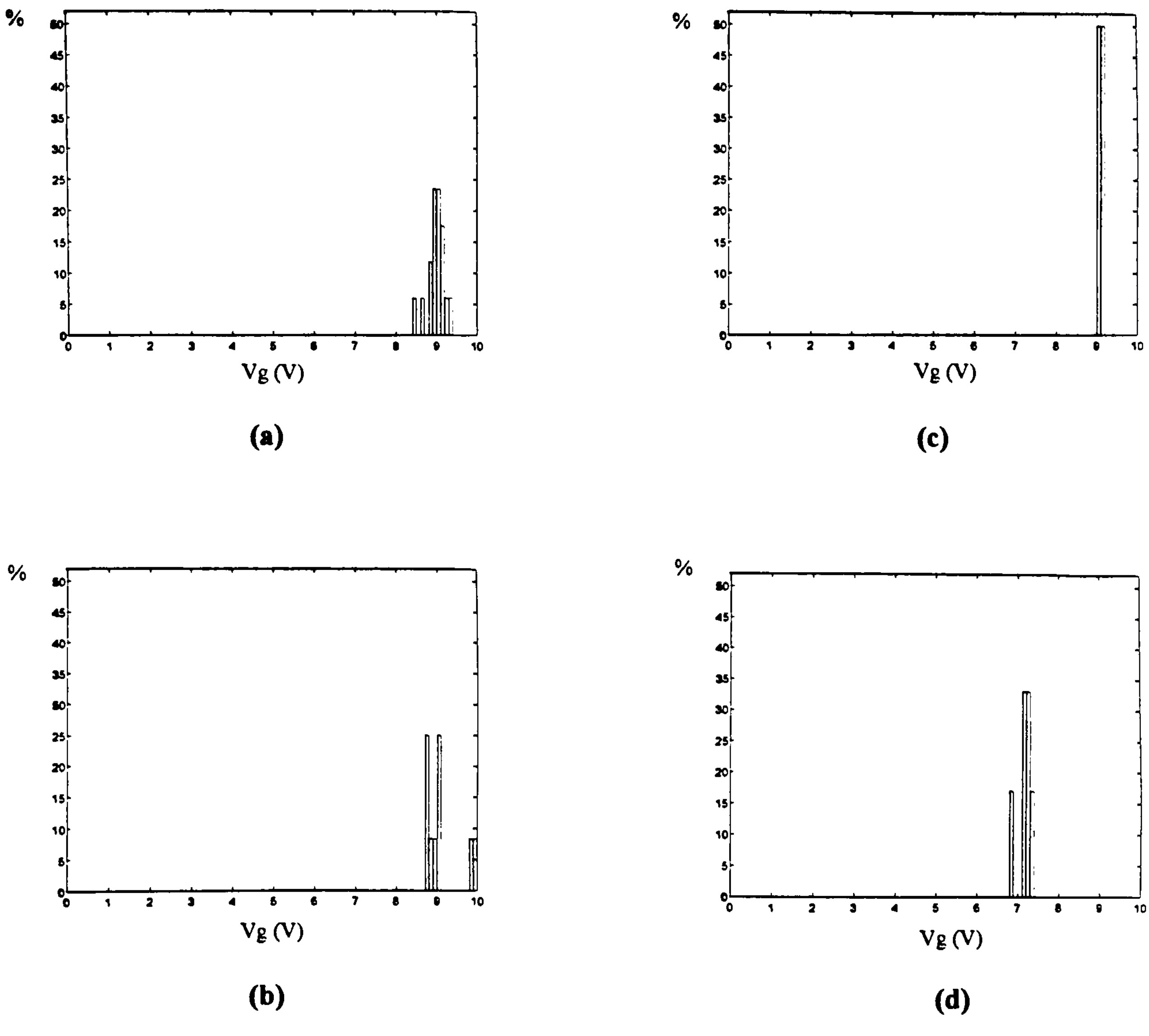


Fig. 4-4. Voltage distribution at 1nA leakage among C mode, unimplanted, 100 Kμm² samples. (a) 1500 Å etch back. (b) 3500 Å etch back. (c) 4500 Å etch back. (d) 5500 Å etch back. All etch backs performed in BOE

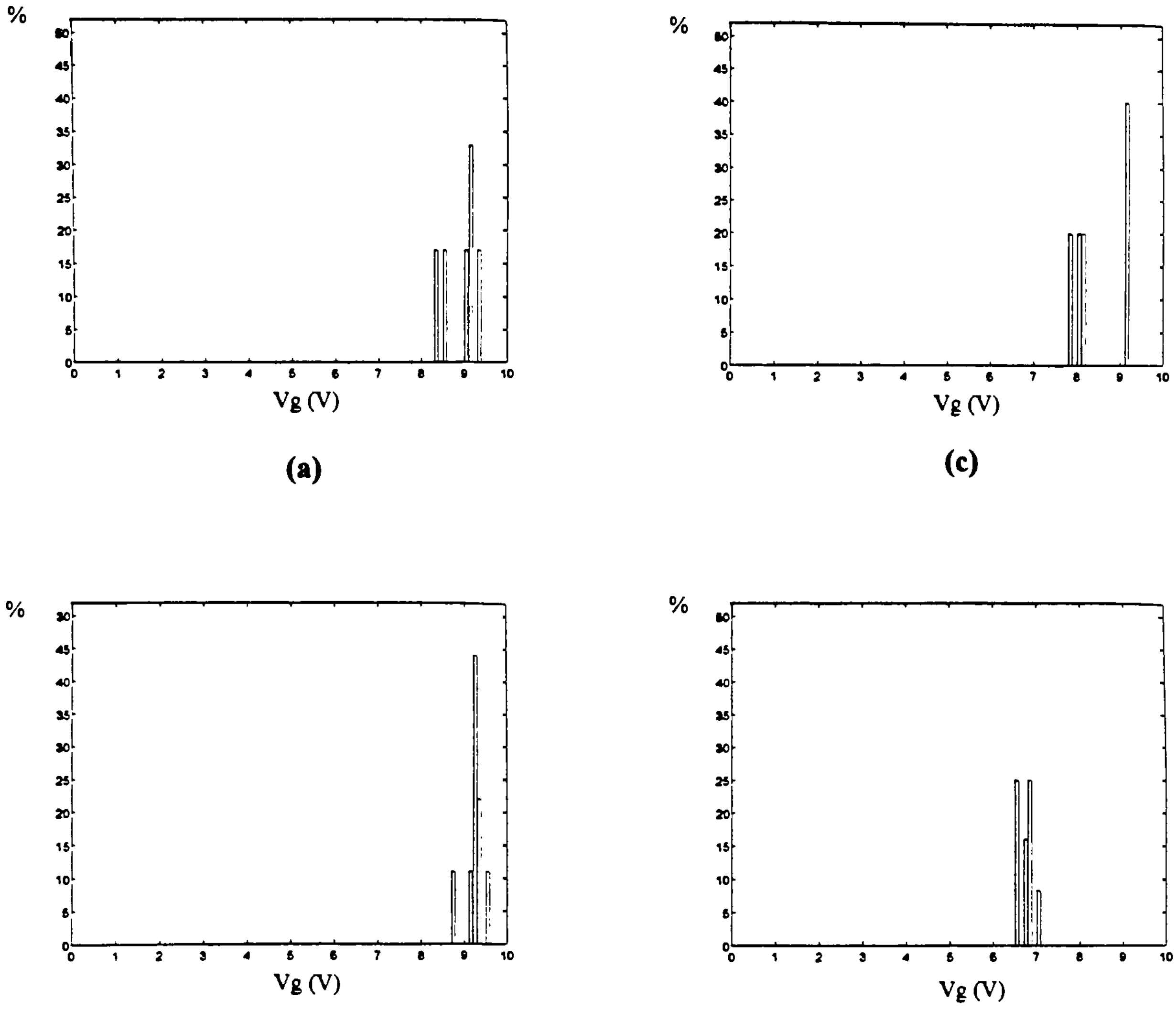


Fig. 4-5. Voltage distribution at 10nA leakage among C mode, unimplanted, 1 Mμm^2 samples. (a) 1500 Å etch back. (b) 3500 Å etch back. (c) 4500 Å etch back. (d) 5500 Å etch back. All etch backs performed in BOE

Among the samples tested, there were no discernible leakage degradation with an increase in oxide etch backs. Only in the case of the 5500Å etch back (as was before), could any degradation be observed. The same was also true for the 400 Kμm^2. There was a lack of correlation between the oxide leakage with the oxide etch back, only at 5500 Å. One point which must be made is that there was a significant decrease in the number of samples tested that qualified as C-mode samples. In the 1 Mμm^2 samples, only 24% qualified of the total samples tested, while 74% of the 100 Kμm^2 samples qualified.

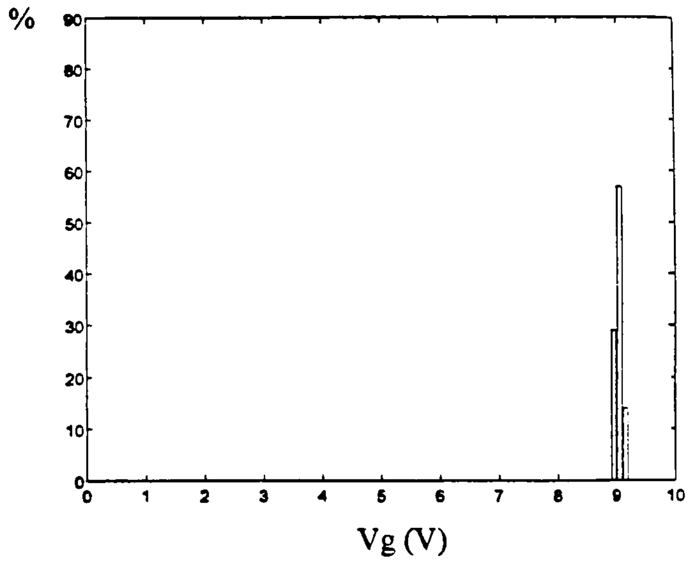


Fig. 4-6 Voltage distribution at 1nA leakage among C mode, unimplanted, 100 Kμm^2 samples. Etch backs performed in BOE. The extent of the etch back was 1500 Å etch back.

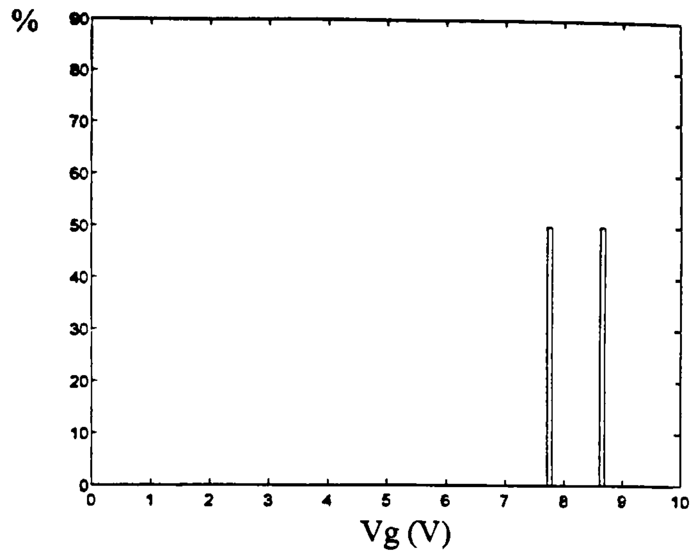


Fig. 4-7. Voltage distribution at 10nA leakage among C mode, unimplanted, 1 Mμm^2 samples. Etch backs performed in BOE. The extent of the etch back was 1500 Å etch back.

Investigation of the impact of the etchants used on the oxide leakage was also performed at the same current density as above (1 μA/cm^2). Fig 4-6 and 4-7 are voltage distribution analysis for the 100 Kμm^2 and 1 Mμm^2 samples. These samples were processed identically to those of group 1 with the only exception being the etchant utilized was HF while in group 1 BOE was used. In the same manner Fig. 4-8 and 4-9 shows the voltage distribution analysis for the samples processed identically to group 4 with only the etchant being the difference. A comparison of Fig. 4-6, Fig. 4-4a, Fig 4-7 and Fig 4-5a, reveals that exact composition of the HF mixture had almost no effect on the sample leakage. The same observation can also be noted for Fig. 4-8, Fig. 4-4d, Fig 4-9, and Fig. 4-5a.

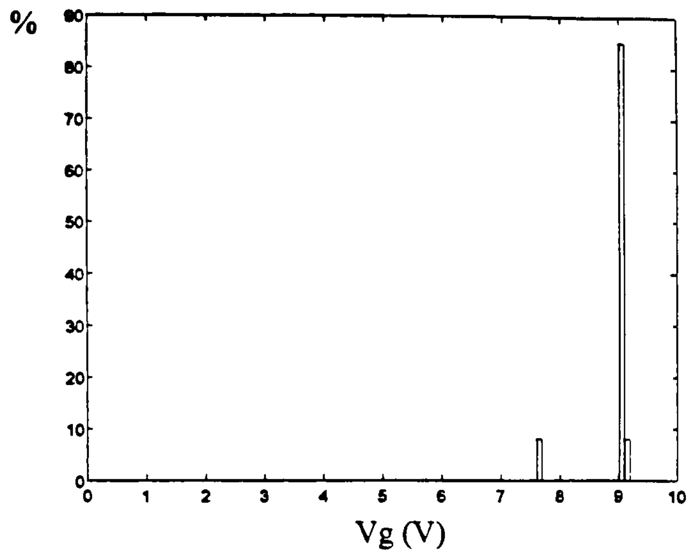


Fig. 4-8. Voltage distribution at 1nA leakage among C mode, unimplanted, 100 Kμm^2 samples. Etch backs performed in HF. The extent of the etch back was 4500 Å etch back.

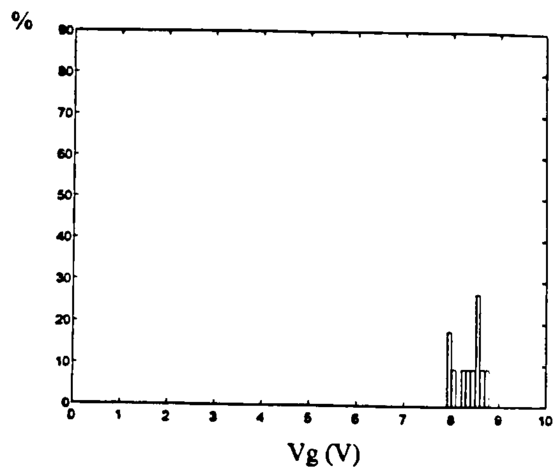


Fig. 4-9. Voltage distribution at 10nA leakage among C mode, unimplanted, 1 Mμm^2 samples. Etch backs performed in HF. The extent of the etch back was 4500 Å etch back.

4.2-4 Implantation Test results

Results from devices fabricated over the heavy n^+ implant are shown in Fig. 4-10 and 4-11. These figures are for 100 Kμm^2 area, from group 1 and group 4. Comparisons were made based on the electric field and not on the applied voltage. This is because the tunnel oxide over the heavy implant is 67% thicker than that of the non-implanted samples. Comparing Fig 4-10 to Fig. 4-4a, and Fig. 4-11 to Fig. 4-4d, shows that the oxide over the implant was of poorer quality than that of the non-implanted samples. This may be attributed to the incorporation of more dopants into the oxide, which might be modifying the structure of the oxide.

The field requirement for a 1 $\mu A/cm^2$ leakage current density was approximately 5.4 MV/cm ((8.4 V/157 x 10^{-8}cm)= 5.4 MV/cm) for the implanted samples compared to 8.4 MV/cm ((7.9 V/94 x10^{-8}cm)= 8.4 MV/cm) for the non-implanted samples. Although the oxide required a smaller field for the same leakage current density, the voltage applied was the same. This would lead to a device which would be symmetric for both the Erase and the Write cycles of an EEPROM.

As far as the impact of the etch backs on the leakage of the n^+ implanted samples, the distribution shown in Fig 4-10 and Fig 4-11 again indicated almost no correlation between oxide leakage and oxide etch backs, at least up to 4500 Å.

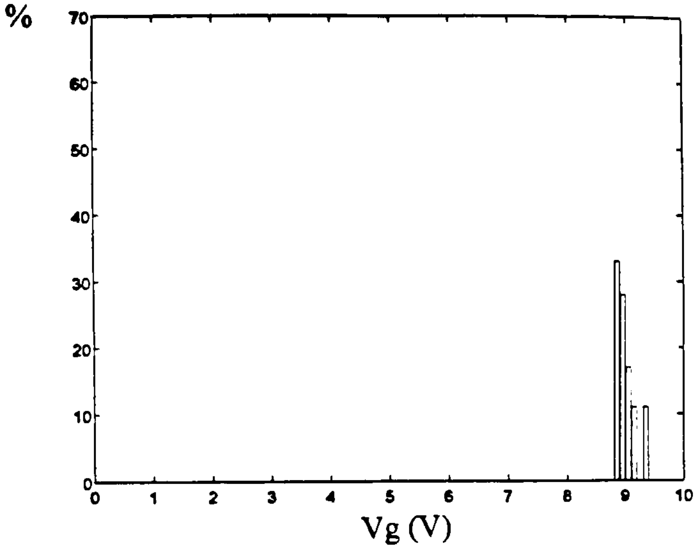


Fig. 4-10. Voltage distribution at 1nA leakage among C mode, implanted, 100 Kμm^2 samples. Etch backs performed in BOE. The extent of the etch back was 1500 Å etch back.

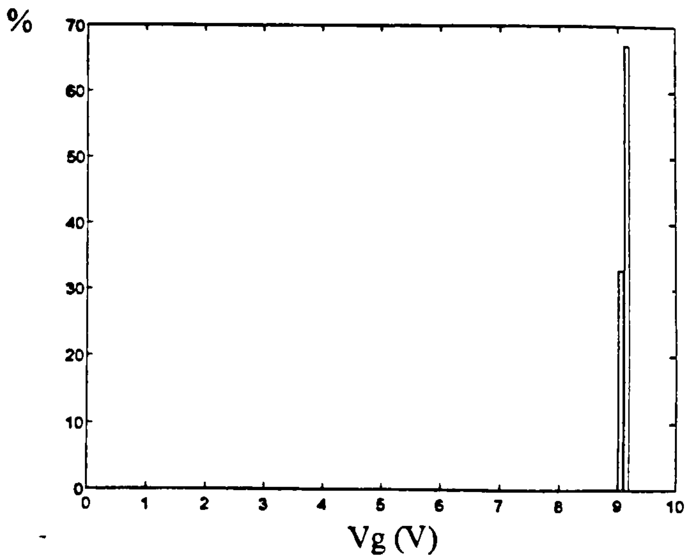


Fig. 4-11. Voltage distribution at 1nA leakage among C mode, implanted, 100 Kμm^2 samples. Etch backs performed in BOE. The extent of the etch back was 4500 Å etch back.

4.2-5 Time-Dependent Dielectric Breakdowns (TDDB) under Constant Current Stress Test Results

The reliability of the samples was tested under constant current stress conditions. Unimplanted, buffered HF etched, 100 Kμm^2 samples were tested at a current level of I= 500μA. This corresponds to a stress current density of .5 A/cm^2. A total of 25 samples were tested from each group. From the data obtained, the longest time-to-breakdown t_{BD} values were 252 s, 78 s, 132 s, and 124 s, for samples from groups 1, 3, 4, and 5 respectively. The respective time to 50% failure values were 65s, 9s, 12 s and 11 s, respectively. Please note that there were no processed samples from group 2 that met the criteria's described, by which this testing was done.

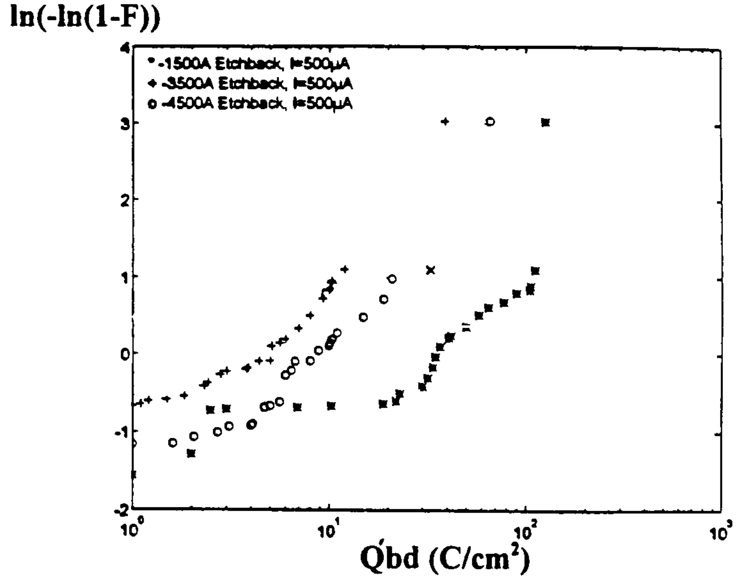


Fig. 4-12 Cumulative failure plots for unimplanted, BOE etched, 100 Kμm^2 samples from group 1 (1500 etch back), 3 (3500 etch back), 4 (4500 etch back). The constant current stress level is 500 μA (.5 A/cm^2)

Fig 4-12 illustrates the statistical data plotted as the log(-ln(1-F)) vs. the observed charge to breakdown per unit area (Q_{BD} (C/cm^2)). The TDDB data obtained at a stress current of I= 500 μA clearly shows that the group 1 samples has the highest endurance to charge flux. The group 5 samples had the lowest Q_{BD} values out of all the samples tested.

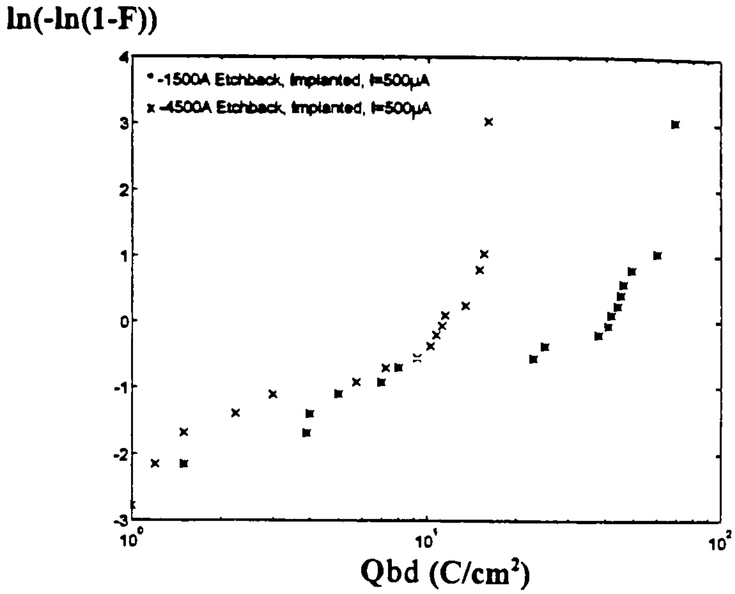


Fig. 4-13. Cumulative failure plots for unimplanted, BOE etched, 100 Kμm^2 samples from groups 1, and 4 . The constant current stress level is 100 μA (.1 A/cm^2)

TDDB was tests were also performed at a constant current stress of 100 μA for 17 samples from group 1 and group 4. The corresponding statistical plots are shown in Fig 4-13. The maximum observed t_{BD} was 570 s, and 378 s from the samples from group 1 and from group 4 respectively. The respective time to 50% failure value were 490 s, and 70 s. Again, the samples from group 1 exhibited a superior endurance to the stress test. Pre-tunnel implant samples were also studied under TDDB. Fig. 4-14 shows the statistical plots of samples from group 1 and group 4. The capacitor area was 100 Kμm^2 and all the tested samples had their respective etch backs done in BOE. The constant stress current level was I= 500 μA. From the acquired data, the longest t_{BD} values were 140 s, and 31 s, for sample from group 1 and group 4 respectively. Again it is shown that the oxide endurance is degraded by increasing oxide etch back.

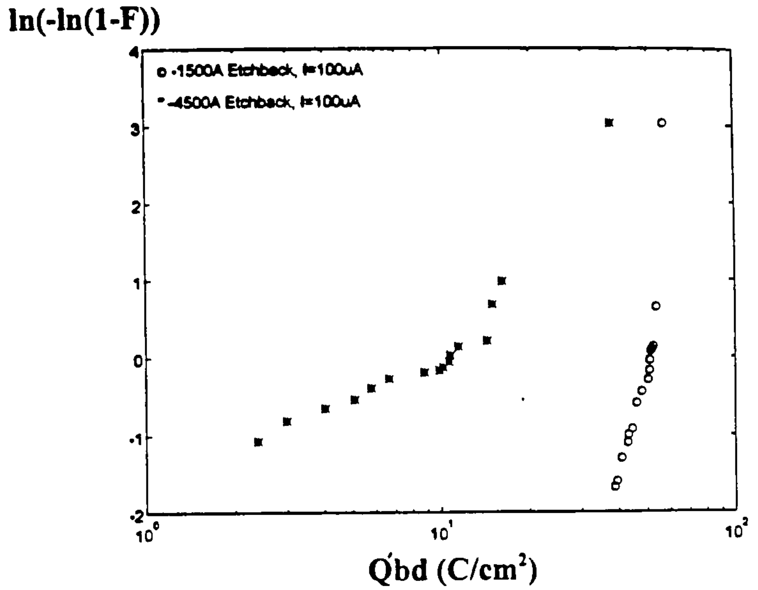
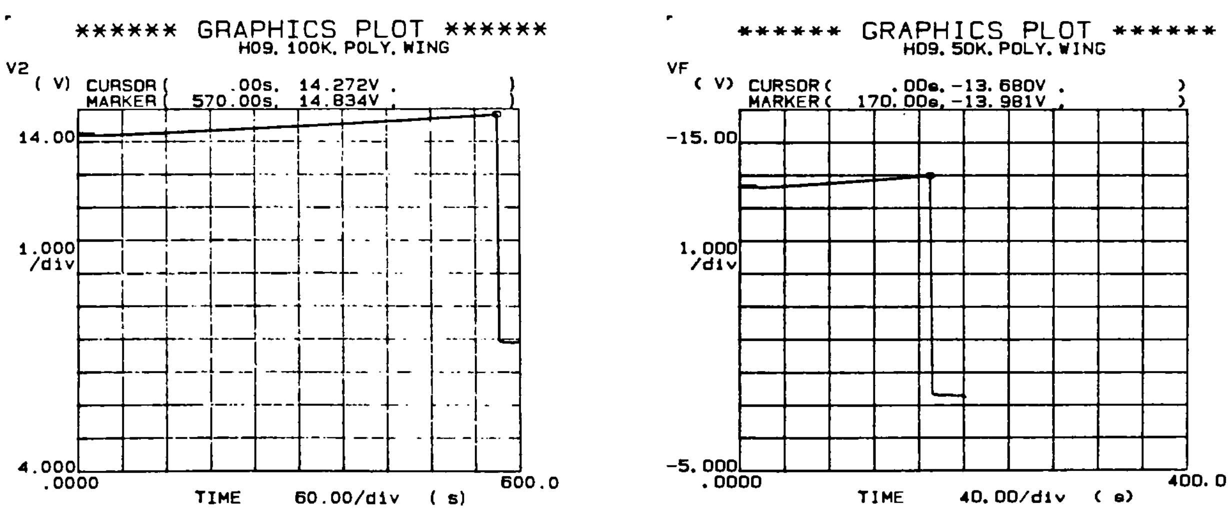


Fig. 4-14. Cumulative failure plots for P^{31} implanted, BOE etched, 100 $K\mu m^2$ samples from groups 1, and 4. The constant current stress level is 500 μA (.5 A/cm^2)

Compared to the unimplanted samples that possessed a 67% thinner tunnel oxide, the samples exhibited larger 50% failure time values, but smaller t_{BD} peak values. This trend has been observed in other studies.[26]

Gate Injection Effects

In all the TDDB tests, positive current stress (positive voltage applied to the gate), was applied to each sample. This would translate in to the electron injecting surface to be the silicon substrate. In applying a stress to a sample with a negative current, the gate electrode becomes the injecting surface. Fig 4-15a is a plot of a TDDB sample stressed with a positive I=100 μA. Fig. 4-15b shows the same constant current stress test on a different device but with a negative current, I= -100 μA. In comparing the two plots, the t_{BD} for the negative current (gate injecting) sample, was half as long as the positive current sample (substrate injecting). The reasons applied to the reduction in the t_{BD} is due to more interface traps being generated at the stacked gate/oxide interface.



(a) (b)

Fig 4-15. (a) Constant current stress plot of 100 Kμm² device, I= 100 μA

(b) Constant current stress plot of 50 Kμm² device, I= 100 μA

It can also be inferred that due to the thin films comprising the stacked gate, enhanced field may be forming which is aiding in the breakdown of the oxide.

Cascaded Breakdown

In Fig 4-16, the TDDB test result is shown of a device in which the breakdown characteristic was in the form of steps. This result has been termed a cascaded breakdown plot. Each step represents the breakdown of a weak area incorporated in the device which was tested. The reasons for this result could be attributed to the fact that the gate electrode could not provide enough into the oxide to produce a conductive path, which would result in the device shorting out. Thus another area within the device then continued with the conduction of the charges.

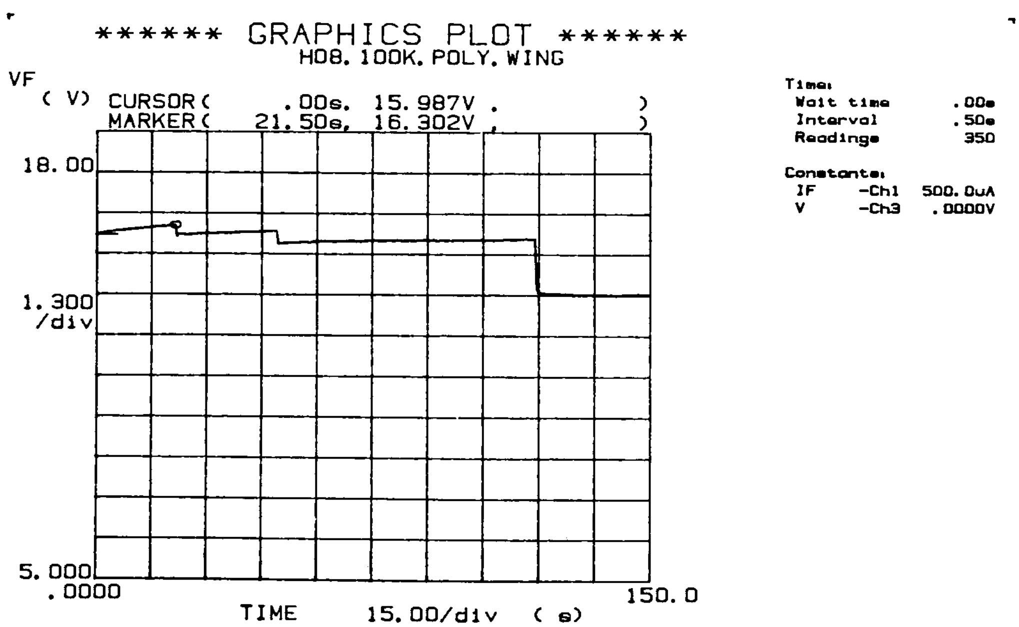


Fig. 4-16 Cascaded breakdown plot

5.0 CONCLUSIONS

This work found that the extent of the pre-tunnel oxide etch back does not significantly degrades the low level leakage on the tunnel oxide. However, from the constant stress tests, these oxide etch backs have a major impact on the long range endurance of the device. Approximately a five fold decrease in the time to 50% failure was observed when the etch back exceeded 1500 Å.

Samples etched in dilute BOE did not show any substantial difference in the tunnel oxide quality when compare to samples etched in HF.

The pre-tunnel oxide growth n^+ implanted samples resulted in a tunnel oxide of 157 Å. At any given oxide field value, these structures showed a higher leakage than the unimplanted samples. Their endurance under constant current stress were less than the non-implanted samples, although the implanted samples had large median breakdown times. Similarities between the two samples were the apparent lack of correlation to the oxide etch backs in regards to the low level oxide leakage. However, the oxide etch backs resulted in significantly less reliable structures as the TDDB shows.

6.0 References

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APPENDIX A

Process outline and Results

Processing Description

1.0 Scribe wafer

2.0 RCA clean wafers

3.0 Oxide growth for Back Implant

980 °C for 2 mins, dry O_2

4.0 Implant back side of wafers

P^{31}, dose: $1x10^{15}/cm^2$, energy: 110 KeV

5.0 Etch wafers

6.0 Pad oxide Growth

1100 °C for 15 mins., dry O_2

7.0 Nitride deposition

60 sccm Dichlorosilane

150 sccm Ammonia

Deposition time: 23 mins.

8.0 Nitride Removal from back of wafers

8.1. Standard WaferTrac coat program

8.2 Wafers inverted and placed in the RIE

SF_6, pressure: 90 mtorrs, power: 200 watts

9.0 Ash wafers

10.0 Clean wafers

Piranha Clean (3:1, H_2SO_4: H_2O_2) time: 10 mins.

11.0 Active area photolithography step

12.0 Patterning of Nitride

Wafers placed in the RIE

SF_6, pressure: 90 mtorrs, power: 200 watts

13.0 Ash wafers

14.0 Etch oxide

15.0 Piranha Clean

16.0 Field oxide growth (LOCOS formation)

Time: 210 mins.

Ambient: wet O_2

Temperature: 1100 °C

17.0 Nitride removal

SF_6, pressure: 90 mtorrs, power: 200 watts

18.0 Etch Pad oxide

BOE, 50 sec.

19.0 Kooi oxide growth

Temperature: 900 °C

Ambient: Wet O_2

Time: 45 mins.

20.0 First lot split

Implant half the lot

P^{31}, dose: 4×10^{15} /cm^2, energy: 120 KeV

21.0 Second lot split: divide lot for etch back (1500, 2500, 3500, 4500, 5500 Å)

22.0 Third lot split: divide lot to do etch back in either BOE or HF

23.0 Clean wafers

Piranha Clean: 10 mins. in solution

APM clean: 10 mins. in solution

24.0 Tunnel oxide growth

(see details in this Appendix)

25.0 Stacked gate formation

25.1 Amorphous silicon deposition

45% Silane flow

Temperature: 550 °C

Time: 100 mins.

REMOVE WAFERS

25.2 Polysilicon Deposition

45% Silane flow

Temperature: 610

Time: 50 mins.

26.0 Gate implantation

P^{31}, dose: $4x10^{15}$ /cm^2, energy: 50 KeV

27.0 Removal of gate material fro back of wafers

26.1. Coat wafers with thick layer of Photoresist

bake for two mins.

26.2 Emerse wafer in wet polysilicon etchant

27.0 Ash resist

28.0 Coat wafer with resist

29.0 Gate electrode photo step

30.0 Pattern the Gate electrode

RIE, SF_6; 30 sccm, O_2: 3 sccm

Pressure: 250 mtorr, Power: 200 watts

31.0 Etch oxide

32.0 Gate dopant drive-in

Temperature: 900 °C

Ambient: dry O_2

Time: 12 mins.

33.0 Coat wafer with photoresist

34.0 Poly contact cuts lithography

35.0 Etch polyoxide

Wet chemical etchant

36.0 Ash photoresist

37.0 Clean wafers

Piranha clean/APM solution

38.0 Sputter Al on wafers

39.0 Coat wafer with photoresist

40.0 Pattern Al

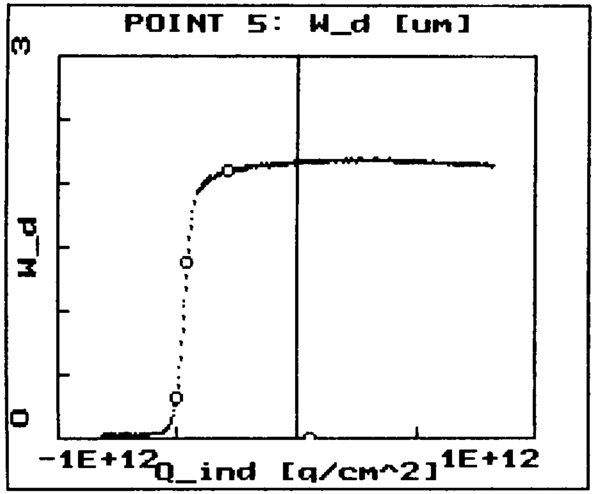
Use Al etchants

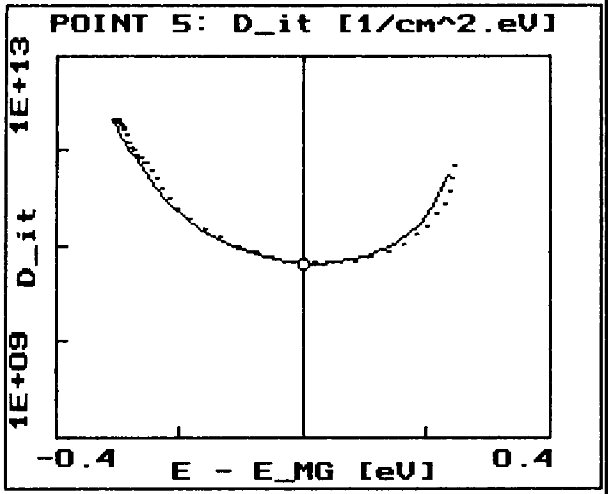
41.0 Ash resist

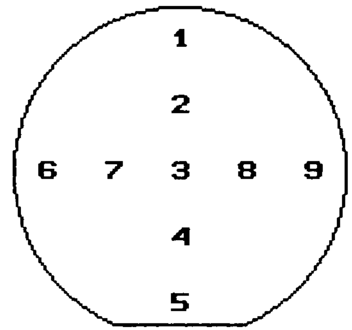
42.0 Sinter wafers

Temperature: 425 °C, time: 15 mins, Ambient: 10% H_2/ 90% N_2.

PRINTING SCREEN... REVIEW RESULTS 03/29/95 19:05:25







	5	4	3	2	1
Type :	N	N	N	N	N
Nsc_inv :	1.77E+14	1.76E+14	1.92E+14	1.71E+14	2.50E+14
Qox_inv :	-4.79E+11	-4.58E+11	-4.45E+11	-4.23E+11	-3.45E+11
DitMGinv:	6.48E+10	4.57E+10	4.11E+10	4.57E+10	6.97E+10
Qfb_inv :	-5.09E+11	-4.81E+11	-4.68E+11	-4.47E+11	-3.77E+11
Ts:	157	132	148	146	184

03/02/95 08:21:48
USER ID : ROHAN
TEST ID : 08800895
LOT ID : THESIS_N
CASSETTE: NONE
WAFER NO: BARE
PROGRAM : TUNNEL-N
PROBE NO: 2429
IND CHG : 8.2E+11
SWEEP : Inver.

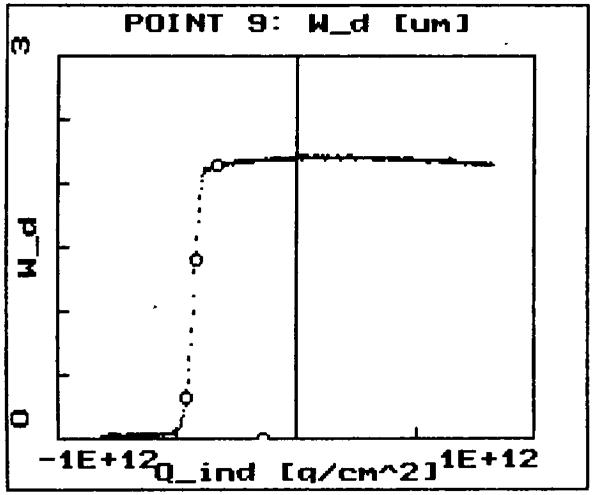
SCA0521088

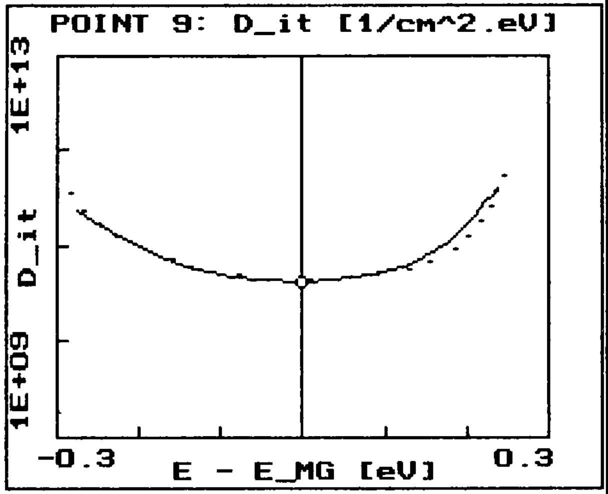
F1 PREVIOUS	=>F2<= NEXT	F3 ZOOM Wd	F4 ZOOM Dit	F5 ONSET	F6 PARM'S	F7 VIEW	F8

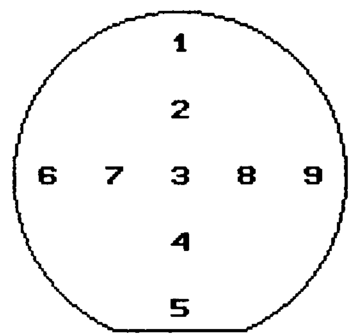
Display Next Test Point's Results <F9>Seri

SCA

PRINTING SCREEN... REVIEW RESULTS 03/29/95 19:09:57







	9	8	7	6	5
Type :	N	N	N	N	N
Nsc_inv :	1.70E+14	1.82E+14	1.83E+14	1.68E+14	1.77E+14
Qox_inv :	-4.44E+11	-4.52E+11	-4.37E+11	-4.33E+11	-4.79E+11
DitMGinv:	4.16E+10	4.43E+10	4.20E+10	4.69E+10	6.48E+10
Qfb_inv :	-4.65E+11	-4.75E+11	-4.60E+11	-4.55E+11	-5.09E+11
Ts:	142	141	144	139	157

03/02/95 08:21:48
USER ID : ROHAN
TEST ID : 08800895
LOT ID : THESIS_N
CASSETTE: NONE
WAFER NO: BARE
PROGRAM : TUNNEL-N
PROBE NO: 2429
IND CHG : 8.2E+11
SWEEP : Inver.

SCA0521088

F1 PREVIOUS	=>F2<= NEXT	F3 ZOOM Wd	F4 ZOOM Dit	F5 ONSET	F6 PARM'S	F7 VIEW	F9

Display Next Test Point's Results <F9>Seri

SCA

ROHAN'S THESIS DATA

NF	1.100	0.100	4.000	0.000	0.000	0.000
NS	4.050	0.000	0.000	0.007	0.000	0.000
CND	4.000	78.500	95.500	103.300	315.000	0.000
CND	4.000	78.500	95.500	103.300	315.000	

DEL1= 98.000023 PSI1= 78.500000
DEL2= 101.000000 PSI2= 76.699997

DEL= 99.387665 PSI= 77.660233

INDEX OF MEDIUM= 1.00000 ANGLE OF INCIDENCE= 70.000 WAVE LENGTH= 5461.0

THICK	NF REAL	KAPPA	ADSORPTION	D DEL	D PSI	ERROR	NF-NM
1147.6	1.47075	0.00000	1.0901E-02	0.001	0.000	-0.00082	0.47075

THE THICKNESS AT WHICH DEL & PSI REPEATS = 2413.4

OTHER FILM THICKNESSES ARE 3560.9 5974.3 8387.7 10801.0 13214.4 15627.7 180

PAGE	0.000	0.000	0.000	0.000	0.000	0.000

TUNNEL OXIDE GROWTH 2/26/95; FLAT TO THE RIGHT.

CD	31.400	13.900	120.600	166.300	315.000	0.000
CD	31.400	13.900	120.600	166.300	315.000	

DEL1= 152.800003 PSI1= 13.899995
DEL2= 151.199982 PSI2= 13.700007

DEL= 152.006027 PSI= 13.798751

INDEX OF MEDIUM= 1.00000 ANGLE OF INCIDENCE= 70.000 WAVE LENGTH= 5461.0

THICK	NF REAL	KAPPA	ADSORPTION	D DEL	D PSI	ERROR	NF-NM
286.9	1.10000	0.00000	6.3816E-04	-1.184	-0.544	29.43328	0.10000
162.9	1.20000	0.00000	7.0854E-04	-1.391	-0.778	22.94540	0.20000
123.2	1.30000	0.00000	7.8322E-04	-1.435	-0.874	19.23817	0.30000
104.1	1.40000	0.00000	8.5842E-04	-1.451	-0.938	17.32465	0.40000
93.3	1.50000	0.00000	9.3346E-04	-1.457	-0.991	16.32155	0.50000
86.7	1.60000	0.00000	1.0084E-03	-1.456	-1.042	15.85064	0.60000
82.4	1.70000	0.00000	1.0834E-03	-1.449	-1.092	15.73436	0.70000
79.7	1.80000	0.00000	1.1589E-03	-1.435	-1.144	15.88366	0.80000
78.1	1.90000	0.00000	1.2354E-03	-1.412	-1.200	16.25355	0.90000
77.3	2.00000	0.00000	1.3135E-03	-1.379	-1.261	16.82401	1.00000
77.1	2.10000	0.00000	1.3939E-03	-1.332	-1.326	17.59110	1.10000
77.4	2.20000	0.00000	1.4772E-03	-1.267	-1.399	18.56261	1.20000
78.2	2.30000	0.00000	1.5642E-03	-1.179	-1.478	19.75682	1.30000
79.4	2.40000	0.00000	1.6557E-03	-1.062	-1.567	21.20221	1.40000
81.0	2.50000	0.00000	1.7528E-03	-0.906	-1.664	22.93849	1.50000
83.0	2.60000	0.00000	1.8564E-03	-0.701	-1.772	25.01868	1.60000
85.5	2.70000	0.00000	1.9676E-03	-0.430	-1.893	27.51229	1.70000
88.3	2.80000	0.00000	2.0876E-03	-0.072	-2.025	30.51036	1.80000
91.6	2.90000	0.00000	2.2176E-03	0.398	-2.172	34.13163	1.90000
95.4	3.00000	0.00000	2.3589E-03	1.017	-2.331	38.53219	2.00000
99.7	3.10000	0.00000	2.5127E-03	1.831	-2.503	43.91846	2.10000
104.4	3.20000	0.00000	2.6798E-03	2.899	-2.684	50.56675	2.20000
109.7	3.30000	0.00000	2.8607E-03	4.294	-2.868	58.85250	2.30000
115.4	3.40000	0.00000	3.0547E-03	6.097	-3.041	69.29667	2.40000

121.4	3.50000	0.00000	3.2596E-03	8.388	-3.186	82.64845	2.50000
127.7	3.60000	0.00000	3.4699E-03	11.218	-3.275	100.04671	2.60000
133.6	3.70000	0.00000	3.6736E-03	14.576	-3.272	123.38573	2.70000
138.2	3.80000	0.00000	3.8423E-03	18.344	-3.137	156.31364	2.80000
138.4	3.90000	0.00000	3.8843E-03	22.275	-2.834	207.76567	2.90000
110.4	4.00000	0.00000	3.1288E-03	25.954	-2.346	311.34583	3.00000

```
CND          31.400    13.900   120.600   166.300   315.000     0.000
CND          31.400    13.900   120.600   166.300   315.000

DEL1=  152.800003 PSI1=    13.899995
DEL2=  151.199982 PSI2=    13.700007

 DEL=    152.006027 PSI=    13.798751

INDEX OF MEDIUM=    1.00000  ANGLE OF INCIDENCE=     70.000  WAVE LENGTH=   5461.0

   THICK   NF REAL     KAPPA  ADSORPTION     D DEL     D PSI       ERROR      NF-NM
PAGE           0.000     0.000     0.000     0.000     0.000     0.000
```

```
  TUNNEL ABOVE WITH REF. INDEX OF 1.46
NF             1.460     0.000     0.000     0.000     0.000     0.000
CD             0.000     0.000     0.000     0.000     0.000     0.000

INDEX OF MEDIUM=    1.00000  ANGLE OF INCIDENCE=    70.000  WAVE LENGTH=   5461.0

   THICK  NF REAL    KAPPA  ADSORPTION    D DEL     D PSI      ERROR     NF-NM

    97.0  1.46000  0.00000  9.0347E-04   -1.456    -0.971   16.64429    0.46000
PAGE           0.000     0.000     0.000     0.000     0.000     0.000
```

```
 TUNNEL OXIDE: SECOND READING, SAME WAFER, 90 DEGRESS ROTATION
CD            29.700   14.400  121.200  165.800  315.000    0.000
CD            29.700   14.400  121.200  165.800  315.000

DEL1=  149.400055 PSI1=   14.399996
DEL2=  152.399994 PSI2=   14.200005

 DEL=   150.889084 PSI=   14.295346

INDEX OF MEDIUM=   1.00000  ANGLE OF INCIDENCE=    70.000  WAVE LENGTH=   5461.0

   THICK  NF REAL    KAPPA  ADSORPTION    D DEL    D PSI      ERROR     NF-NM

   103.5  1.46000  0.00000  9.6372E-04   -2.040   -1.333   22.92147    0.46000
CND           29.700   14.400  121.200  165.800  315.000    0.000
CND           29.700   14.400  121.200  165.800  315.000

DEL1=  149.400055 PSI1=   14.399996
DEL2=  152.399994 PSI2=   14.200005

 DEL=   150.889084 PSI=   14.295346

INDEX OF MEDIUM=   1.00000  ANGLE OF INCIDENCE=    70.000  WAVE LENGTH=   5461.0

   THICK  NF REAL    KAPPA  ADSORPTION    D DEL    D PSI      ERROR     NF-NM
PAGE           0.000    0.000    0.000    0.000    0.000    0.000
```

TUNNEL OXIDE WITH THE ABOVE READING: NF=1.46

NF	1.460	0.000	0.000	0.000	0.000	0.000
CD	0.000	0.000	0.000	0.000	0.000	0.000

INDEX OF MEDIUM= 1.00000 ANGLE OF INCIDENCE= 70.000 WAVE LENGTH= 5461.0

THICK	NF REAL	KAPPA	ADSORPTION	D DEL	D PSI	ERROR	NF-NM
103.5	1.46000	0.00000	9.6372E-04	-2.040	-1.333	22.92147	0.46000

PAGE	0.000	0.000	0.000	0.000	0.000	0.000

```
  TUNNEL OXIDE: 180 DEGREES ROTATION (CLOCKWISE)
CND          31.100   14.000  122.100  166.000  315.000    0.000
CND          31.100   14.000  122.100  166.000  315.000

DEL1=  152.200043 PSI1=   13.999993
DEL2=  154.199997 PSI2=   14.000002

 DEL=   153.200027 PSI=   13.997950

INDEX OF MEDIUM=   1.00000  ANGLE OF INCIDENCE=    70.000  WAVE LENGTH=   5461.0

   THICK  NF REAL    KAPPA  ADSORPTION    D DEL    D PSI      ERROR      NF-NM
PAGE          0.000    0.000    0.000    0.000    0.000    0.000
```

```
  TUNNEL OXIDE WITH THE ABOVE READING: NF=1.46
NF            1.460     0.000     0.000     0.000     0.000     0.000            .
CD            0.000     0.000     0.000     0.000     0.000     0.000

INDEX OF MEDIUM=    1.00000  ANGLE OF INCIDENCE=    70.000  WAVE LENGTH=   5461.0

   THICK  NF REAL     KAPPA  ADSORPTION    D DEL    D PSI      ERROR      NF-NM

    93.7  1.46000  0.00000  8.7263E-04   -1.767   -1.236   21.02149    0.46000
PAGE          0.000     0.000     0.000     0.000     0.000     0.000
```

TUNNEL OXIDE: 270 DEGREES ROTATION (CLOCKWISE)

CND	29.600	14.200	121.400	166.100	315.000	0.000
CND	29.600	14.200	121.400	166.100	315.000	

DEL1= 149.200012 PSI1= 14.199998
DEL2= 152.799988 PSI2= 13.899994

DEL= 150.979980 PSI= 14.043437

INDEX OF MEDIUM= 1.00000 ANGLE OF INCIDENCE= 70.000 WAVE LENGTH= 5461.0

THICK	NF REAL	KAPPA	ADSORPTION	D DEL	D PSI	ERROR	NF-NM
PAGE	0.000	0.000	0.000	0.000	0.000	0.000	

```
  TUNNEL OXIDE WITH THE ABOVE READINGS: NF=1.46
NF            1.460    0.000    0.000    0.000    0.000    0.000
CD            0.000    0.000    0.000    0.000    0.000    0.000

INDEX OF MEDIUM=   1.00000  ANGLE OF INCIDENCE=    70.000  WAVE LENGTH=   5461.0

   THICK  NF REAL    KAPPA  ADSORPTION    D DEL     D PSI      ERROR      NF-NM

   101.9  1.46000  0.00000  9.4891E-04   -1.715    -1.115    19.19331     0.46000
PAGE          0.000    0.000    0.000    0.000    0.000    0.000
```

```
  BELOW ARE THE READING FOR THE TUNNEL OXIDE OVER DIFFUSION: FLAT RIGHT
CND          23.900   15.700  114.100  164.900  315.000    0.000
CND          23.900   15.700  114.100  164.900  315.000

DEL1=  137.799988 PSI1=   15.699994
DEL2=  138.199997 PSI2=   15.100017

 DEL=   137.995895 PSI=   15.400351

INDEX OF MEDIUM=   1.00000  ANGLE OF INCIDENCE=    70.000  WAVE LENGTH=   5461.0

   THICK  NF REAL    KAPPA  ADSORPTION    D DEL    D PSI      ERROR     NF-NM
PAGE          0.000    0.000    0.000    0.000    0.000    0.000
```

ABOVE READINGS WITH NF=1.46

NF	1.460	0.000	0.000	0.000	0.000	0.000
CD	0.000	0.000	0.000	0.000	0.000	0.000

INDEX OF MEDIUM= 1.00000 ANGLE OF INCIDENCE= 70.000 WAVE LENGTH= 5461.0

THICK	NF REAL	KAPPA	ADSORPTION	D DEL	D PSI	ERROR	NF-NM
158.1	1.46000	0.00000	1.4725E-03	-2.215	-1.076	20.11470	0.46000

PAGE	0.000	0.000	0.000	0.000	0.000	0.000

```
  90 DEGREES CLOCKWISE ROTATION
CND         22.200   16.000  113.500  165.200  315.000    0.000
CND         22.200   16.000  113.500  165.200  315.000

DEL1=  134.400024 PSI1=   15.999996
DEL2=  137.000015 PSI2=   14.800008

 DEL=   135.646851 PSI=   15.397964

INDEX OF MEDIUM=   1.00000  ANGLE OF INCIDENCE=    70.000  WAVE LENGTH=   5461.0

   THICK  NF REAL     KAPPA  ADSORPTION    D DEL     D PSI       ERROR     NF-NM
PAGE         0.000     0.000     0.000     0.000     0.000     0.000
```

ABOVE READINGS WITH NF=1.46

NF	1.460	0.000	0.000	0.000	0.000	0.000
CD	0.000	0.000	0.000	0.000	0.000	0.000

INDEX OF MEDIUM= 1.00000 ANGLE OF INCIDENCE= 70.000 WAVE LENGTH= 5461.0

THICK	NF REAL	KAPPA	ADSORPTION	D DEL	D PSI	ERROR	NF-NM
167.0	1.46000	0.00000	1.5552E-03	-1.772	-0.820	15.62939	0.46000

PAGE	0.000	0.000	0.000	0.000	0.000	0.000

```
  180 DEGREES CLOCKWISE ROTATION
CND          21.800    15.500  113.100  164.700  315.000     0.000
CND          21.800    15.500  113.100  164.700  315.000

DEL1=  133.599960 PSI1=   15.499998
DEL2=  136.199982 PSI2=   15.300007

 DEL=   134.891113 PSI=   15.396276

INDEX OF MEDIUM=   1.00000  ANGLE OF INCIDENCE=    70.000  WAVE LENGTH=   5461.0

   THICK  NF REAL    KAPPA  ADSORPTION    D DEL     D PSI      ERROR     NF-NM
PAGE          0.000    0.000    0.000    0.000    0.000    0.000
```

ABOVE READINGS WITH NF=1.46

NF	1.460	0.000	0.000	0.000	0.000	0.000
CD	0.000	0.000	0.000	0.000	0.000	0.000

INDEX OF MEDIUM= 1.00000 ANGLE OF INCIDENCE= 70.000 WAVE LENGTH= 5461.0

THICK	NF REAL	KAPPA	ADSORPTION	D DEL	D PSI	ERROR	NF-NM
169.9	1.46000	0.00000	1.5817E-03	-1.614	-0.735	14.11056	0.46000

PAGE	0.000	0.000	0.000	0.000	0.000	0.000

270 DEGREES CLOCKWISE ROTATION

CND	22.500	15.800	113.500	164.800	315.000	0.000
CND	22.500	15.800	113.500	164.800	315.000	

DEL1= 134.999985 PSI1= 15.799996
DEL2= 137.000015 PSI2= 15.199997

DEL= 135.979675 PSI= 15.498186

INDEX OF MEDIUM= 1.00000 ANGLE OF INCIDENCE= 70.000 WAVE LENGTH= 5461.0

THICK	NF REAL	KAPPA	ADSORPTION	D DEL	D PSI	ERROR	NF-NM
PAGE	0.000	0.000	0.000	0.000	0.000	0.000	

```
  ABOVE READINGS WITH NF=1.46
NF             1.460     0.000     0.000     0.000     0.000     0.000
CD             0.000     0.000     0.000     0.000     0.000     0.000

INDEX OF MEDIUM=    1.00000  ANGLE OF INCIDENCE=     70.000  WAVE LENGTH=   5461.0

   THICK  NF REAL    KAPPA  ADSORPTION    D DEL     D PSI      ERROR      NF-NM

   166.5  1.46000  0.00000  1.5505E-03   -1.999    -0.935    17.75843    0.46000
STOP           0.000     0.000     0.000     0.000     0.000     0.000
```

Tunnel Oxide Processing Steps for RIT.

	Furnace Settings	Temperature (degC)	Gas flow(LPM)
Wafer Load: 650 C			
	Load: 527	645	N_2: 8.5
	Center: 229	649	
	Source: 509	655	

Stabilization time 650 C: 10min.

	Furnace Settings	Temperature (degC)	Gas flow(LPM)
Ramp to 950 C			
	Load: 527	645	N_2: 8.5
	Center: 229	649	O_2: 3 sccm
	Source: 509	655	

Ramp Time: 21min.

	Furnace Settings	Temperature (degC)	Gas flow(LPM)
First Oxidation			
	Load: 529	950.5	N_2: 8.5
	Center: 535	949.4	O_2: 2.0
	Source: 510	950.3	

First oxidation time: 10min.

Ramp from 950 C to 1050 C in 100% Nitrogen

	Furnace Settings	Temperature (degC)	Gas flow(LPM)
First Anneal			
	Load: 528	1050.4	N_2: 8.5
	Center: 635	1050.0	
	Source: 507	1050.3	

Anneal time: 30min.

Ramp down to 950 C in 100% Nitrogen

	Furnace Settings	Temperature (degC)	Gas flow(LPM)
Second Oxidation:			
	Load: 526	950.2	N_2: 8.5
	Center: 538	950.2	O_2: 2.0
	Source: 507	949.9	

Oxidation time: 14min.

Second Anneal performed at 950C for 30 mins. 100% Nitrogen.
Ramp down to 650C in 100% Nitrogen, and then pull wafers.

Wafer Clean Processing Steps

1. Piranha Clean (H_2SO_4: DI water; 3:1)............. 10 mins.

2. DI rinse .... 5mins.

3. HPM .... 10 mins.

4. DI rinse .... 5mins.

5. 50:1 DI: HF .... 1 min.

6. DI rinse .... 5mins.

7. Rinse and Spin Dry in the SRD using Program 1.

N.B.

Check to make sure that your wafers are dry completely!

APPENDIX B

Dielectric Breakdown Calculations

Dielectric Strength calculations

Rs=3.7 KΩ

I= 100 μA

Vseries=.370 V

Assume $N_d=10^{15}/cm^3$

$\phi_F=26\ mV[\ln(10^{15}/10^{10})]$

=.3 V

$E_c-E_f=.56-.299=.26$ V

Assume $10^{18}/cm^3$, gate doping at the tunnel oxide interface

$\phi_f=.179$ V

$2\phi_F+8\phi_t=.567$ V

Non implanted group:

Vox2=14.3-[.3+.26+.567+.370]

Vox2=12.8

Dielectric Strength:

12.8/94 Å=**13.6 MV/cm**

Implanted Group

Vox2=14.992-[1.85+.567]

Vox2=14.992-2.417 V

Vox2=12.575 V

Dielectric Strength:

12.575/94 Å=8 MV/cm

APPENDIX C

Simulation Results

```
         ****************************************************
         ***               TMA SUPREM-3 (TM)              ***
         ***                 Version 6.0.0                ***
         ***            System C (DEC VAX: VMS)           ***
         ***            Copyright (C) 1985-1993           ***
         ***      Technology Modeling Associates, Inc.    ***
         ***              All Rights Reserved             ***
         ****************************************************

                        25-MAY-95 04:33:10


   Statements input from file TOX.SUP


  1... TITLE SIMULATION OF A TWO-STEP TUNNEL OXIDE GROWTH
  2... COM  ROHAN S. BRAITHWAITE
  3... COM  OCTOBER 19TH, 1994
  4... COM
  5... INITIALIZE SILICON <100> PHOSPHOROUS=1E15 THICKNESS=.1 DX=.001
  6... COM
  7... COM OXIDE GROWTH
  8... COM
  9... COM
 10... DIFFUSION TIME=10 TEMPERATURE=650 F.N2=9.0 F.O2=.1
 11... DIFFUSION TIME=28.75 TEMPERATURE=650 F.N2=9.0 F.O2=.1 T.RATE=16
 12... DIFFUSION TIME=10 TEMPERATURE=950 F.N2=7 F.O2=3
 13... DIFFUSION TIME=12.5 TEMPERATURE=950 INERT T.RATE=16
 14... DIFFUSION TIME=30 TEMPERATURE=1050 INERT
 15... DIFFUSION TIME=25 TEMPERATURE=1050 INERT T.RATE=-8
 16... COM
 17... EXTRACT NAME=XOX1 THICKNESS LAYER=2
 18... COM
 19... PLOT NET ACTIVE TITLE="OXIDE THICKNESS- FIRST STEP" BOTTOM=1E10 TOP=1E16
   ... + DEVICE="HP7550" PLOT.OUT="TOX1.OUT"
 20... LABEL LABEL="OXIDE THICKNESS FIRST STEP:"@XOX1" MICRONS"
 21... LABEL LABEL="10 MINS. @950 degC IN 5 SLPM AR + 2 SLPM O2"
 22... LABEL LABEL="30 MIN ANNEAL: 100% AR"
 23... COM
 24... COM SECOND STEP OF TUNNEL OXIDE GROWTH
 25... COM
 26... DIFFUSION TIME=14 TEMPERATURE=950 F.N2=7 F.O2=3
 27... DIFFUSION TIME=30 TEMPERATURE=950 INERT
 28... DIFFUSION TIME=37.5 TEMPERATURE=950 INERT T.RATE=-8
 29... COM
 30... EXTRACT NAME=XOX2 THICKNESS LAYER=2
 31... COM
 32... PLOT NET ACTIVE TITLE="TUNNEL OXIDE FINAL THICKNESS" BOTTOM=1E10 TOP=1E16
   ... + DEVICE="HP7550" PLOT.OUT="TOX2.OUT"
 33... LABEL LABEL="FINAL THICKNESS:"@XOX2" MICRONS"
 34... LABEL LABEL="INITIAL THICKNESS:"@XOX1" MICRONS"
 35... LABEL LABEL="24 MINS. GROWTH @950 IN 5 SLPM AR + 2 SLPM O2"
 36... LABEL LABEL="ANNEAL @950 FOR 1HR. IN 100% AR"
 37... COM
 38... COM PLOYSILICON DEPOSITION
 39... DEPOSITION POLYSILICON TEMPERATURE=610 PRESSURE=5.04E-04 THICKNESS=.54
```

```
 40... COM
 41... COM IMPLANTATION OF THE POLYSILICON
 42... IMPLANT DOSE=4E15 ENERGY=50 PHOSPHOROUS
 43... COM
 44... COM ACTIVATION OF IMPLANT
 45... DIFFUSION TIME=10 TEMPERATURE=650 F.N2=5 F.O2=3
 46... DIFFUSION TIME=20 TEMPERATURE=650 F.N2=5 F.O2=3 T.RATE=12
 47... DIFFUSION TIME=12 TEMPERATURE=900 DRYO2
 48... DIFFUSION TIME=31 TEMPERATURE=900 T.RATE=-8
 49... COM
 50... COM PRINT OUT OF THE DIFFERENT LAYERS
 51... PLOT NET ACTIVE TITLE="N+ DOPANT ACTIVATION PROFILE" BOTTOM=1E14
   ... + TOP=1E20 DEVICE="REGIS"
 52... PLOT ACTIVE PHOSPHOROUS LINE=2 COLOR=2 ADD
 53... EXTRACT NAME=POX THICKNESS LAYER=4
 54... EXTRACT NAME=PTHX THICKNESS LAYER=3
 55... EXTRACT NAME=THXT THICKNESS LAYER=2
 56... ELECTRICAL STEPS=1
 57... BIAS LAYER=3 V=0
 58... END
 59... EXTRACT NAME=RS1 E.RESIST LAYER=3 MIN.REGI=1 MAX.REGI=1
 60... LABEL LABEL="CAP OXIDE ON POLY="@POX" MICRONS"
 61... LABEL LABEL="POLYSILICON THICKNESS="@PTHX" MICRONS"
 62... LABEL LABEL="TUNNEL OXIDE THICKNESS="@THXT" MICRONS"
 63... LABEL LABEL="POLYSILICON SHEET RESISTANCE="@RS1" OHMS/SQR" PAUSE
 64... PRINT LAYERS CONCENTRATION PHOSPHOROUS ACTIVE LAYER=3 X.MAX=.54
 65... PRINT LAYERS CONCENTRATION PHOSPHOROUS ACTIVE LAYER=2 X.MAX=.0108
 66... STOP

Input line #   5
Coefficient data group read
File: LIB$DISK:[ACCLIB.TMA.SUPREM_6_0_0.LIBRARY]S3COF0.DAT
Date: 14-SEP-93 11:01:19
Documentation from data file:

S-3 Rev 6.0 Release Version Default Coefficients
s3init,v 1.1 93/02/25 10:57:04 lynetteq Exp $


Warning number   45 detected in line number  10
The temperature specified was less than 800 degrees Celsius.
The default diffusion and oxidation coefficients are not reliable
below this temperature.

Warning number   45 detected in line number  11
The temperature specified was less than 800 degrees Celsius.
The default diffusion and oxidation coefficients are not reliable
below this temperature.

Warning number  441 detected in line number  13
A non-negligible impurity flux was detected at the bottom of the
simulation regime.  A thicker simulation regime may be advisable.

Warning number   47 detected in line number  28
The temperature will ramp to a temperature of less than 800 degrees Celsius.
The default diffusion and oxidation coefficients are not reliable
below this temperature.

Warning number  527 detected in line number  45
During the present high-temperature step the implantation-damage
```

```
(used in the POINT.DE model) is regarded as having been annealed out.
The interstitial concentration has been set to its equilibrium value.

Warning number   45 detected in line number  45
The temperature specified was less than 800 degrees Celsius.
The default diffusion and oxidation coefficients are not reliable
below this temperature.

Warning number   45 detected in line number  46
The temperature specified was less than 800 degrees Celsius.
The default diffusion and oxidation coefficients are not reliable
below this temperature.

Warning number   47 detected in line number  48
The temperature will ramp to a temperature of less than 800 degrees Celsius.
The default diffusion and oxidation coefficients are not reliable
below this temperature.
```

SIMULATION OF A TWO-STEP TUNNEL OXIDE GROWTH
PRINT OUT OF THE DIFFERENT LAYERS

Electrical information
Input line # 58

Bias step 1

layer no.	region no.	type	Conductor Bias (volts)	Electron Bias (volts)	Hole Bias (volts)
3	1	n		0.0000E+00	0.0000E+00
1	1	n		0.0000E+00	0.0000E+00

Electron Charge, Conductance, and Resistance

layer no.	region no.	type	Electron Charge (#/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
3	1	n	3.695E+15	3.9150E-02	2.5543E+01	1.9927E+06	5.0183E-07
1	1	n	7.042E+10	1.4511E-05	6.8913E+04	6.7502E+04	1.4814E-05

Hole Charge, Conductance, and Resistance

layer no.	region no.	type	Hole Charge (#/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
3	1	n	0.000E+00	0.0000E+00		0.0000E+00	
1	1	n	0.000E+00	0.0000E+00		0.0000E+00	

SIMULATION OF A TWO-STEP TUNNEL OXIDE GROWTH
PRINT OUT OF THE DIFFERENT LAYERS

Material layer information
Input line # 64

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
4	oxide	0.0114	0.0100	0.00	841	842	
3	polysilicon	0.5350	0.0100	0.00	843	897	0.3251
2	oxide	0.0087	0.0100	0.00	898	901	
1	silicon	0.0962	0.0010	0.00	902	1000	<100>

Polysilicon Ratios of Chemical Interior Grain to Total Concentrations

layer no.	phosphorus
3	9.2872E-01

Integrated Dopant (#/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
4	4.3007E+12	4.3007E+12	4.3007E+12	4.3007E+12
3	3.9786E+15	3.9786E+15	3.9786E+15	3.9786E+15
2	1.4371E+09	1.4371E+09	1.4371E+09	1.4371E+09
1	9.9919E+09	9.9919E+09	9.9919E+09	9.9919E+09
sum	3.9829E+15	3.9829E+15	3.9829E+15	3.9829E+15

Integrated Dopant (#/cm**2)

layer	phosphorus	
no.	active	chemical
4	4.3007E+12	4.3007E+12
3	3.9786E+15	3.9786E+15
2	1.4371E+09	1.4371E+09
1	9.9919E+09	9.9919E+09
sum	3.9829E+15	3.9829E+15

Boundary Locations and Integrated Dopant
Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (#/cm**2)	sum chemical Qd (#/cm**2)
4	1	n	0.0000	0.0114	4.3007E+12	4.3007E+12
3	1	n	0.0000	0.5350	3.9786E+15	3.9786E+15
2	1	n	0.0000	0.0087	1.4371E+09	1.4371E+09
1	1	n	0.0000	0.0962	9.9919E+09	9.9919E+09

SIMULATION OF A TWO-STEP TUNNEL OXIDE GROWTH
PRINT OUT OF THE DIFFERENT LAYERS

Concentration information
Input line # 64

layer 3 depth (microns)	active phosphorus (#/cm**3)	layer 3 depth (microns)	active phosphorus (#/cm**3)
0.0000	2.24153E+20	0.2750	3.42399E+19
0.0050	2.24001E+20	0.2850	2.97201E+19
0.0150	2.22844E+20	0.2950	2.56549E+19
0.0250	2.20572E+20	0.3050	2.20232E+19
0.0350	2.17225E+20	0.3150	1.88005E+19
0.0450	2.12861E+20	0.3250	1.59598E+19
0.0550	2.07552E+20	0.3350	1.34725E+19
0.0650	2.01383E+20	0.3450	1.13092E+19
0.0750	1.94447E+20	0.3550	9.44001E+18
0.0850	1.86844E+20	0.3650	7.83563E+18
0.0950	1.78677E+20	0.3750	6.46760E+18
0.1050	1.70048E+20	0.3850	5.30876E+18
0.1150	1.61061E+20	0.3950	4.33356E+18
0.1250	1.51818E+20	0.4050	3.51829E+18
0.1350	1.42416E+20	0.4150	2.84124E+18
0.1450	1.32949E+20	0.4250	2.28276E+18
0.1550	1.23505E+20	0.4350	1.82531E+18
0.1650	1.14168E+20	0.4450	1.45336E+18
0.1750	1.05012E+20	0.4550	1.15338E+18
0.1850	9.61060E+19	0.4650	9.13731E+17
0.1950	8.75098E+19	0.4750	7.24508E+17
0.2050	7.92748E+19	0.4850	5.77461E+17
0.2150	7.14438E+19	0.4950	4.65855E+17
0.2250	6.40505E+19	0.5050	3.84353E+17
0.2350	5.71200E+19	0.5150	3.28918E+17
0.2450	5.06688E+19	0.5250	2.96728E+17
0.2550	4.47055E+19	0.5350	2.86112E+17
0.2650	3.92311E+19		

SIMULATION OF A TWO-STEP TUNNEL OXIDE GROWTH
PRINT OUT OF THE DIFFERENT LAYERS

Material layer information
Input line # 65

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
4	oxide	0.0114	0.0100	0.00	841	842	
3	polysilicon	0.5350	0.0100	0.00	843	897	0.3251
2	oxide	0.0087	0.0100	0.00	898	901	
1	silicon	0.0962	0.0010	0.00	902	1000	<100>

Polysilicon Ratios of Chemical Interior Grain to Total Concentrations

layer no.	phosphorus
3	9.2872E-01

Integrated Dopant (#/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
4	4.3007E+12	4.3007E+12	4.3007E+12	4.3007E+12
3	3.9786E+15	3.9786E+15	3.9786E+15	3.9786E+15
2	1.4371E+09	1.4371E+09	1.4371E+09	1.4371E+09
1	9.9919E+09	9.9919E+09	9.9919E+09	9.9919E+09
sum	3.9829E+15	3.9829E+15	3.9829E+15	3.9829E+15

Integrated Dopant (#/cm**2)

layer	phosphorus	
no.	active	chemical
4	4.3007E+12	4.3007E+12
3	3.9786E+15	3.9786E+15
2	1.4371E+09	1.4371E+09
1	9.9919E+09	9.9919E+09
sum	3.9829E+15	3.9829E+15

Boundary Locations and Integrated Dopant
Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (#/cm**2)	sum chemical Qd (#/cm**2)
4	1	n	0.0000	0.0114	4.3007E+12	4.3007E+12
3	1	n	0.0000	0.5350	3.9786E+15	3.9786E+15
2	1	n	0.0000	0.0087	1.4371E+09	1.4371E+09
1	1	n	0.0000	0.0962	9.9919E+09	9.9919E+09

```
SIMULATION OF A TWO-STEP TUNNEL OXIDE GROWTH
PRINT OUT OF THE DIFFERENT LAYERS

Concentration information
Input line #  65

   layer  2      active
    depth      phosphorus
  (microns)    (#/cm**3)
    0.0000   9.53707E+15
    0.0030   8.26647E+12
    0.0066   1.73421E+12
    0.0087   3.25844E+11


*** END SUPREM-3 ***


TOTAL CPU TIME =     0.05 minutes
```

```
$ 10 MICRON CAPACITOR W/100 ANGSTROM OXIDE
$
$
$
$
$ Mask data file "tma_rohan.tl1"
$
$
$
MASK      IN.FILE=tma_rohan.tl1 PRINT
$
$ Set Display to X-windows
OPTION DEVICE=X
$
$ Set up grid and initialize structure
$
$
LINE      X LOCATION=0 SPACING=0.1
LINE      X LOCATION=1 SPACING=0.05
LINE      X LOCATION=2 SPACING=0.05
LINE      X LOCATION=3 SPACING=0.05
$
$ SET INITIAL Y GRID SPACING
$
LINE      Y LOCATION=0 SPACING=0.1
LINE      Y LOCATION=1 SPACING=0.1
LINE      Y LOCATION=2 SPACING=0.1
LINE      Y LOCATION=2.5 SPACING=1.0
$
$
$
%DEFINE gf 1.0
MESH      GRID.FAC=@gf
$
$ Start of Processing
$ Substrate wafer N-type,<100>, 5-15 Ohm-cm (10 Ohm-cm used)
$
INITIALIZE RATIO=1.5 <100> ROT.SUB=0.0 PHOSPHOR=1e15
$
$
SELECT    TITLE="TUNNEL OXIDE CAPACITOR: INITIAL GRID FOR DEVICE"
PLOT.2D   X.MIN=0 X.MAX=3 Y.MIN=0 Y.MAX=2.5 SCALE ^CLEAR X.SIZE=0.25 +
Y.SIZE=0.25 X.OFFSET=5.0 Y.OFFSET=5.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1 +
GRID L.GRID=1 C.GRID=1
$
$
$
$
$ STEP 1   GROW PAD OXIDE (DRYO2)
$
$       (START SOAK AT 1090 C)
$
METHOD VERTICAL INIT=0.2
DIFFUSION TIME=4 TEMPERAT=900 INERT
DIFFUSION TIME=9.5 TEMPERAT=900 T.FINAL=1090 INERT
DIFFUSION TIME=.5 TEMPERAT=1090 T.FINAL=1100 DRYO2
DIFFUSION TIME=14.5 TEMPERAT=1100 DRYO2
DIFFUSION TIME=10 TEMPERAT=1100 T.FINAL=1000 INERT
DIFFUSION TIME=4 TEMPERAT=1000 INERT
EXTRACT  X=1 OXIDE AREA.EXT NAME=PAD
```

```
$
$
$
$ STEP 2  CV02 CVD NITRIDE
$
DEPOSITION NITRIDE THICKNES=.15 SPACES=4
DIFFUSION TIME=28 TEMPERAT=800 inert
$
$ STEP 3  PH03 PHOTOLITH  (NITRIDE & OXIDE ETCH)
$
DEPOSITION PHOTORES POSITIVE THICKNES=1.05 SPACES=2
EXPOSE    MASK=NITRIDE
DEVELOP
$
$
$ STEP 4  ET09 NITRIDE  (PRE-FIELD)
$
ETCH  NITRIDE  TRAPEZOI
$
$
$ STEP 5  ET06 OXIDE ETCH
$
ETCH    OXIDE   TRAPEZOI
$
$
$ STEP 6  ET07 STRIP
$
ETCH    PHOTORES  ALL
$
$
$
$ STEP 7 OX04 WET OXIDE  (FIELD OXIDE)
$
$       (START SOAK AT 1090 C)
$
METHOD  VISCOUS  GRID.OXI=4 INIT=0.2
DIFFUSION TIME=4 TEMPERAT=900 DRYO2
DIFFUSION TIME=9.5 TEMPERAT=900 T.FINAL=1090 DRYO2
DIFFUSION TIME=.5 TEMPERAT=1090 T.FINAL=1100 WETO2
DIFFUSION TIME=209.5 TEMPERAT=1100 WETO2
DIFFUSION TIME=10 TEMPERAT=1100 T.FINAL=1000 INERT
DIFFUSION TIME=4 TEMPERAT=1000 INERT
$
$
$ CALCULATE THE STRESS IN THE SILICON SUBSTRATE
$
METHOD  ^SKIP.SIL
DIFFUSION TIME=1E-6  TEMP=1100  WETO2
$
$
SELECT  TITLE="INDUCED STRESS FROM LOCOS"
PLOT.2D  X.OFFSET=5 SCALE  STRESS  VLENG=0.35  X.MIN=0  +
   X.MAX=3 Y.MAX=2.5 C.COMPRE=4  C.TENSIO=2  L.TENSIO=2
$
$
METHOD    SKIP.SIL
SELECT    Z=log10(PHOS) TITLE="AFTER FIELD OXIDE GROWTH"
PLOT.2D   X.OFFSET=8.0 X.MIN=0 X.MAX=3 Y.MAX=2.5 SCALE CLEAR T.SIZE=0.4 +
 L.BOUND=1 C.BOUND=1
COLOR     COLOR=3 NITRIDE
```

```
COLOR     COLOR=5 OXIDE
LABEL     LABEL=NITRIDE ^CM X=0.5 Y=1.5 COLOR=3 LEFT SIZE=0.25 RECTANGL +
 C.RECTAN=3 W.RECTAN=.5 H.RECTAN=.5
LABEL     LABEL=OXIDE ^CM X=0.5 Y=2.0 COLOR=5 LEFT SIZE=0.25 RECTANGL C.RECTAN=5
 W.RECTAN=.5 H.RECTAN=.5
$
$ STEP 8  ET09 NITRIDE (POST FIELD NITRIDE ETCH)
$
ETCH    NITRIDE   ALL
$
$
$ STEP 9 ET06 OXIDE ETCH
$
ETCH    OXIDE  TRAPEZOI  THICKNES=@PAD
$
$
$ STEP 10  OX04 WET OXIDE  (KOOI OXIDE)
$
METHOD  VISCOUS  GRID.OXI=4  INIT=0.2
DIFFUSION TIME=4 TEMPERAT=900 INERT
DIFFUSION TIME=45 TEMPERAT=900 WETO2
DIFFUSION TIME=4 TEMPERAT=900 INERT
$
$
$ CALCULATE STRESS IN SUBSTRATE
METHOD  ^SKIP.SIL
DIFFUSION TIME=1E-6 TEMP=900 WETO2
$
SELECT    Z=log10(PHOS) TITLE="AFTER KOOI OXIDE GROWTH"
PLOT.2D   X.OFFSET=8.0 X.MIN=0 X.MAX=3 Y.MAX=2.5 SCALE CLEAR T.SIZE=0.4 +
 L.BOUND=1 C.BOUND=1
COLOR     COLOR=5 OXIDE
LABEL     LABEL=OXIDE ^CM X=5 Y=3 COLOR=5 LEFT SIZE=0.25 RECTANGL C.RECTAN=5 +
 W.RECTAN=.5 H.RECTAN=.5
$
$
$
$ STEP 11 ETCH KOOI OXIDE
$ (IN STEPS OF 0.15, 0.25, 0.35, 0.45, AND 0.55 microns)
$
ETCH  OXIDE  TRAPEZOI  THICKNES=0.15
$
$
SELECT  TITLE="PRESSURE CONTOURS AFTER 1500A ETCH"
$
$ (CHANGE TITLE FOR DIFFERENT ETCHBACKS)
$
PLOT.2D  SCALE X.MIN=0  X.MAX=6 Y.MAX=2.5 X.OFFSET=3 Y.OFFSET=4
COLOR    NITRIDE   COLOR=3
SELECT   Z=(-0.5*(SXX+SYY))
CONTOUR  VALUE=5e4 LINE=1 COLOR=10
CONTOUR  VALUE=1e5 LINE=2 COLOR=11
CONTOUR  VALUE=5e5 LINE=3 COLOR=12
CONTOUR  VALUE=1e6 LINE=4 COLOR=13
CONTOUR  VALUE=5e6 LINE=5 COLOR=14
CONTOUR  VALUE=1e7 LINE=6 COLOR=15
CONTOUR  VALUE=5e7 LINE=7 COLOR=16
CONTOUR  VALUE=1e8 LINE=8 COLOR=17
CONTOUR  VALUE=5e8 LINE=9 COLOR=18
CONTOUR  VALUE=1e9 LINE=10 COLOR=19
```

```
PLOT.2D  ^AX  ^CL
SELECT   Z=Y
PRINT.1D  SILICON /OXIDE
$
METHOD  SKIP.SIL
LABEL X=5   Y=-0.55 LABEL="5e4"  LINE.TYP=1 C.LINE=10 LENGTH=1.0
LABEL X=5   Y=-0.25 LABEL="1e5"  LINE.TYP=2 C.LINE=11 LENGTH=1.0
LABEL X=5   Y=0.05  LABEL="5e5"  LINE.TYP=3 C.LINE=12 LENGTH=1.0
LABEL X=5   Y=0.35  LABEL="1e6"  LINE.TYP=4 C.LINE=13 LENGTH=1.0
LABEL X=5   Y=0.65  LABEL="5e6"  LINE.TYP=5 C.LINE=14 LENGTH=1.0
LABEL X=5   Y=0.95  LABEL="1e7"  LINE.TYP=6 C.LINE=15 LENGTH=1.0
LABEL X=5   Y=1.25  LABEL="5e7"  LINE.TYP=7 C.LINE=16 LENGTH=1.0
LABEL X=5   Y=1.55  LABEL="1e8"  LINE.TYP=8 C.LINE=17 LENGTH=1.0
LABEL X=5   Y=1.85  LABEL="5e8"  LINE.TYP=9 C.LINE=18 LENGTH=1.0
LABEL X=5   Y=2.15  LABEL="1e9"  LINE.TYP=10 C.LINE=19 LENGTH=1.0
$
$
$
$
$
SELECT    Z=log10(BORON) TITLE="AFTER 1500A ETCH"
$
$ (CHANGE TITLE FOR DIFFERENT ETCHBACKS)
$
PLOT.2D   X.OFFSET=7.0 X.MIN=0 X.MAX=3 Y.MAX=2.5 SCALE CLEAR +
  T.SIZE=0.4 L.BOUND=1 C.BOUND=1
COLOR     COLOR=5 OXIDE
LABEL     LABEL=OXIDE ^CM X=0.5 Y=2.0 COLOR=5 LEFT SIZE=0.25 RECTANGL C.RECTAN=5
 W.RECTAN=.5 H.RECTAN=.5
$
$ (SAVEFILE WILL BE CHANGED FOR DIFFERENT ETCHBACKS)
$
SAVEFILE  OUT.FILE=RO15ETCH
$
$ STEP 12  GROW TUNNEL OXIDE
$
$
$ STEP 13   DRY OXIDE GROWTH  (TUNNEL OXIDE)
$
$       (START SOAK AT 650 C)
$
METHOD  VISCOUS  GRID.OXI=4 INIT=0.2
DIFFUSION TIME=15 TEMPERAT=650 F.N2=0.99 F.O2=0.01
DIFFUSION TIME=15 TEMPERAT=650 T.FINAL=950 F.N2=0.99 F.O2=0.01
DIFFUSION TIME=10 TEMPERAT=950 F.N2=0.714 F.O2=0.286
DIFFUSION TIME=5 TEMPERAT=950 T.FINAL=1050 INERT
DIFFUSION TIME=30 TEMPERAT=1050 INERT
DIFFUSION TIME=10 TEMPERAT=1050 T.FINAL=950 INERT
DIFFUSION TIME=14 TEMPERAT=950 F.N2=0.714 F.O2=0.286
DIFFUSION TIME=30 TEMPERAT=950 INERT
DIFFUSION TIME=30 TEMPERAT=950 T.FINAL=650 INERT
EXTRACT X=0.25 OXIDE AREA.EXT NAME=TNOX
EXTRACT   X=0.65 OXIDE AREA.EXT NAME=TOX
$
$
$ CALCULATE THE STRESS IN THE SILICON SUBSTRATE AFTER TUNNEL OX GROWTH
$
METHOD  ^SKIP.SIL
DIFFUSION TIME=1E-6  TEMP=1050  WETO2
$
```

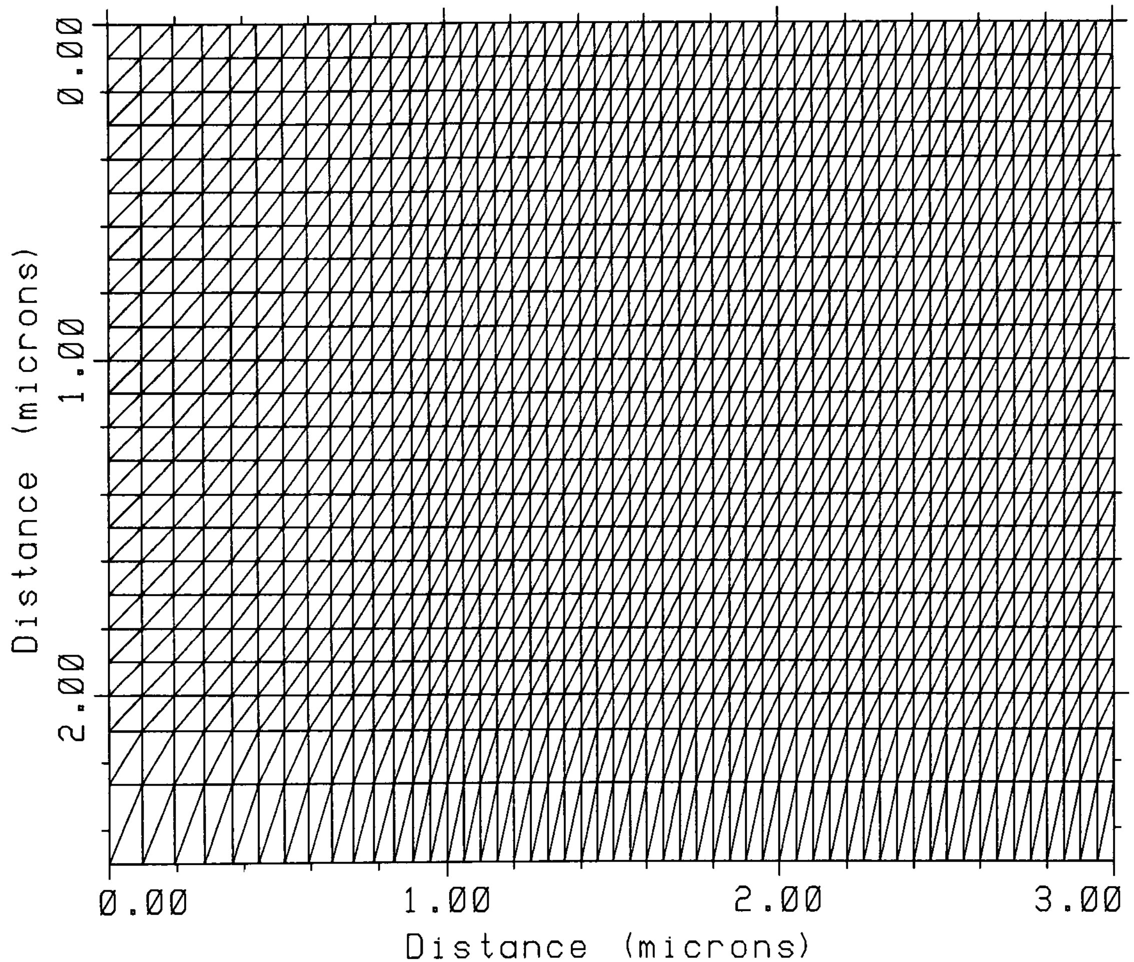
```
$ (SAVEFILE WILL BE CHANGED FOR DIFFERENT ETCHBACKS)
SAVEFILE        OUT.FILE=RO15TOX
$
$
SELECT  TITLE="STRESS AFTER TUNNEL-OX GROWTH"
PLOT.2D  SCALE  X.OFFSET=5 STRESS  VLENG=0.35  X.MIN=0  X.MAX=3 Y.MAX=2.5 +
  C.COMPRE=4  C.TENSIO=2  L.TENSIO=2
$
$
SELECT  TITLE="PRESSURE CONTOURS AFTER TUNNEL-OX GROWTH"
PLOT.2D  SCALE  X.MIN=0  X.MAX=7 Y.MAX=2.5 X.OFFSET=2.5 Y.OFFSET=3
COLOR    NITRIDE   COLOR=3
SELECT   Z=(-0.5*(SXX+SYY))
CONTOUR  VALUE=5e4 LINE=1 COLOR=10
CONTOUR  VALUE=1e5 LINE=2 COLOR=11
CONTOUR  VALUE=5e5 LINE=3 COLOR=12
CONTOUR  VALUE=1e6 LINE=4 COLOR=13
CONTOUR  VALUE=5e6 LINE=5 COLOR=14
CONTOUR  VALUE=1e7 LINE=6 COLOR=15
CONTOUR  VALUE=5e7 LINE=7 COLOR=16
CONTOUR  VALUE=1e8 LINE=8 COLOR=17
CONTOUR  VALUE=5e8 LINE=9 COLOR=18
CONTOUR  VALUE=1e9 LINE=10 COLOR=19
PLOT.2D  ^AX  ^CL
SELECT   Z=Y
PRINT.1D  SILICON /OXIDE
$
METHOD  SKIP.SIL
LABEL X=4   Y=-0.55 LABEL="5e4"  LINE.TYP=1 C.LINE=10 LENGTH=1.0
LABEL X=4   Y=-0.25 LABEL="1e5"  LINE.TYP=2 C.LINE=11 LENGTH=1.0
LABEL X=4   Y=0.05  LABEL="5e5"  LINE.TYP=3 C.LINE=12 LENGTH=1.0
LABEL X=4   Y=0.35  LABEL="1e6"  LINE.TYP=4 C.LINE=13 LENGTH=1.0
LABEL X=4   Y=0.65  LABEL="5e6"  LINE.TYP=5 C.LINE=14 LENGTH=1.0
LABEL X=4   Y=0.95  LABEL="1e7"  LINE.TYP=6 C.LINE=15 LENGTH=1.0
LABEL X=4   Y=1.25  LABEL="5e7"  LINE.TYP=7 C.LINE=16 LENGTH=1.0
LABEL X=4   Y=1.55  LABEL="1e8"  LINE.TYP=8 C.LINE=17 LENGTH=1.0
LABEL X=4   Y=1.85  LABEL="5e8"  LINE.TYP=9 C.LINE=18 LENGTH=1.0
LABEL X=4   Y=2.15  LABEL="1e9"  LINE.TYP=10 C.LINE=19 LENGTH=1.0
LABEL X=5  Y=0    LABEL="OXIDE THICKNESS"
LABEL X=5  Y=0.4  LABEL="AT X=0.25"
LABEL X=5  Y=0.8  LABEL="IS @TNOX microns"
LABEL X=5  Y=1.3  LABEL="OXIDE THICKNESS"
LABEL X=5  Y=1.7  LABEL="AT X=0.65"
LABEL X=5  Y=2.1  LABEL=" IS @TOX microns"
$
$
$
$ STEP 14   CV01 CVD POLY (AMORPHOUS & POLY)
$
DEPOSITION POLYSILI THICKNES=0.2 SPACES=4
$
DIFFUSION TIME=100 TEMPERAT=550 INERT
$
$
$
DEPOSITION POLYSILI THICKNES=0.425 SPACES=8
$
DIFFUSION TIME=50 TEMPERAT=610 INERT
$
$
```

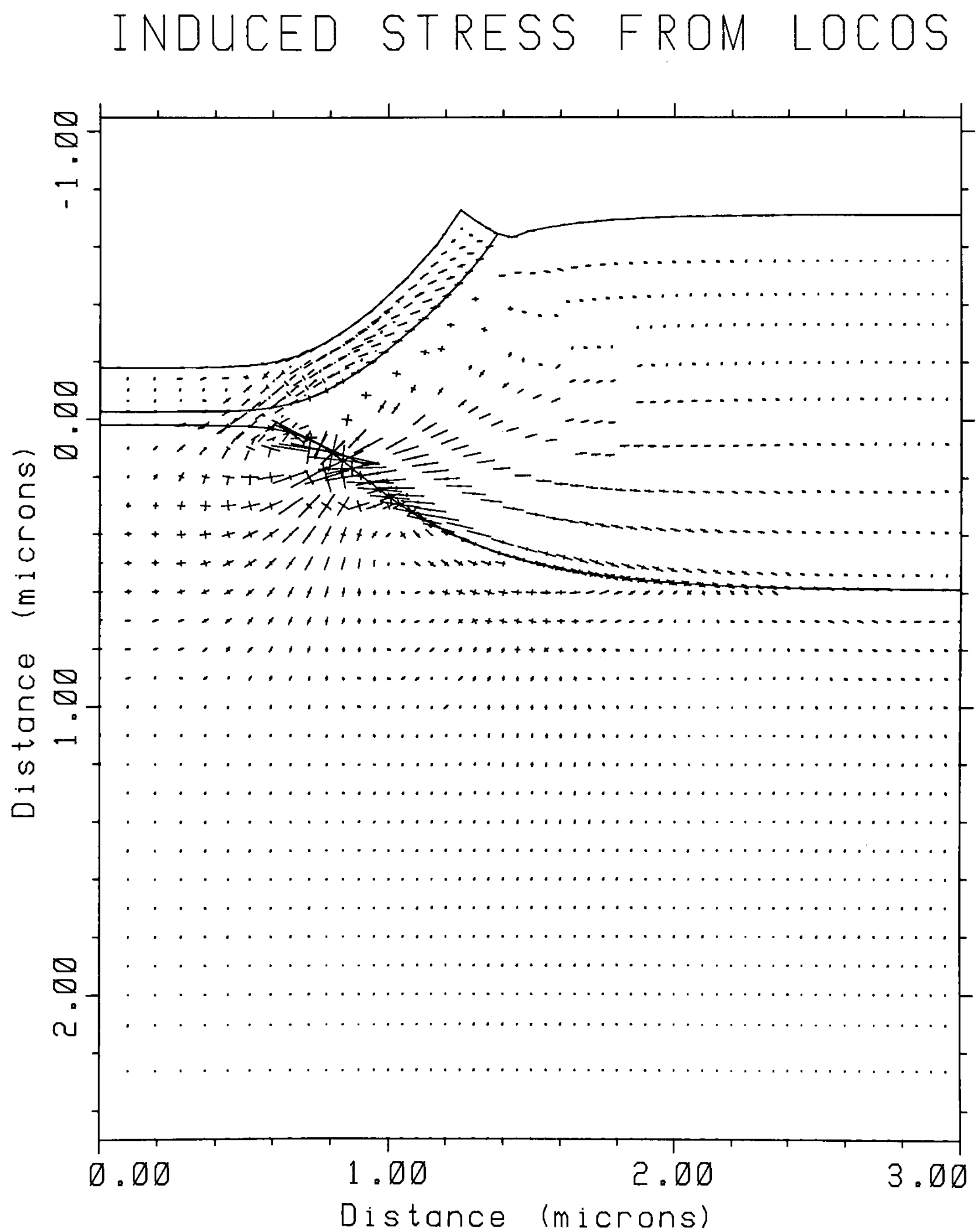
```
$
$ STEP 15   IM01 IMPLANT  (PHOSPHOROUS DOPANT)
$
IMPLANT   PHOSPHOROUS DOSE=5e15 ENERGY=50 GAUSSIAN
$
DIFFUSION TIME=14 TEMPERAT=650 INERT
DIFFUSION TIME=12.5 TEMPERAT=650 T.FINAL=900 INERT
DIFFUSION TIME=11 TEMPERAT=900 INERT
DIFFUSION TIME=25 TEMPERAT=900 T.FINAL=650 INERT
DIFFUSION TIME=4 TEMPERAT=650 INERT
$
$
SELECT   Z=Log10(PHOS) TITLE="AFTER PHOSPHOROUS IMPLANT"
PLOT.2D  X.MIN=0 X.MAX=6 Y.MAX=2.5 X.OFFSET=3 Y.OFFSET=4 SCALE CLEAR
COLOR    COLOR=2  POLYSILICON
COLOR    COLOR=5  OXIDE
FOREACH  X(15)
CONTOUR  VALUE=15 LINE.TYP=8 COLOR=1
END
FOREACH  X(16 TO 20 STEP 1)
CONTOUR  VALUE=X LINE.TYP=2 COLOR=1
END
LABEL    LABEL=OXIDE ^CM X=4 Y=-1.0 COLOR=5 LEFT SIZE=0.25 RECTANGL +
 C.RECTAN=5 W.RECTAN=0.5 H.RECTAN=0.5
LABEL    LABEL=POLYSILICON ^CM X=4 Y=-0.5 COLOR=2 LEFT SIZE=0.25 RECTANGL +
 C.RECTAN=2 W.RECTAN=0.5 H.RECTAN=0.5
LABEL    LABEL="PHOSPHOROUS CONTOURS" ^CM X=4 Y=0 COLOR=1 +
 LEFT SIZE=0.25 LINE.TYP=5 C.LINE=1 LENGTH=1.0
LABEL    LABEL=" 1e15 - 1e20" ^CM X=4 Y=0.5 COLOR=1 LEFT SIZE=0.25
LABEL    LABEL="TUNNEL OXIDE THICKNESS" ^CM X=4  Y=1 COLOR=1 +
 LEFT SIZE=0.25
LABEL    LABEL="= @TNOX microns"  ^CM X=4 Y=1.5 COLOR=1 +
 LEFT SIZE=0.25
$
$
$
$ STEP 16   PH03 PHOTOLITH (PATTERN POLY CAPACITOR)
$
DEPOSITION PHOTORES POSITIVE THICKNES=1.05 SPACES=2
EXPOSE    MASK=POLY
DEVELOP
$
$
$ STEP 17 ETCH POLY
$
ETCH POLYSILI TRAPEZOI
$
$ STEP 18 ETCH OXIDE
$
$ ETCH OXIDE TRAPEZOI
$
$ STEP 19   ET07 STRIP
$
ETCH    PHOTORES   ALL
$
$
SELECT    Z=log10(PHOS) TITLE="FINAL STRUCTURE"
PLOT.2D   X.MIN=0 X.MAX=6 Y.MAX=2.5 X.OFFSET=3 Y.OFFSET=4 SCALE CLEAR
COLOR     COLOR=2 POLYSILI
COLOR     COLOR=5 OXIDE
```

```
FOREACH    X(15)
CONTOUR    VALUE=15 LINE.TYP=8 COLOR=1
END
FOREACH    X(16 TO 20 STEP 1)
CONTOUR    VALUE=X LINE.TYP=2
END
LABEL      LABEL=POLYSILICON ^CM X=4 Y=-1.0 COLOR=1 LEFT SIZE=0.25 RECTANGL +
 C.RECTAN=2 W.RECTAN=.5 H.RECTAN=.5
LABEL      LABEL=OXIDE ^CM X=4 Y=-0.5 COLOR=1 LEFT SIZE=0.25 RECTANGL C.RECTAN=5
 W.RECTAN=.5 H.RECTAN=.5
LABEL      LABEL="PHOSPHOROUS CONTOURS: 1e15 - 1e20" ^CM X=4 Y=0 +
 COLOR=1 LEFT SIZE=0.25 LINE.TYP=5 C.LINE=1 LENGTH=1.0
$
$
$  (SAVEFILE WILL BE CHANGED FOR DIFFERENT ETCHBACKS)
$
SAVEFILE  OUT.FILE=RO15FIN
STOP
```

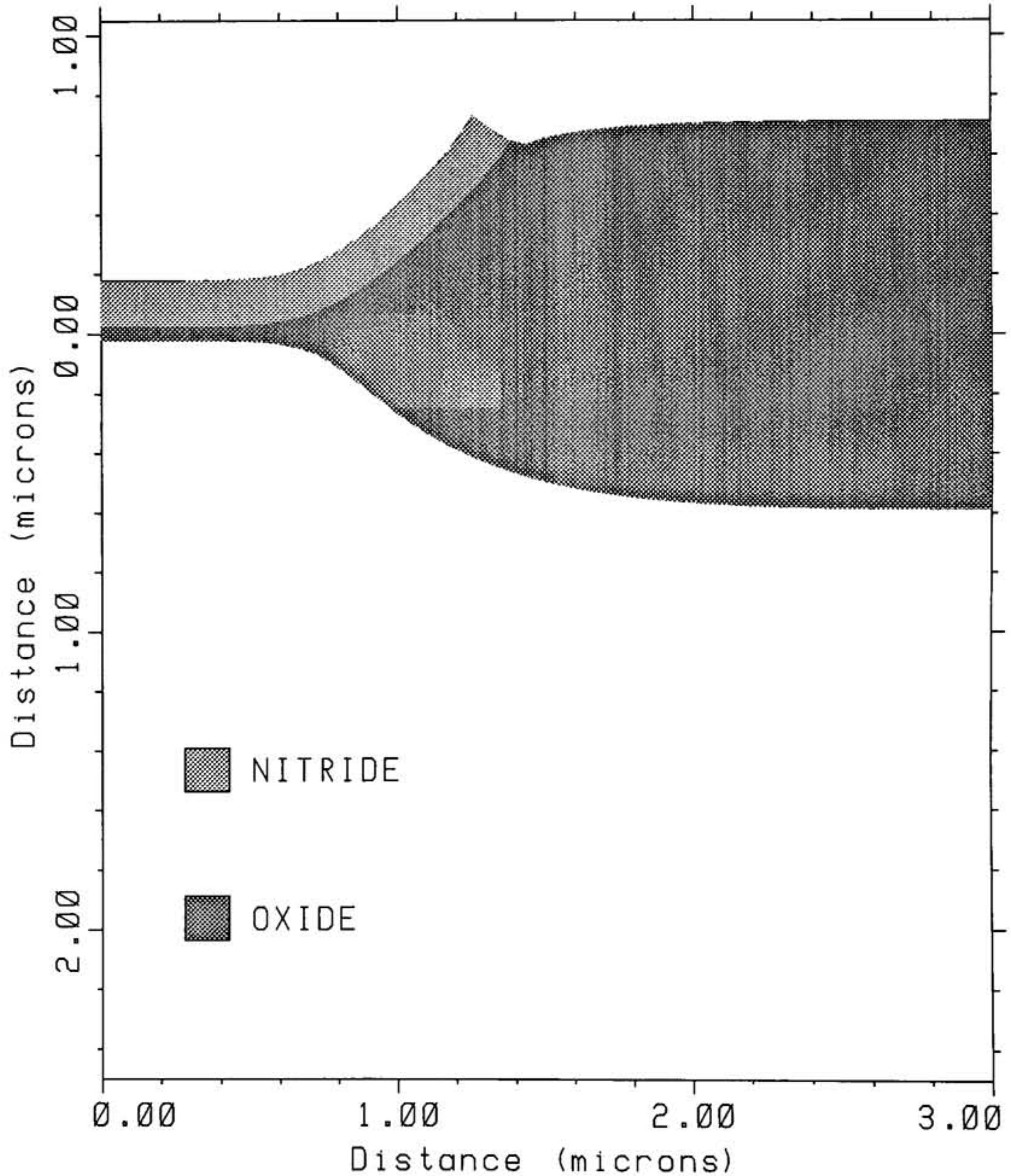
1500 Å Etch Back Results

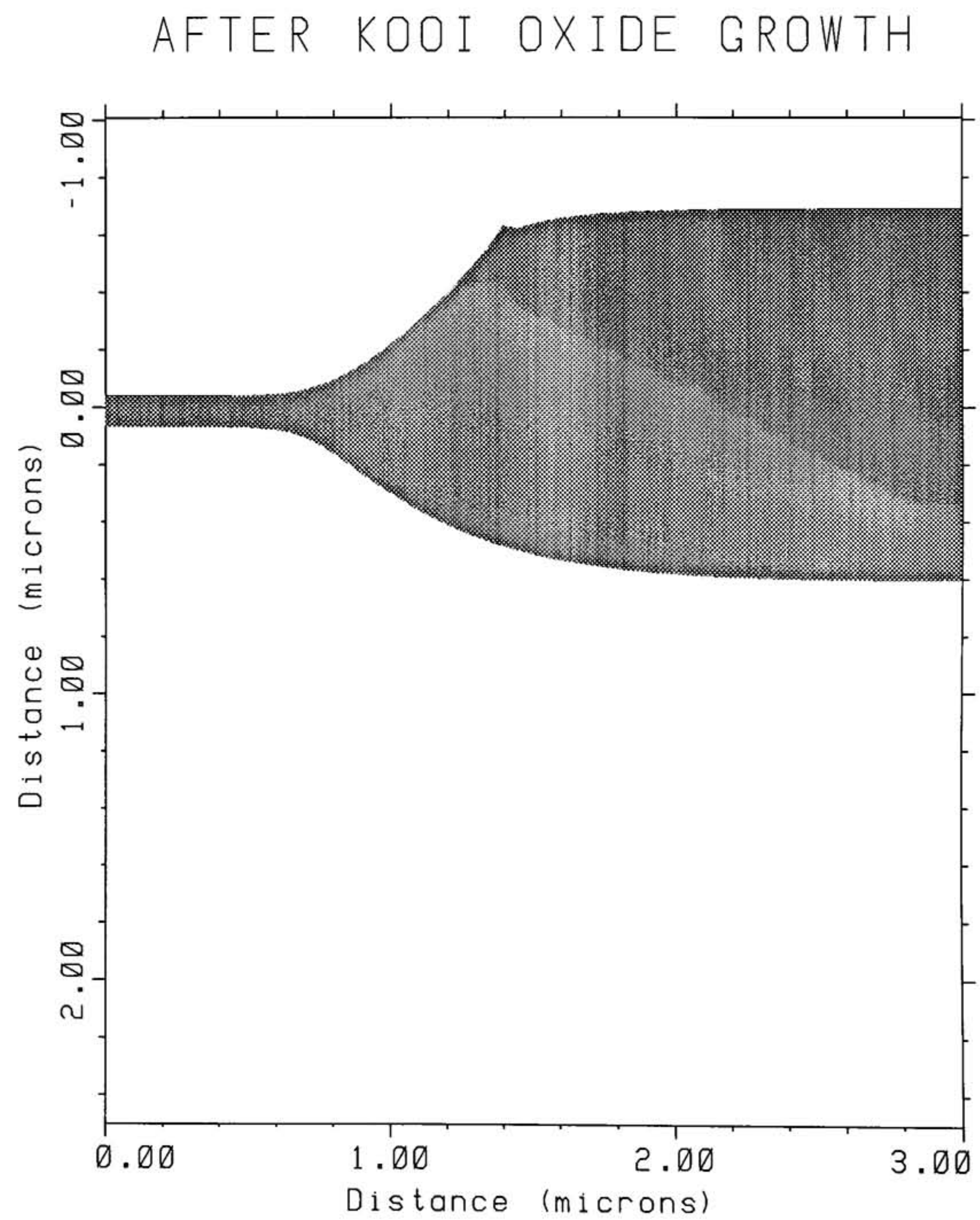
TUNNEL OXIDE CAPACITOR: INITIAL GRID FOR DEVICE



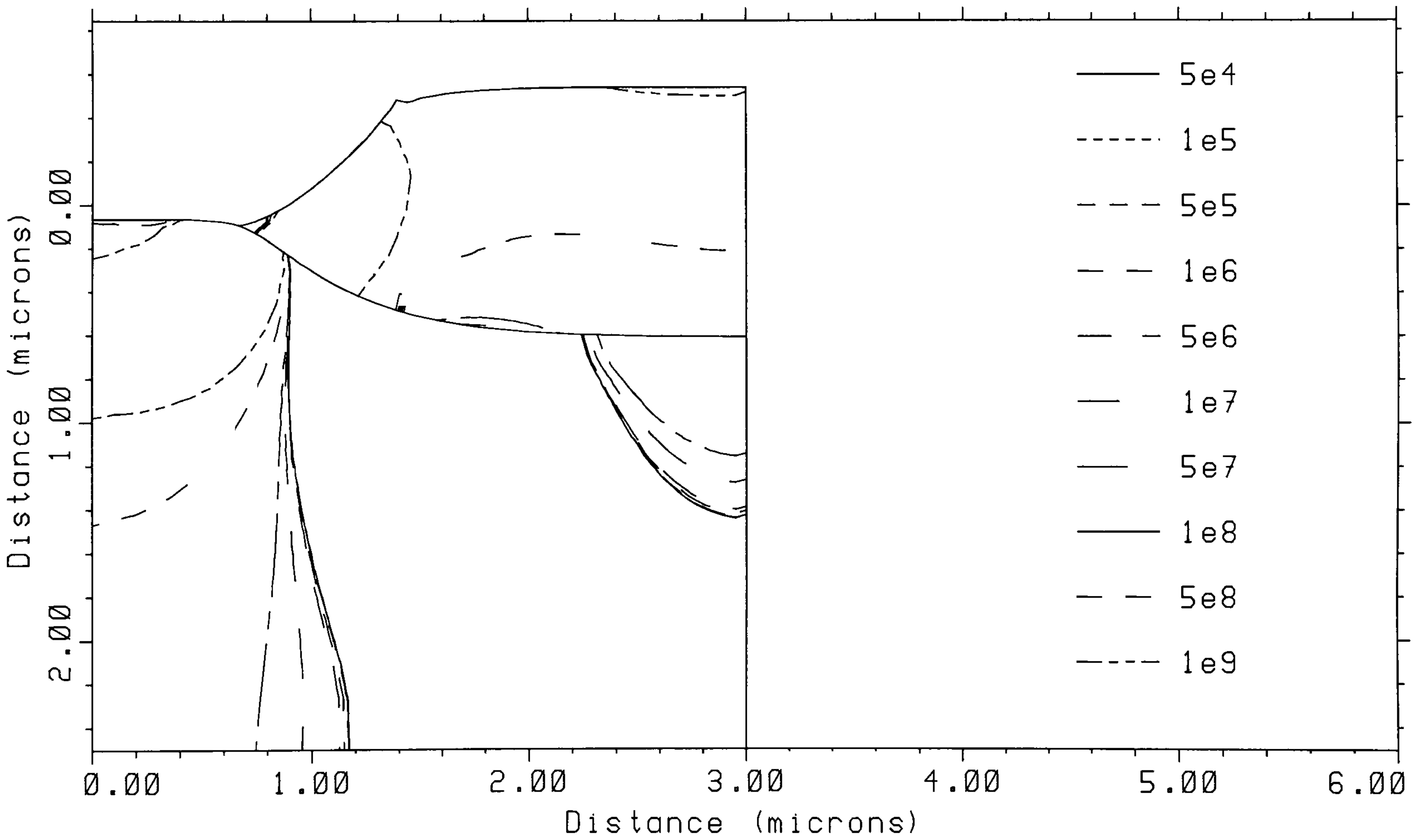

INDUCED STRESS FROM LOCOS
-1.00
0.00
1.00
2.00
Distance (microns)
0.00
1.00
2.00
3.00
Distance (microns)

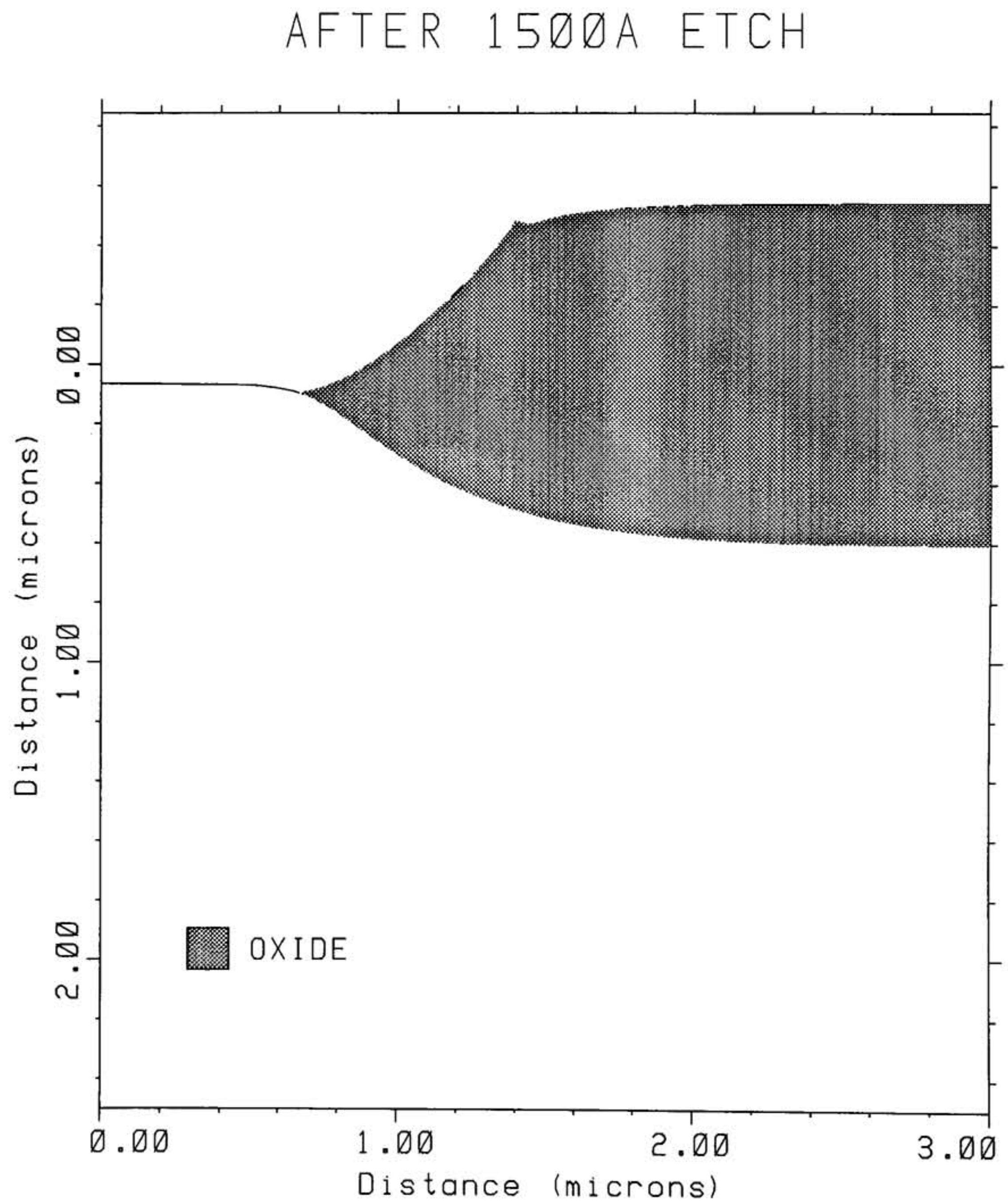
AFTER FIELD OXIDE GROWTH

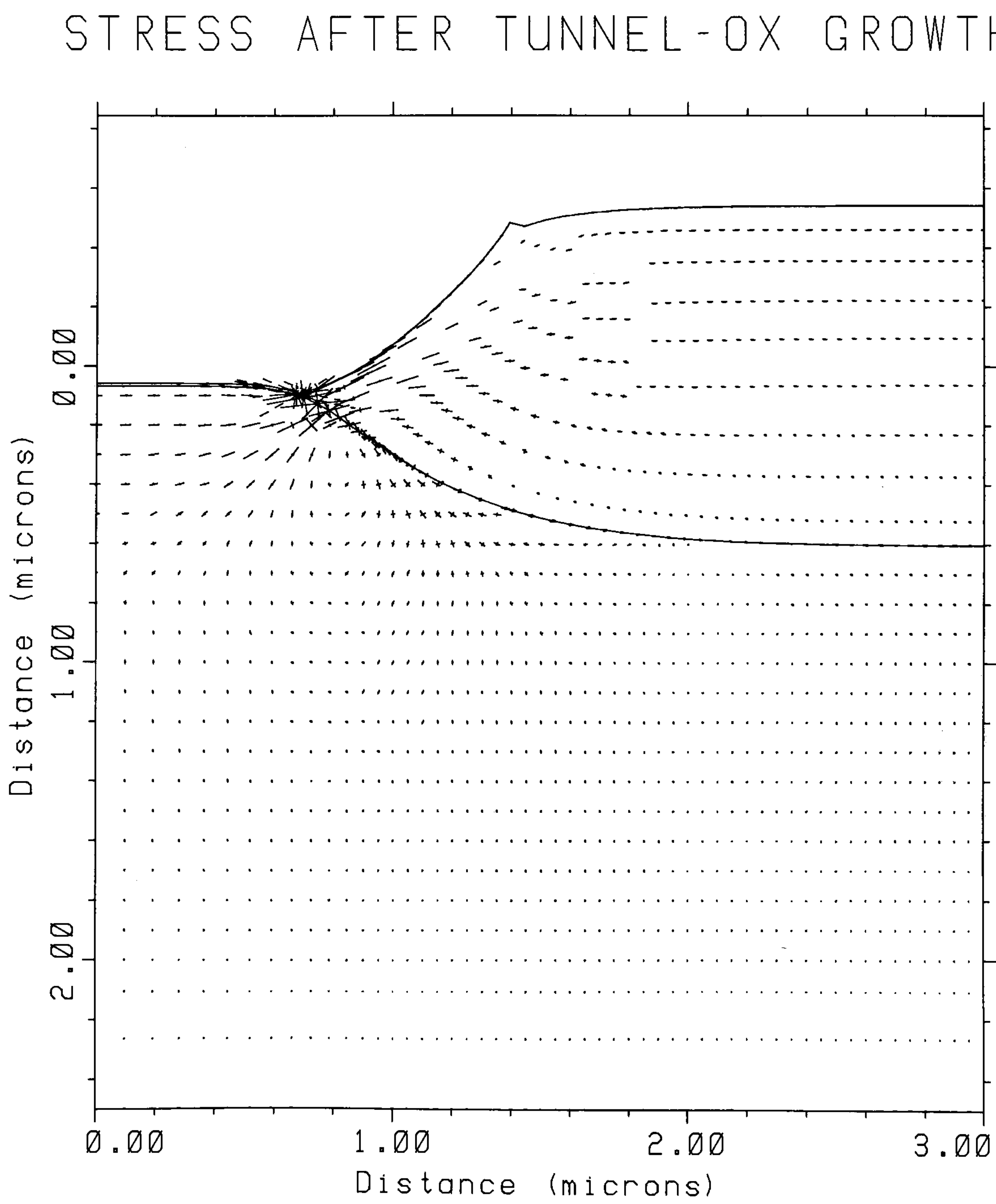



AFTER KOOI OXIDE GROWTH
-1.00
0.00
1.00
2.00
Distance (microns)
0.00
1.00
2.00
3.00
Distance (microns)

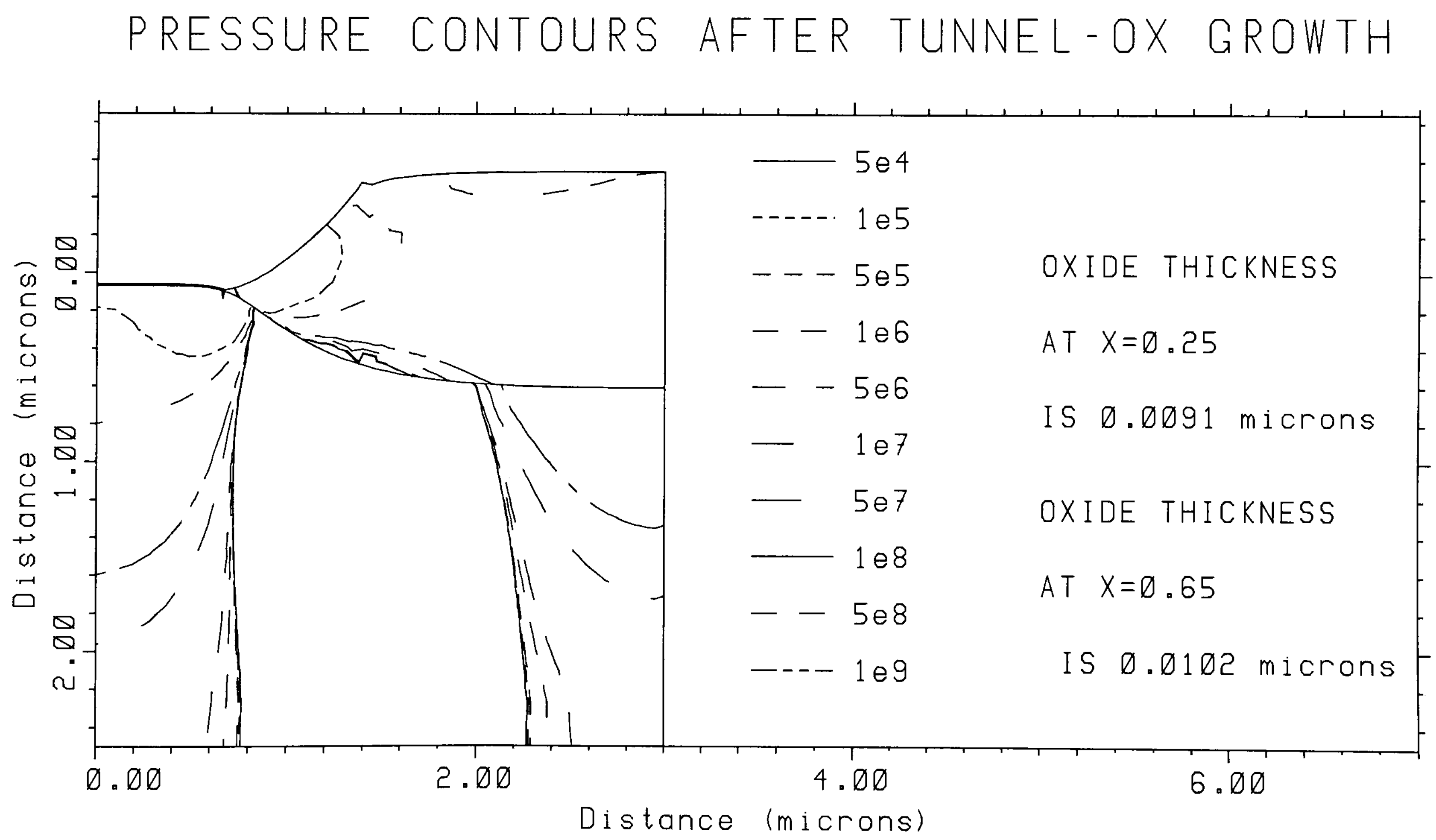
PRESSURE CONTOURS AFTER 1500A ETCH



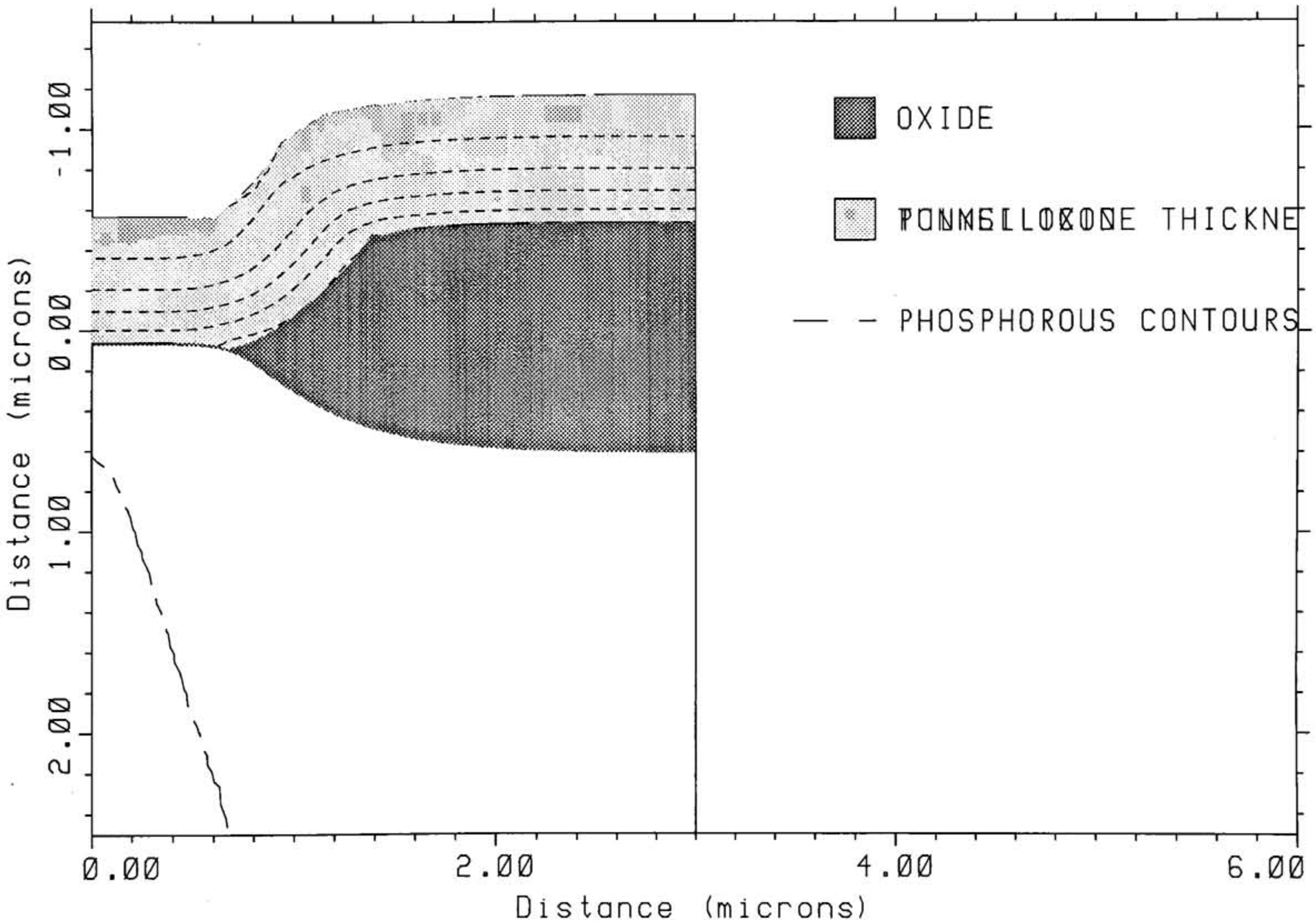

AFTER 1500A ETCH
OXIDE
Distance (microns)
Distance (microns)
0.00
1.00
2.00
3.00
0.00
1.00
2.00

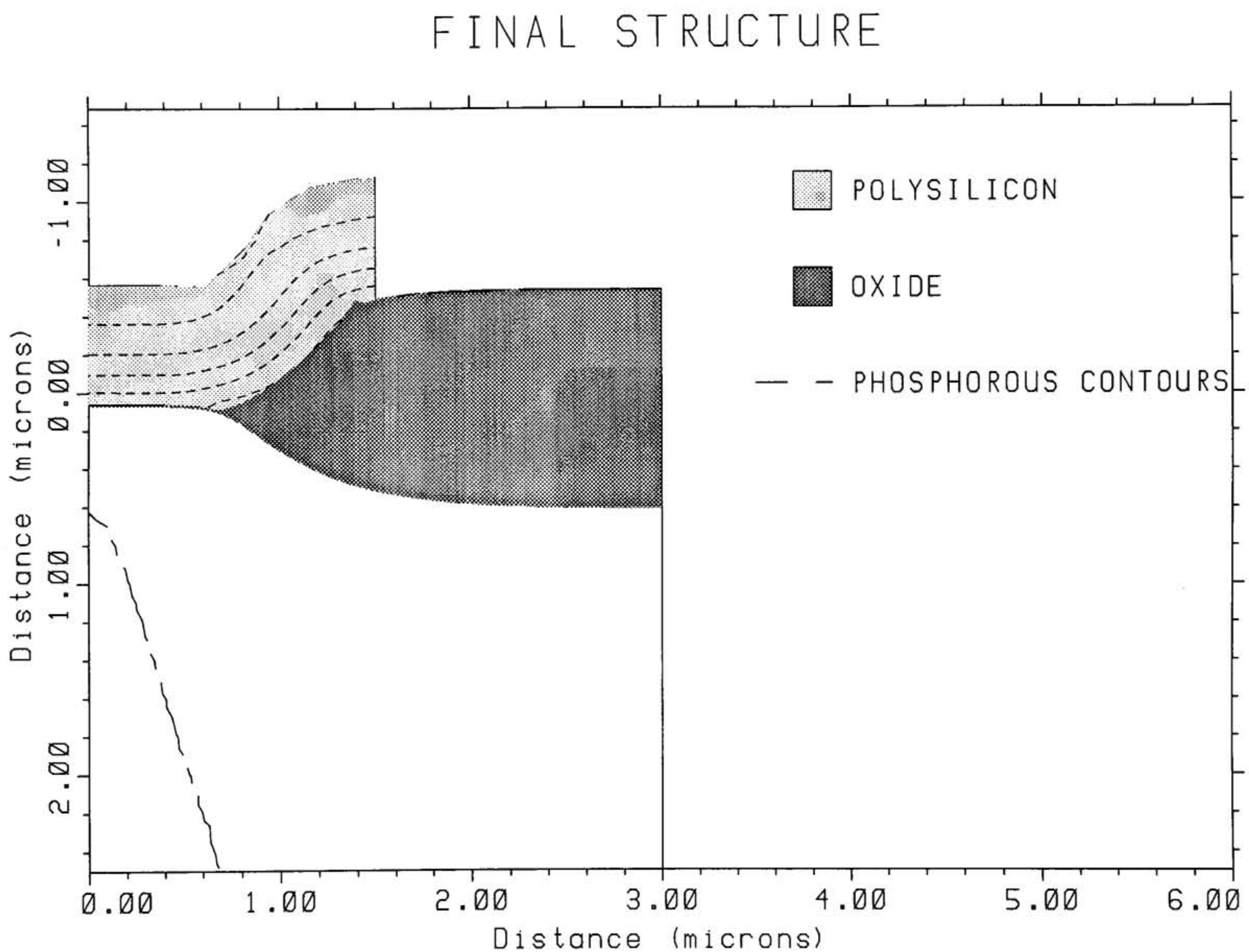


STRESS AFTER TUNNEL-OX GROWTH
0.00
1.00
2.00
3.00
Distance (microns)
0.00
1.00
2.00
Distance (microns)

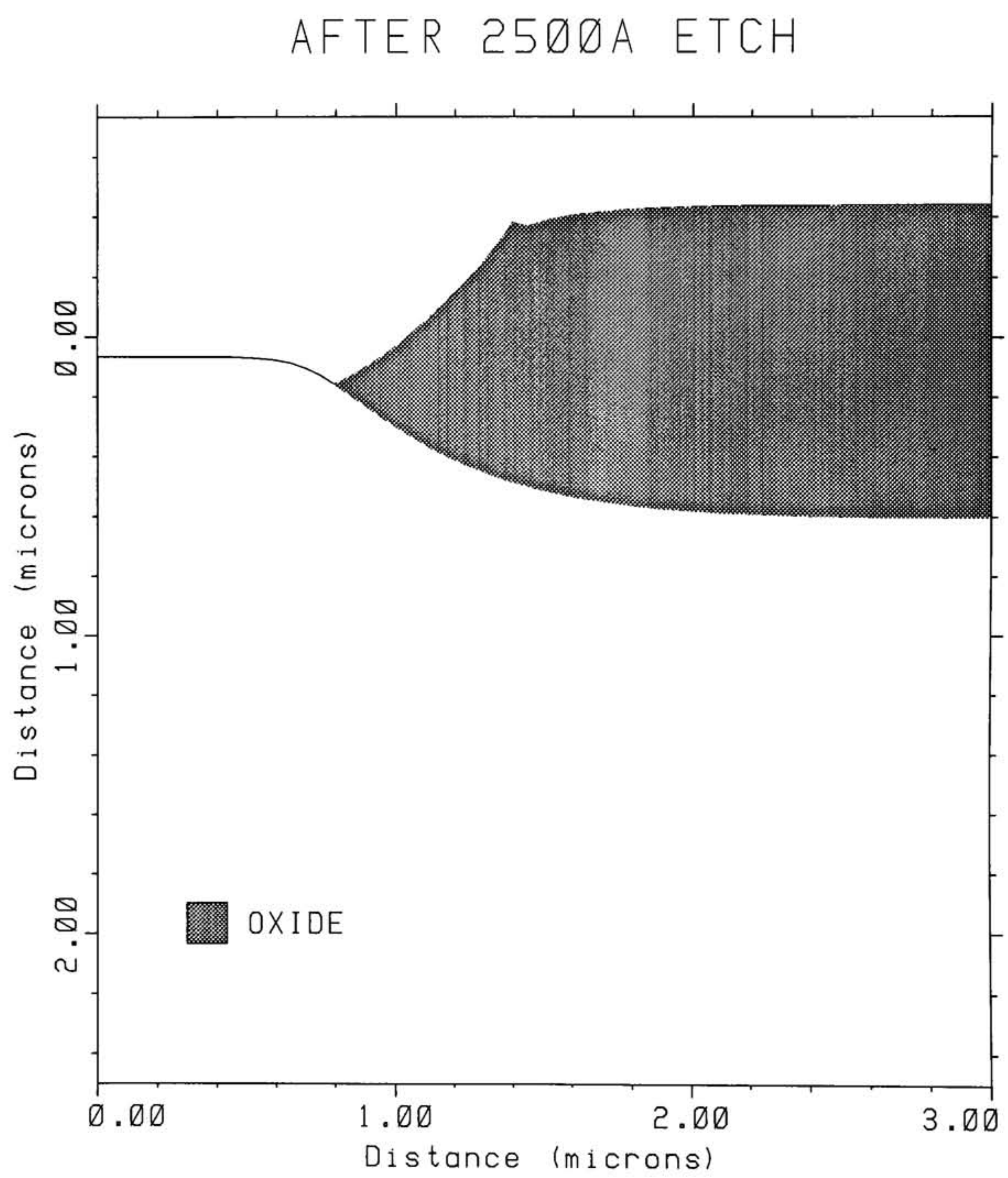

PRESSURE CONTOURS AFTER TUNNEL-OX GROWTH
5e4
1e5
5e5
1e6
5e6
1e7
5e7
1e8
5e8
1e9
OXIDE THICKNESS
AT X=0.25
IS 0.0091 microns
OXIDE THICKNESS
AT X=0.65
IS 0.0102 microns
0.00
2.00
4.00
6.00
Distance (microns)
0.00
1.00
2.00
Distance (microns)

AFTER PHOSPHOROUS IMPLANT



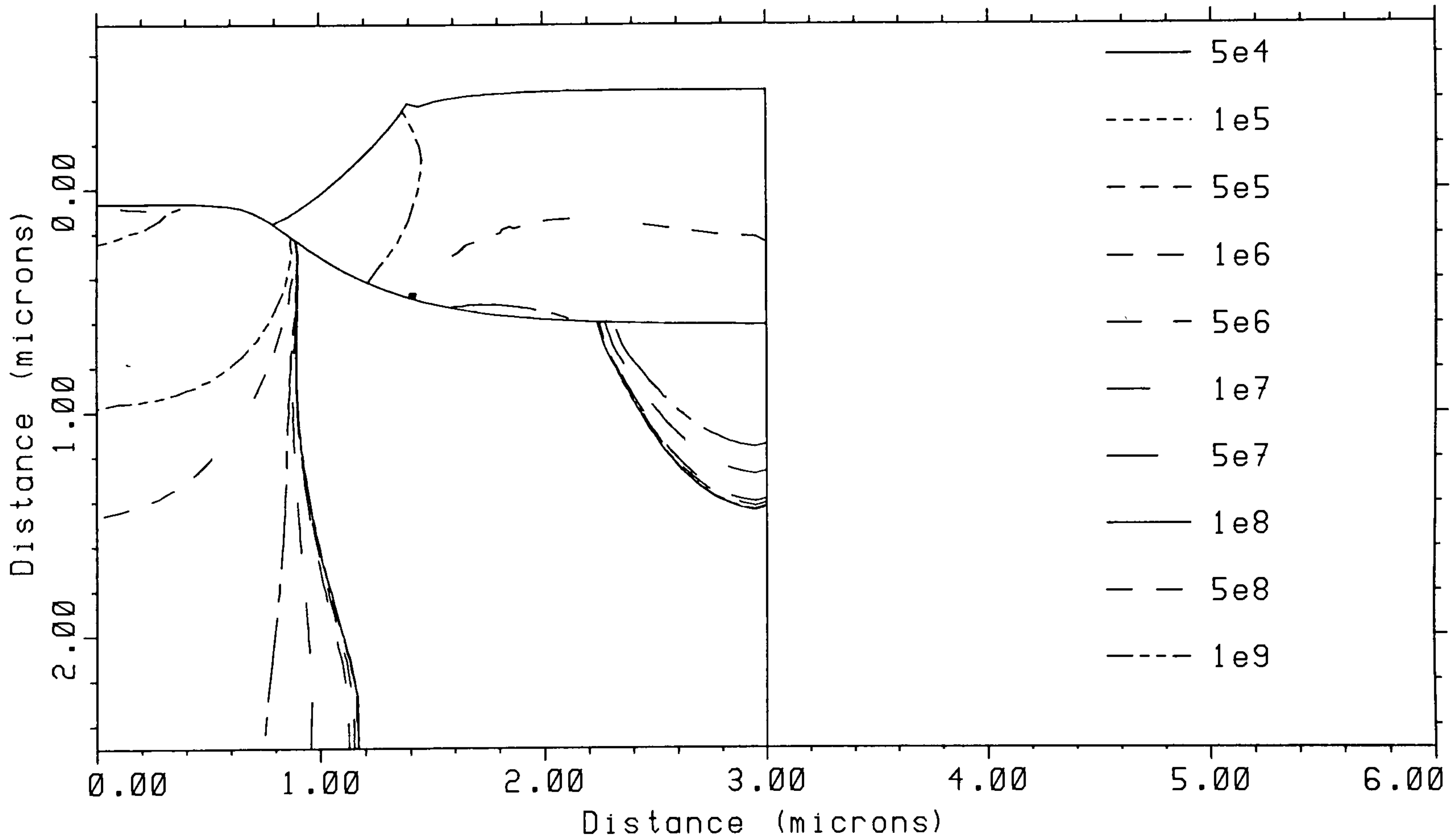

FINAL STRUCTURE
POLYSILICON
OXIDE
PHOSPHOROUS CONTOURS
-1.00
0.00
1.00
2.00
Distance (microns)
0.00
1.00
2.00
3.00
4.00
5.00
6.00
Distance (microns)

2500 Å Etch Back Results

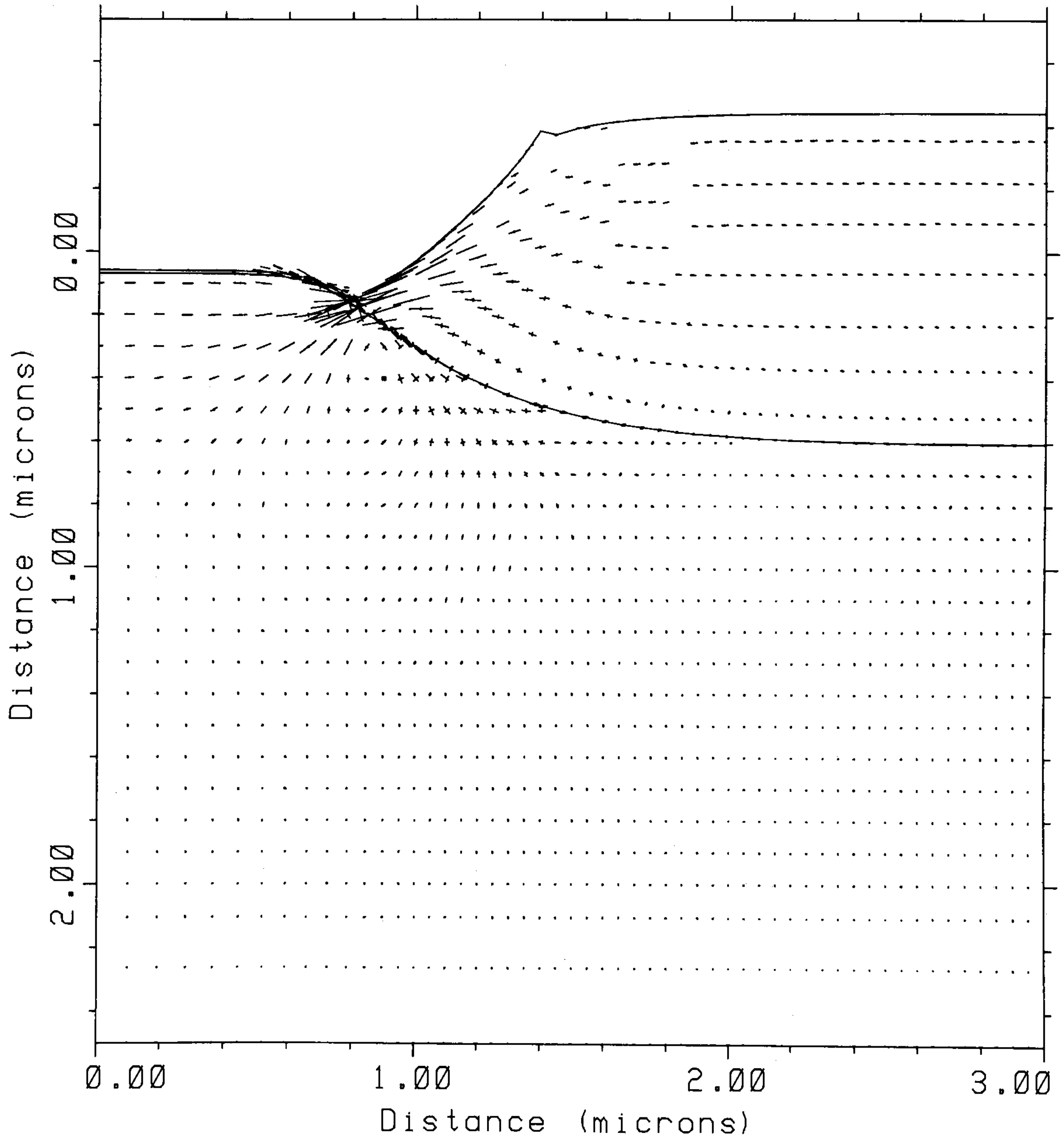


AFTER 2500A ETCH
0.00
1.00
2.00
Distance (microns)
OXIDE
0.00
1.00
2.00
3.00
Distance (microns)

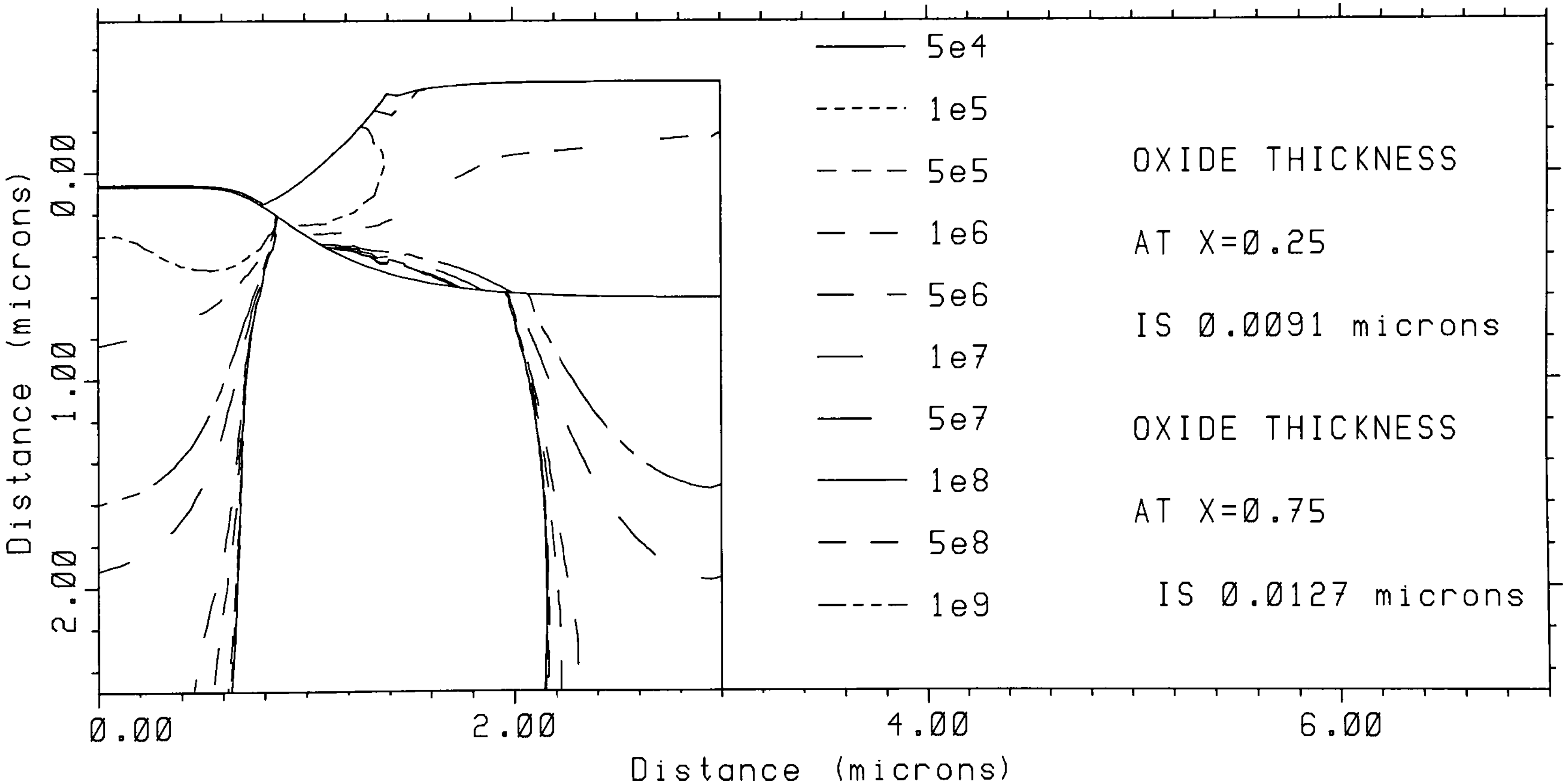
PRESSURE CONTOURS AFTER 2500A ETCH

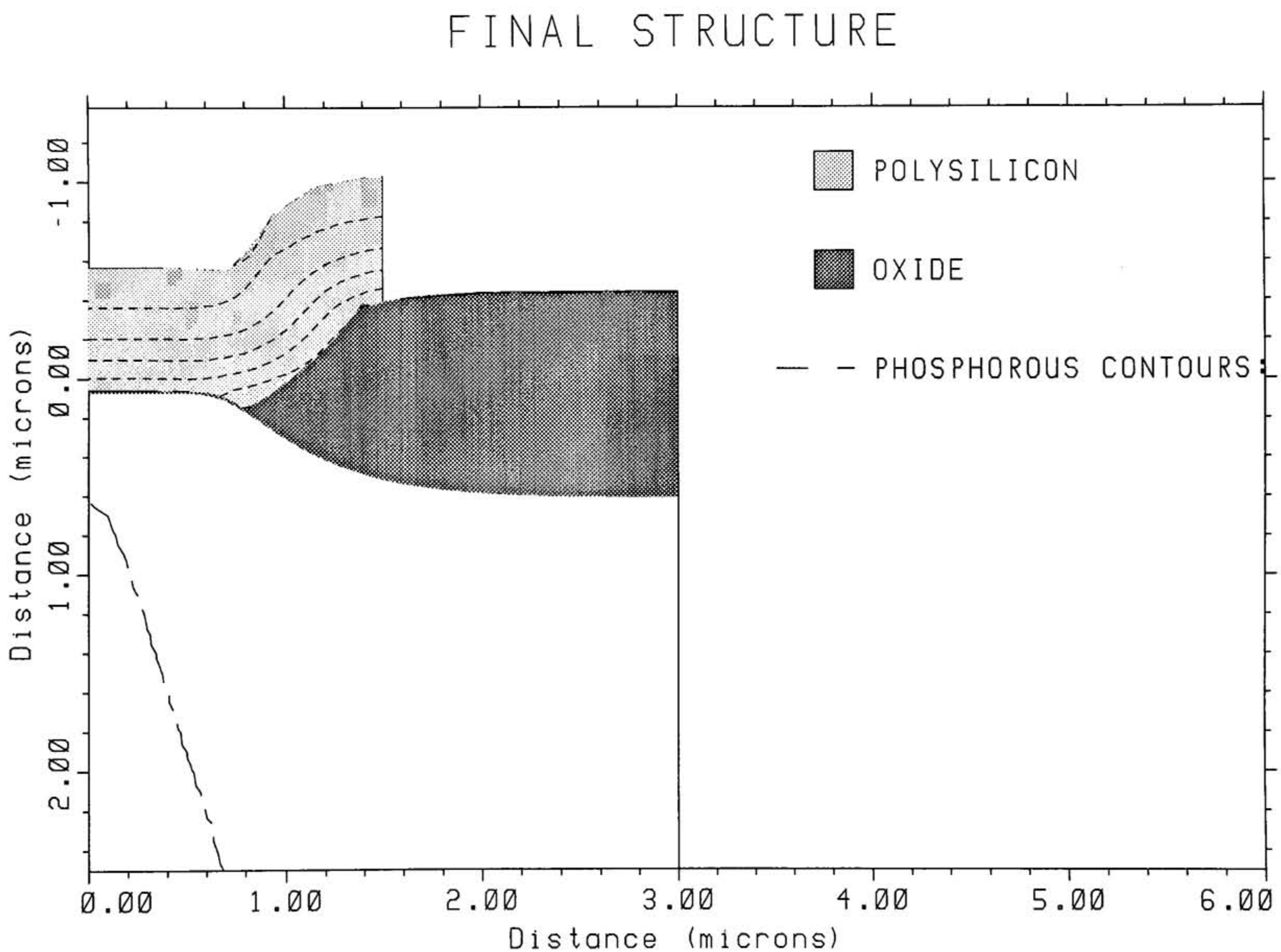


STRESS AFTER TUNNEL-OX GROWTH



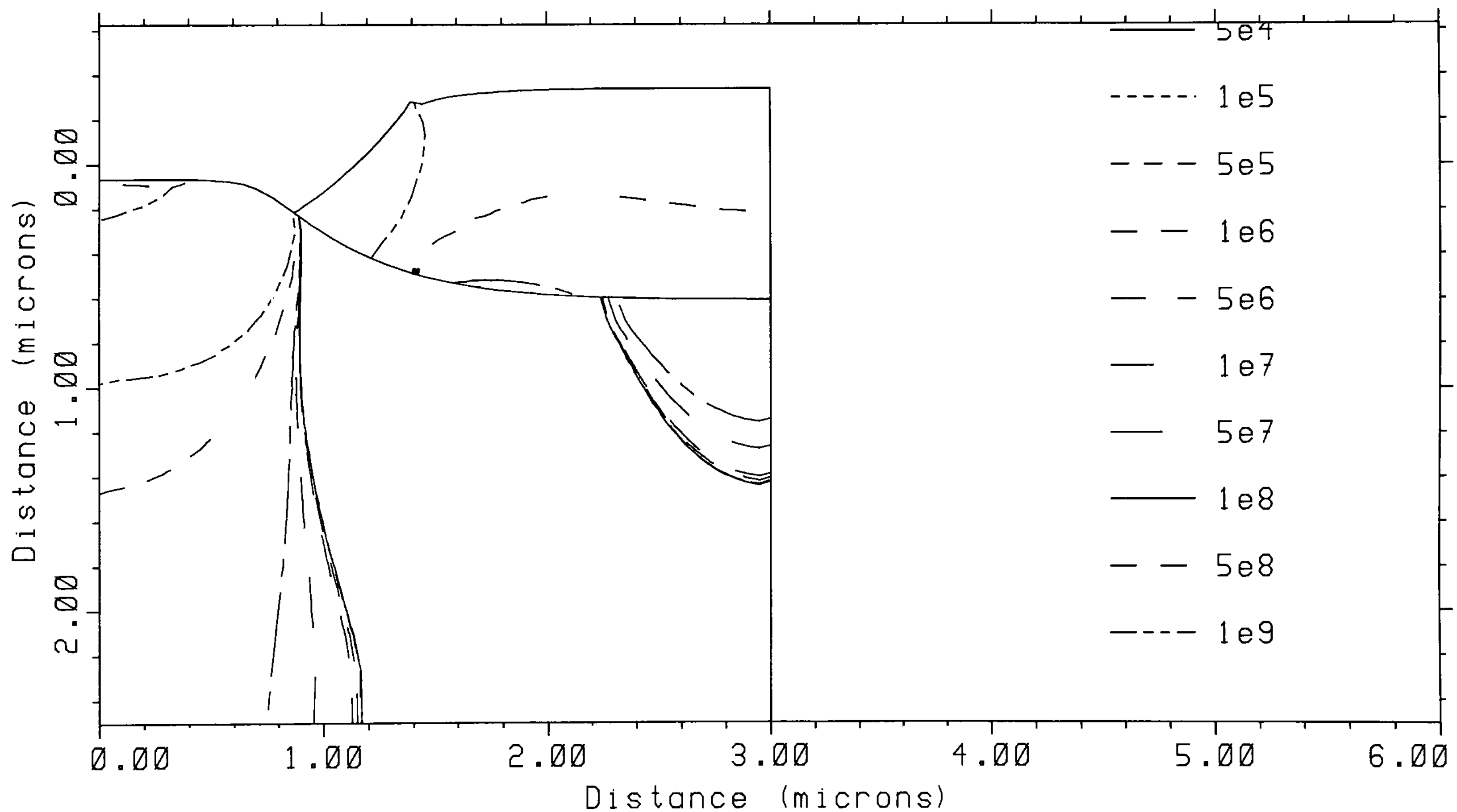
PRESSURE CONTOURS AFTER TUNNEL-OX GROWTH

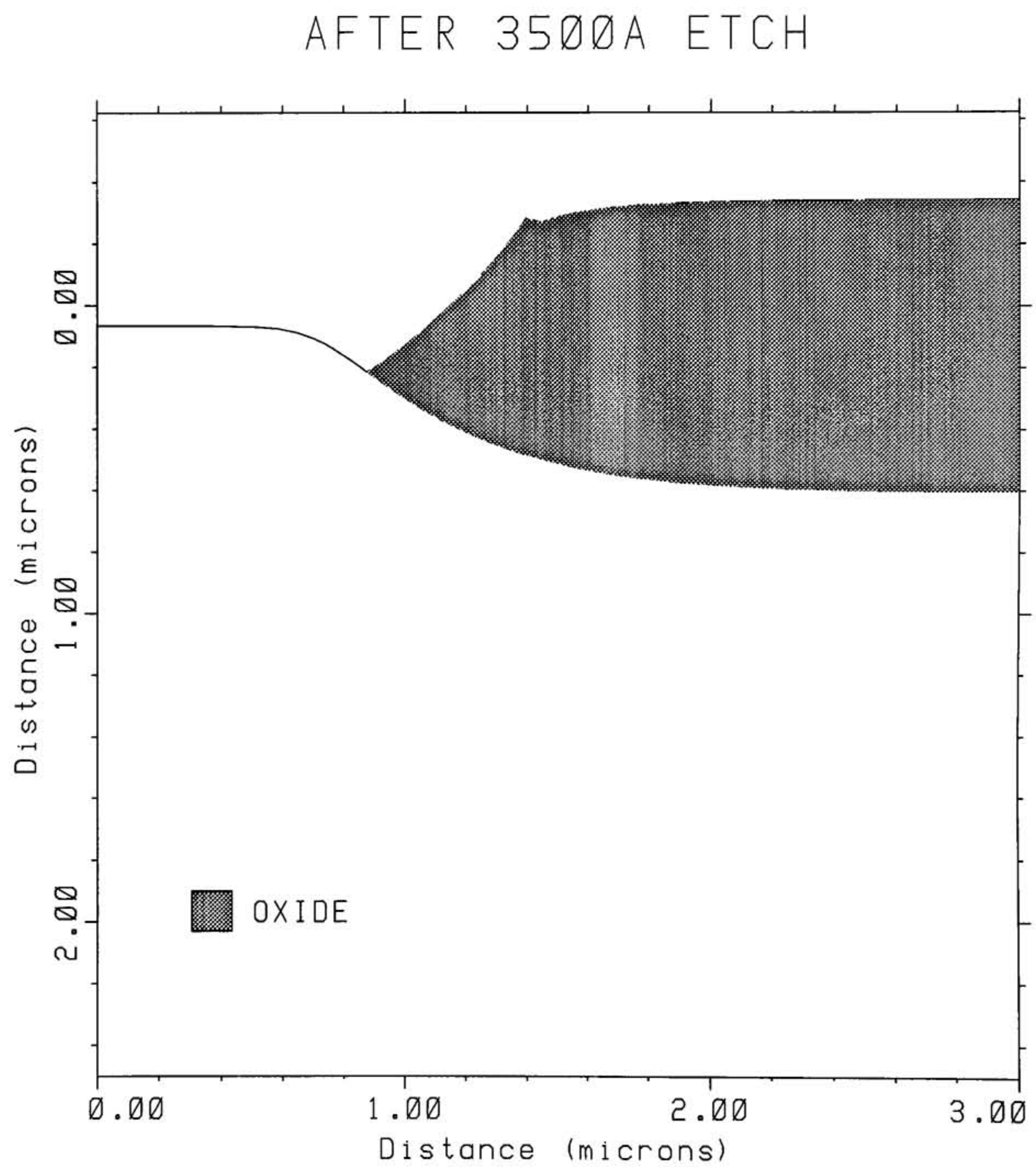



FINAL STRUCTURE
POLYSILICON
OXIDE
PHOSPHOROUS CONTOURS:
-1.00
0.00
1.00
2.00
Distance (microns)
0.00
1.00
2.00
3.00
4.00
5.00
6.00
Distance (microns)

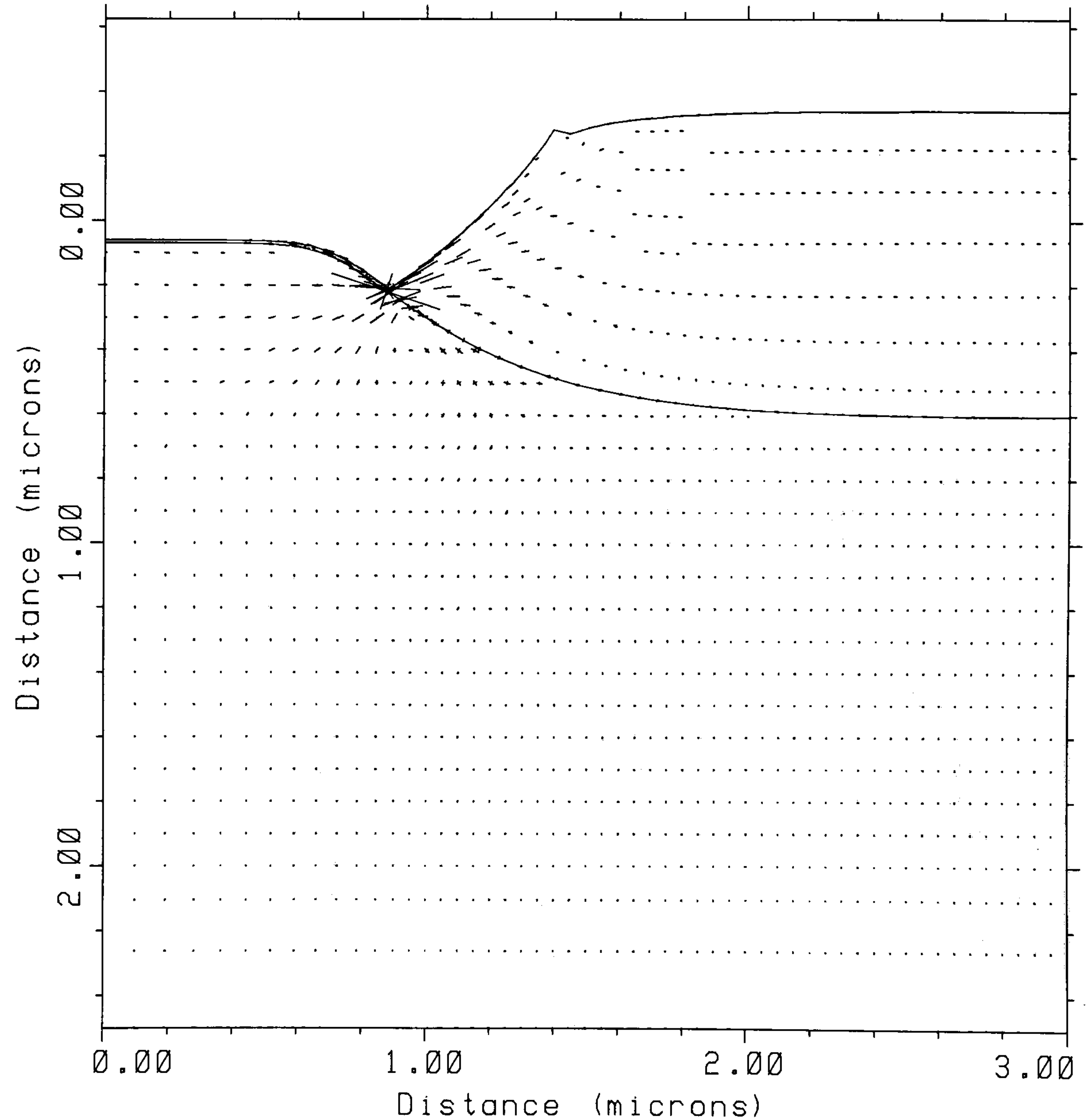
3500 Å Etch Back Results

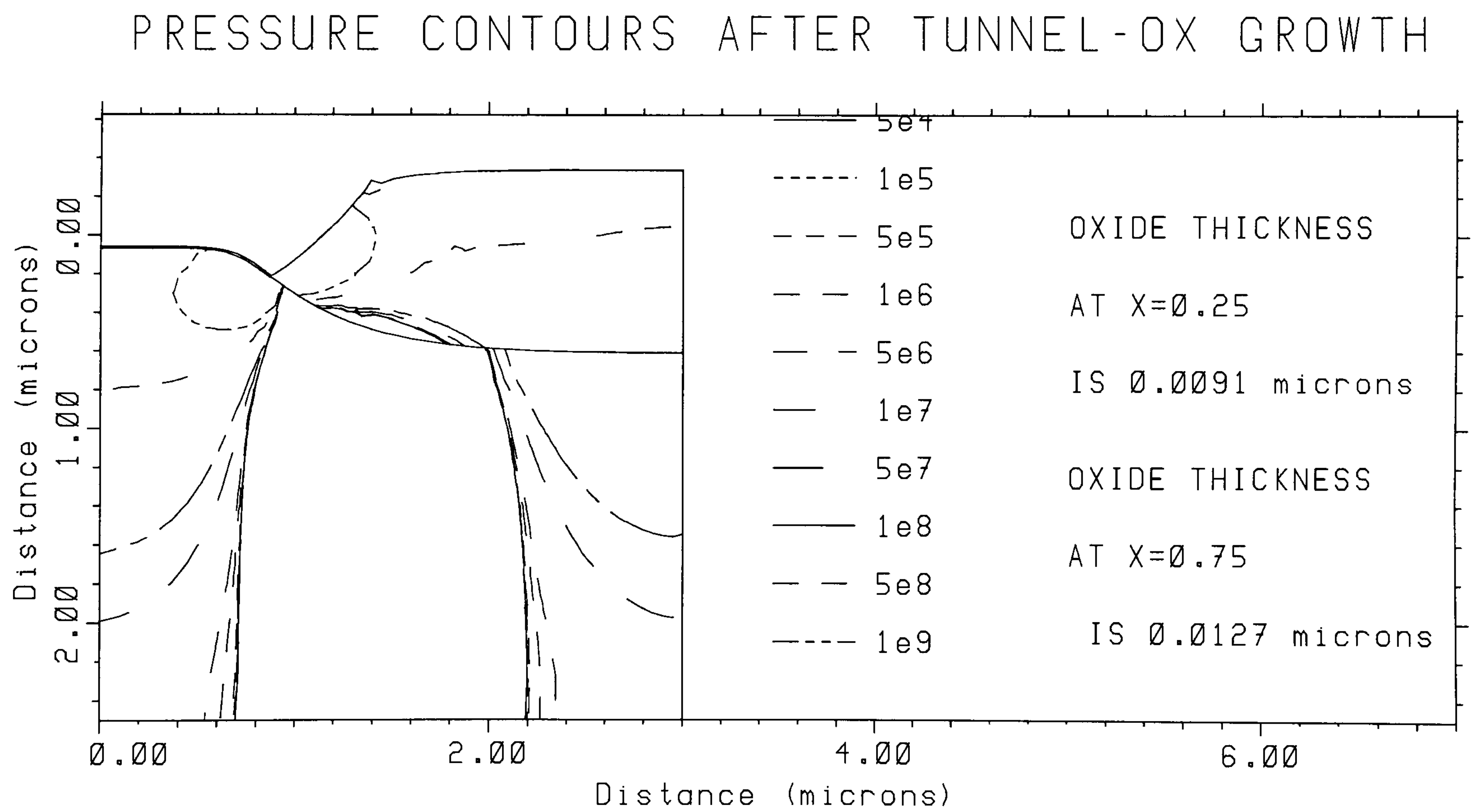
PRESSURE CONTOURS AFTER 3500A ETCH

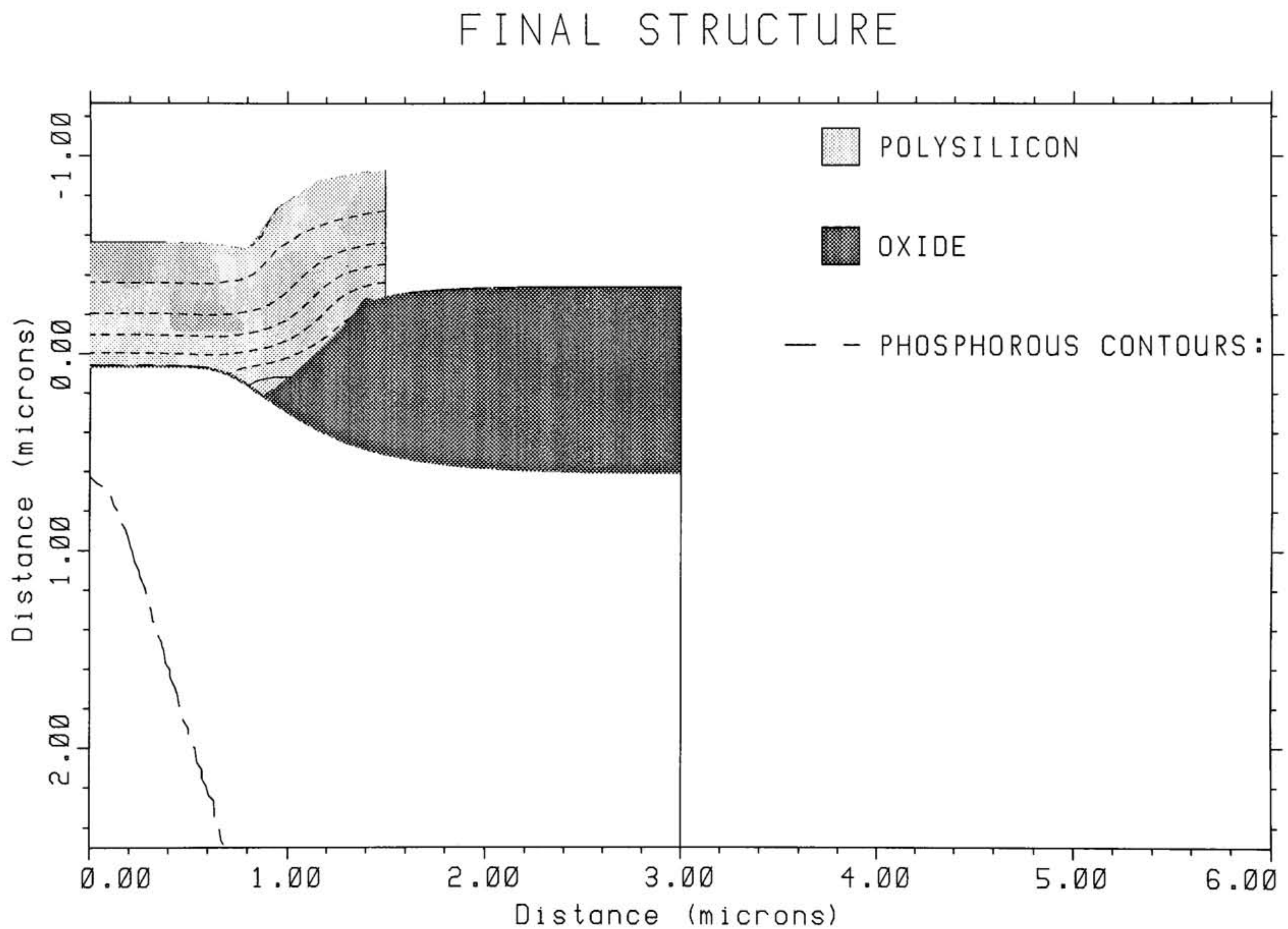



AFTER 3500A ETCH
0.00
1.00
2.00
Distance (microns)
OXIDE
0.00
1.00
2.00
3.00
Distance (microns)

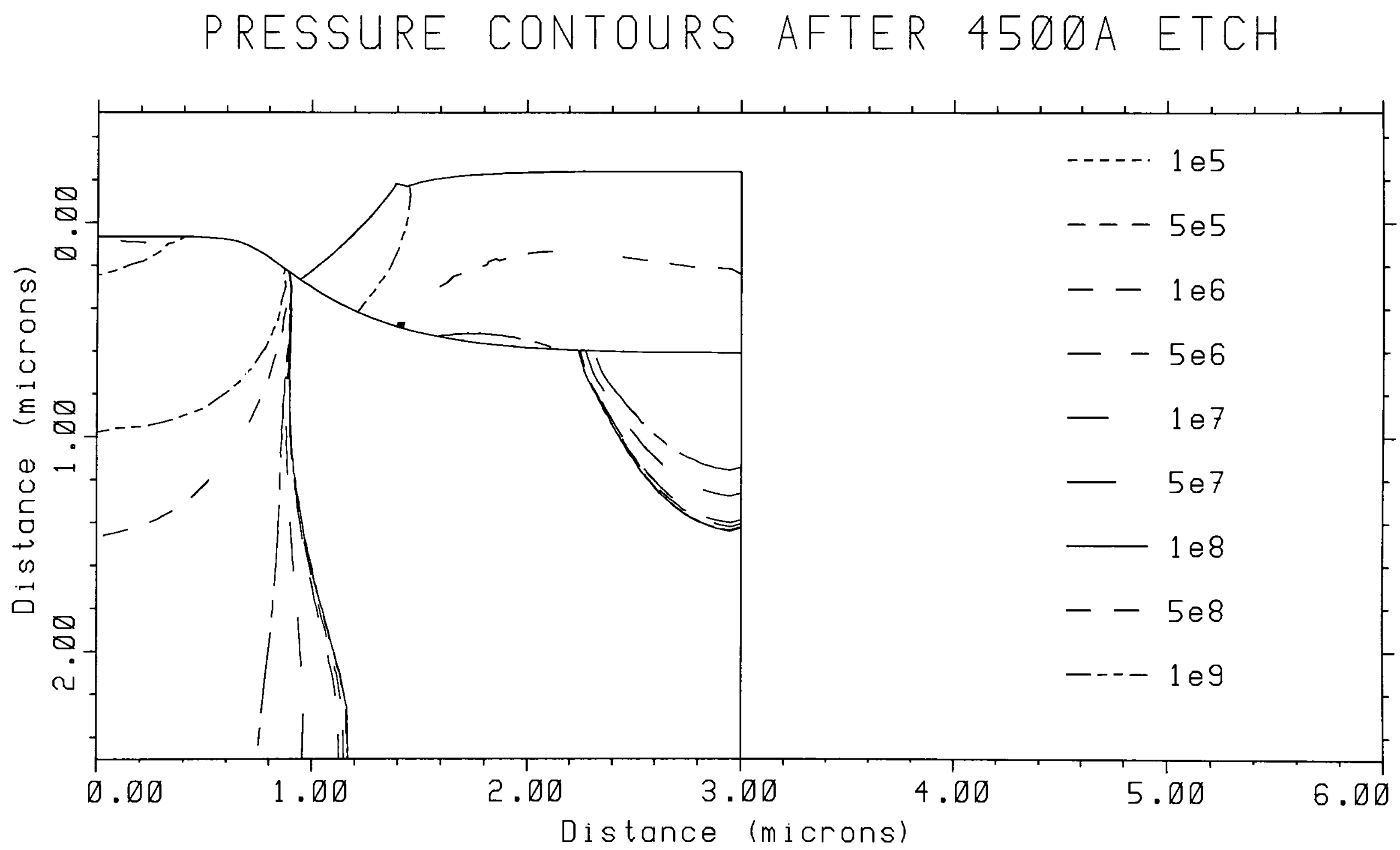
STRESS AFTER TUNNEL-OX GROWTH

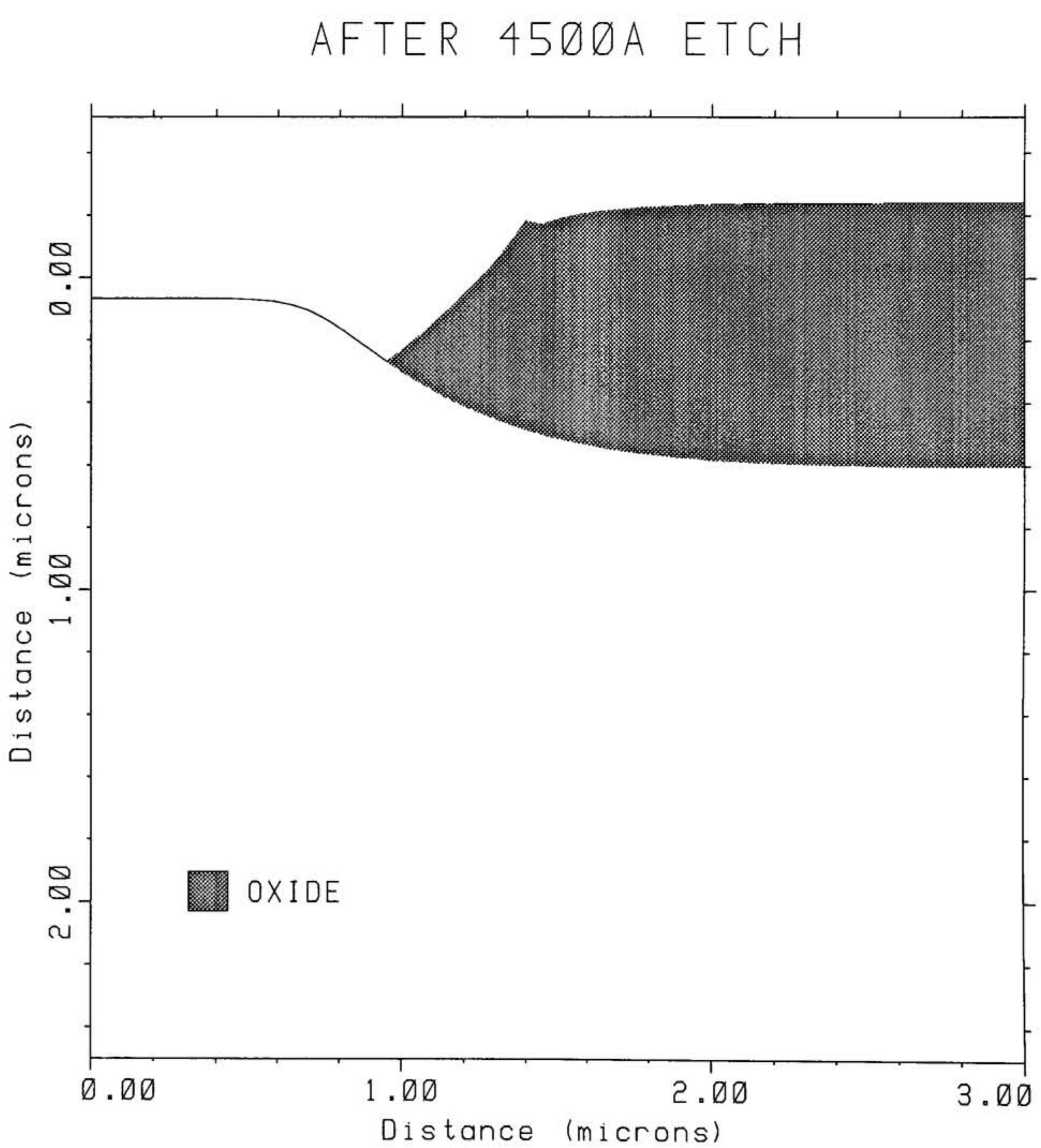



PRESSURE CONTOURS AFTER TUNNEL-OX GROWTH
5e4
1e5
5e5
1e6
5e6
1e7
5e7
1e8
5e8
1e9
OXIDE THICKNESS
AT X=0.25
IS 0.0091 microns
OXIDE THICKNESS
AT X=0.75
IS 0.0127 microns
0.00
2.00
4.00
6.00
Distance (microns)
0.00
1.00
2.00
Distance (microns)

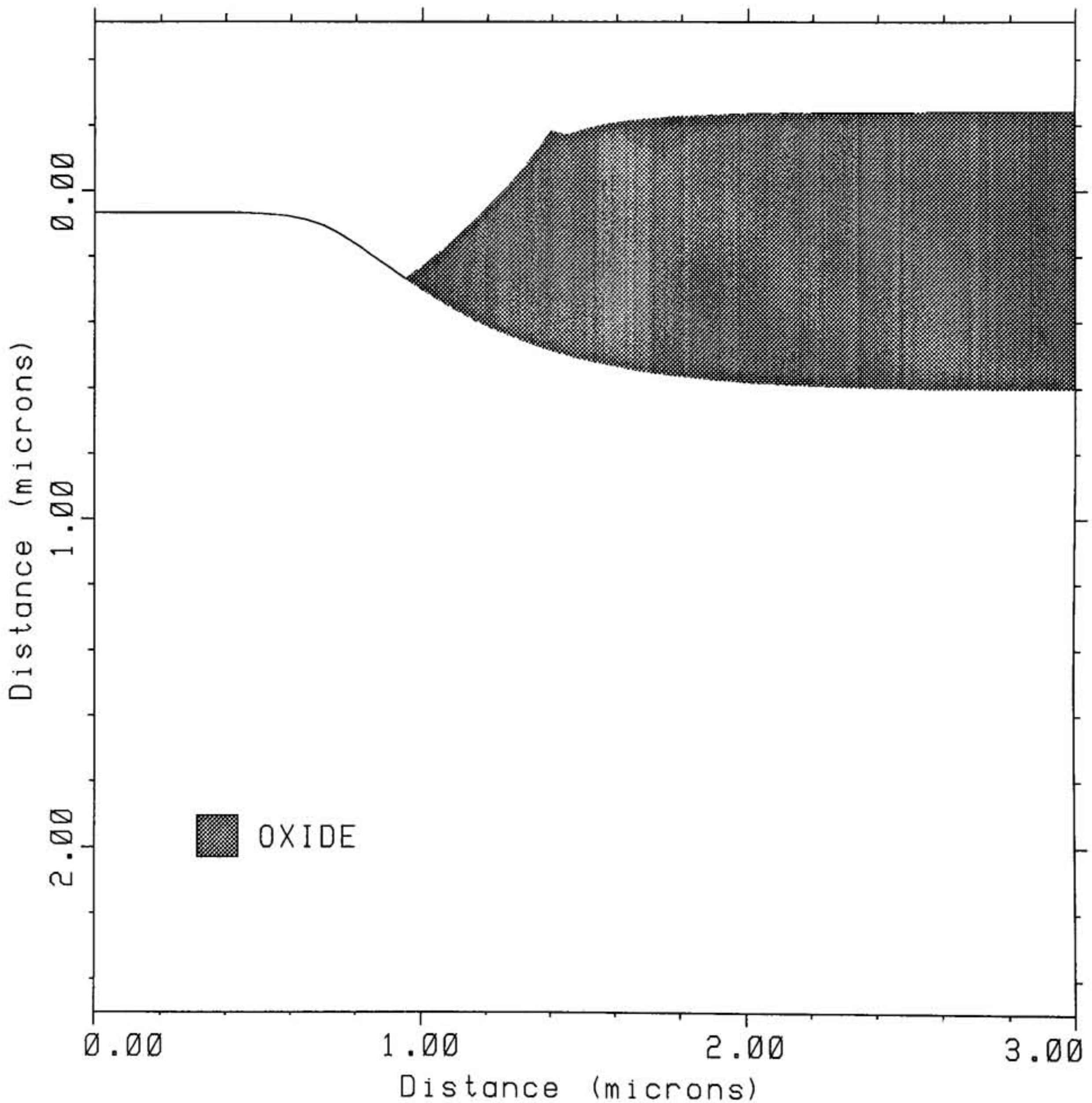

FINAL STRUCTURE
POLYSILICON
OXIDE
PHOSPHOROUS CONTOURS:
Distance (microns)
-1.00
0.00
1.00
2.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
Distance (microns)

4500 Å Etch Back Results

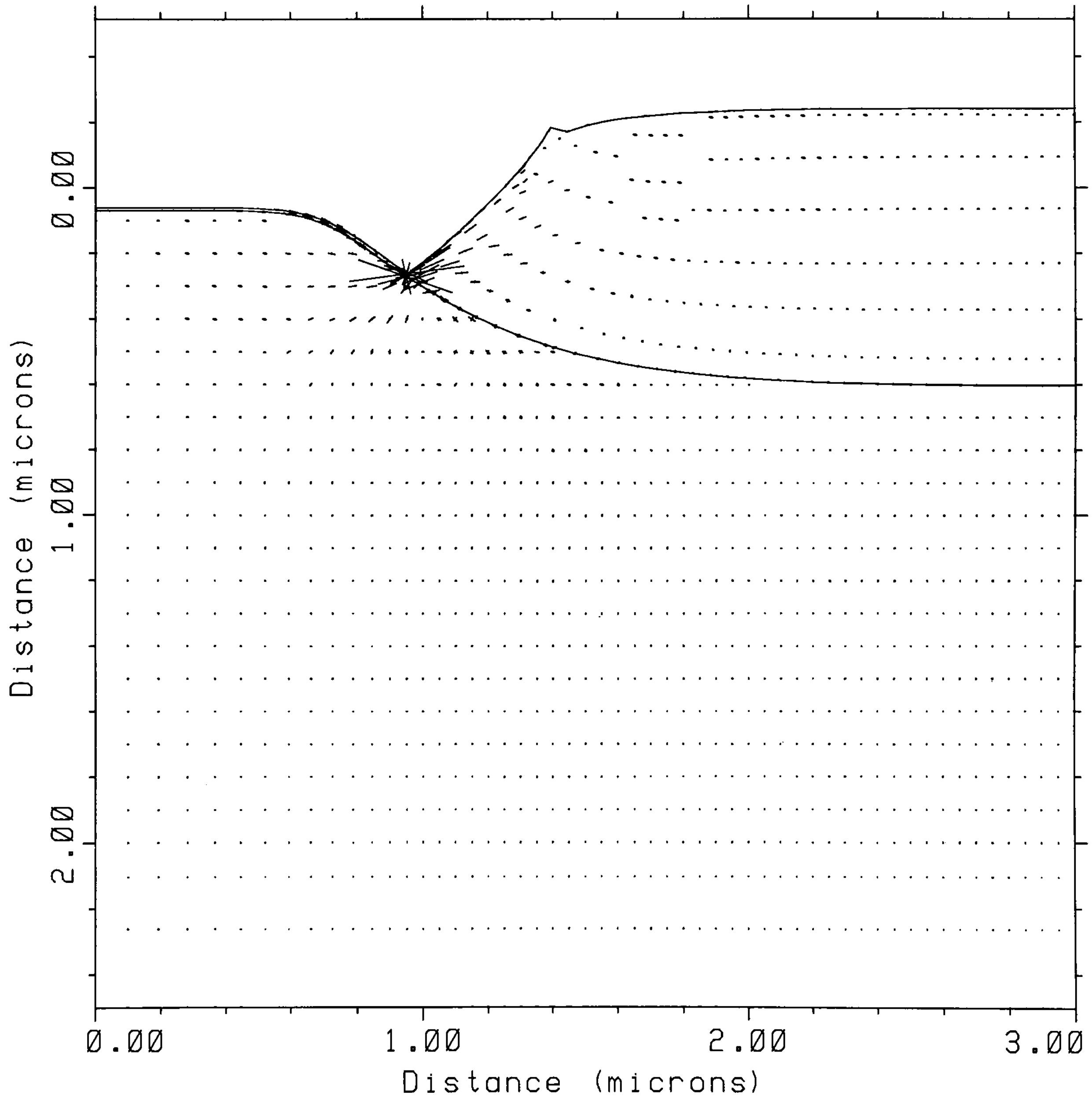

PRESSURE CONTOURS AFTER 4500A ETCH
Distance (microns)
0.00
1.00
2.00
Distance (microns)
0.00
1.00
2.00
3.00
4.00
5.00
6.00
1e5
5e5
1e6
5e6
1e7
5e7
1e8
5e8
1e9


AFTER 4500A ETCH
OXIDE
0.00
1.00
2.00
Distance (microns)
0.00
1.00
2.00
3.00
Distance (microns)

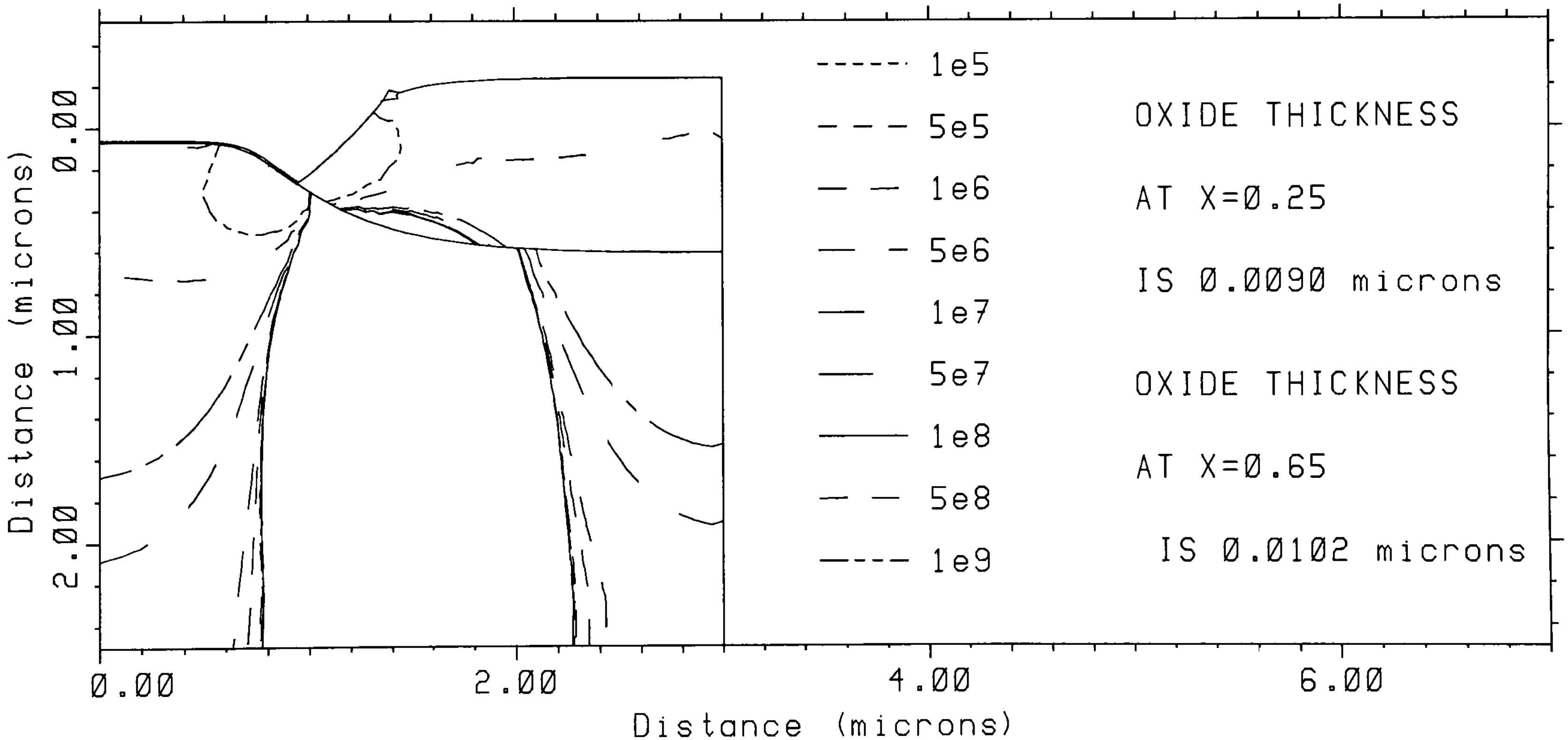
AFTER 4500A ETCH

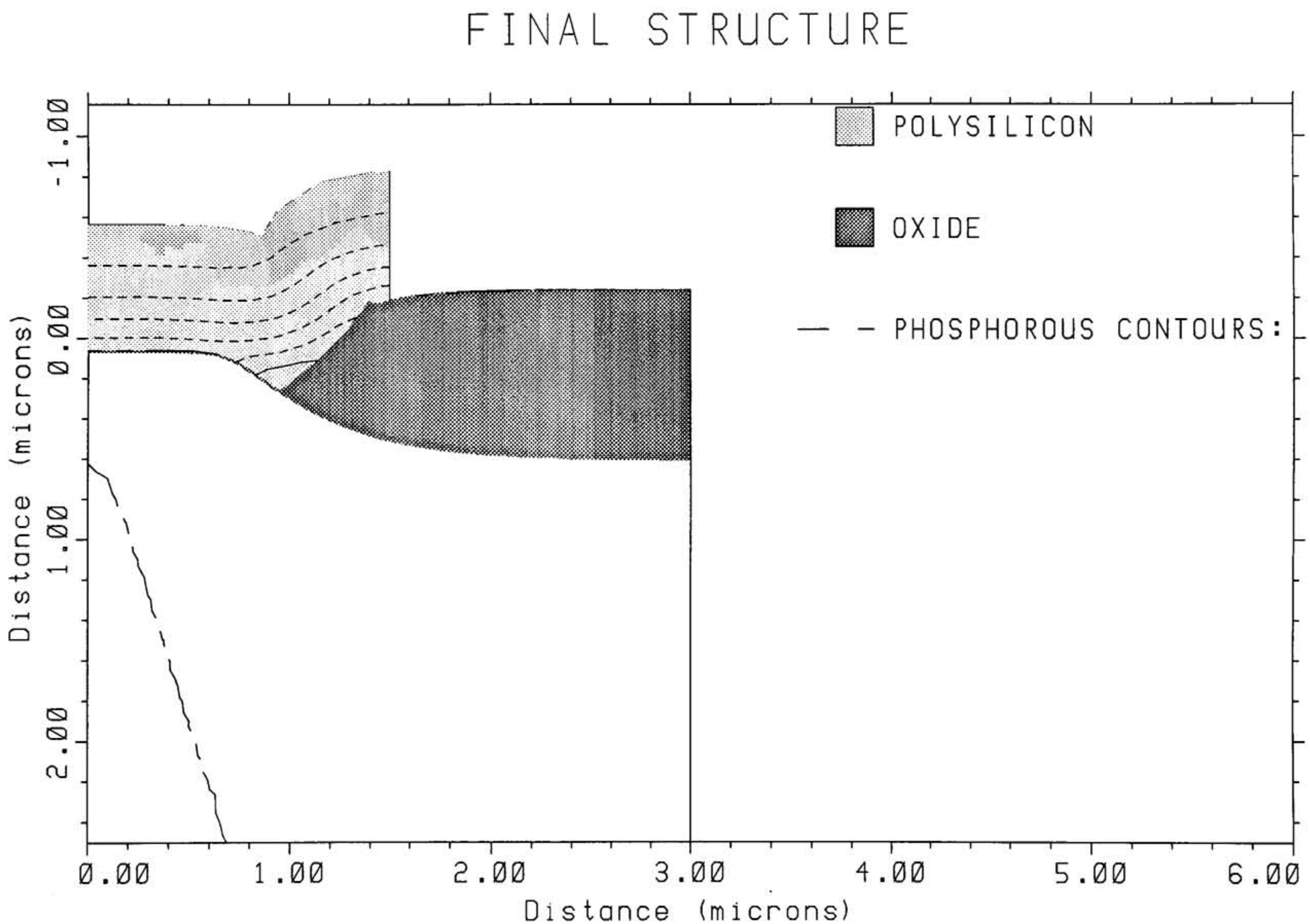


STRESS AFTER TUNNEL-OX GROWTH



PRESSURE CONTOURS AFTER TUNNEL-OX GROWTH

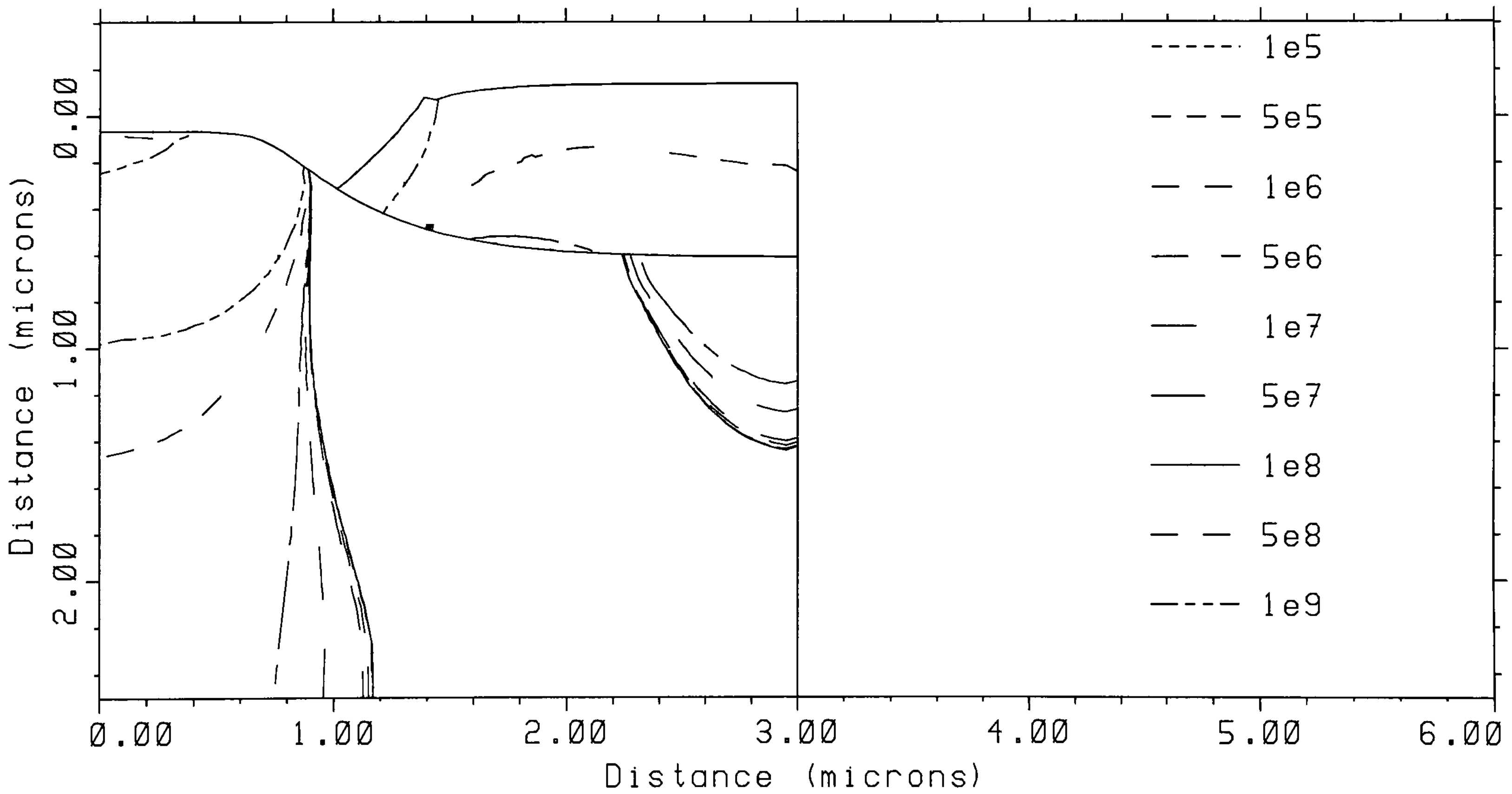


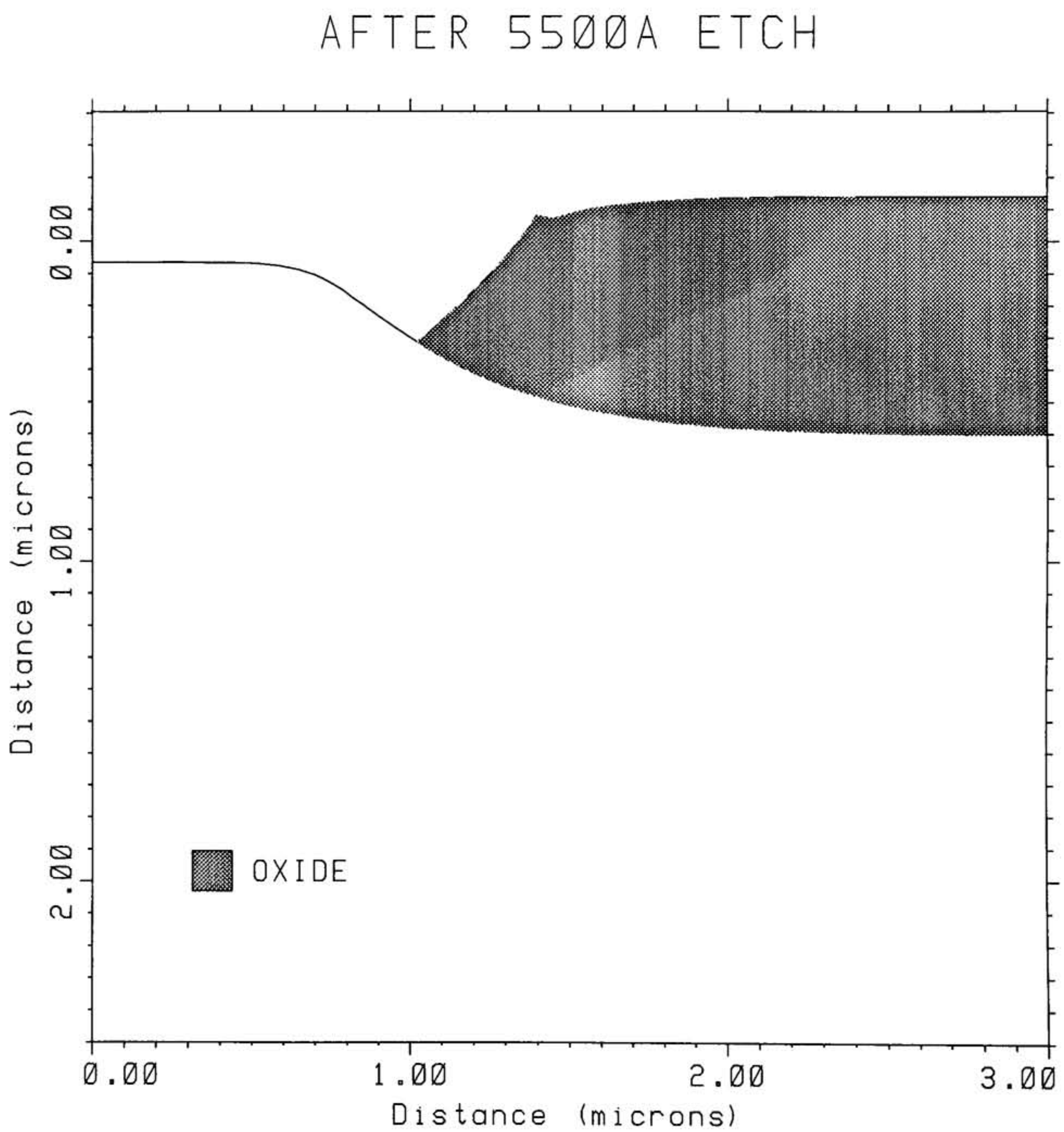


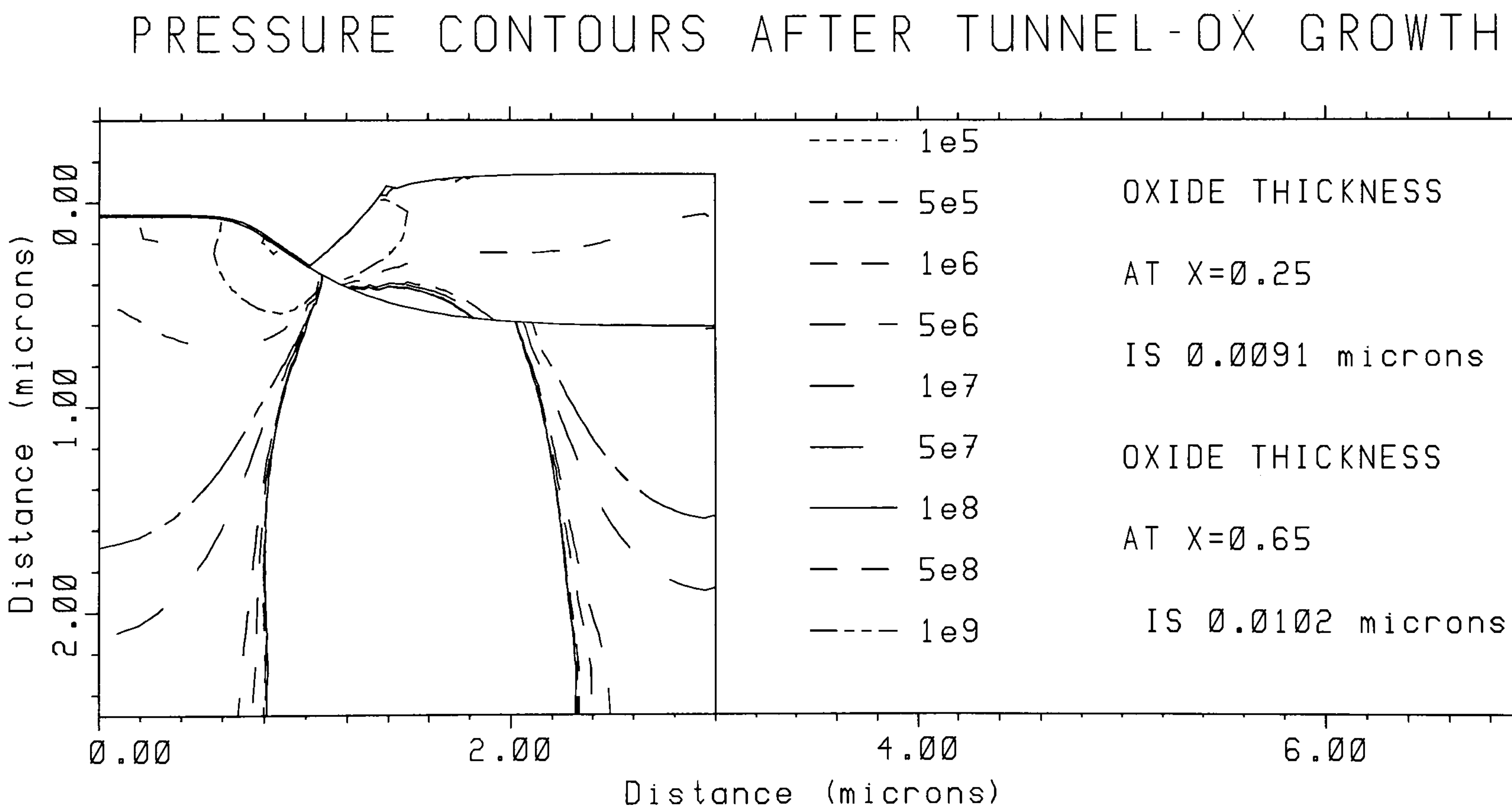
FINAL STRUCTURE
POLYSILICON
OXIDE
PHOSPHOROUS CONTOURS:
-1.00
0.00
1.00
2.00
Distance (microns)
0.00
1.00
2.00
3.00
4.00
5.00
6.00
Distance (microns)

5500 Å Etch Back Results

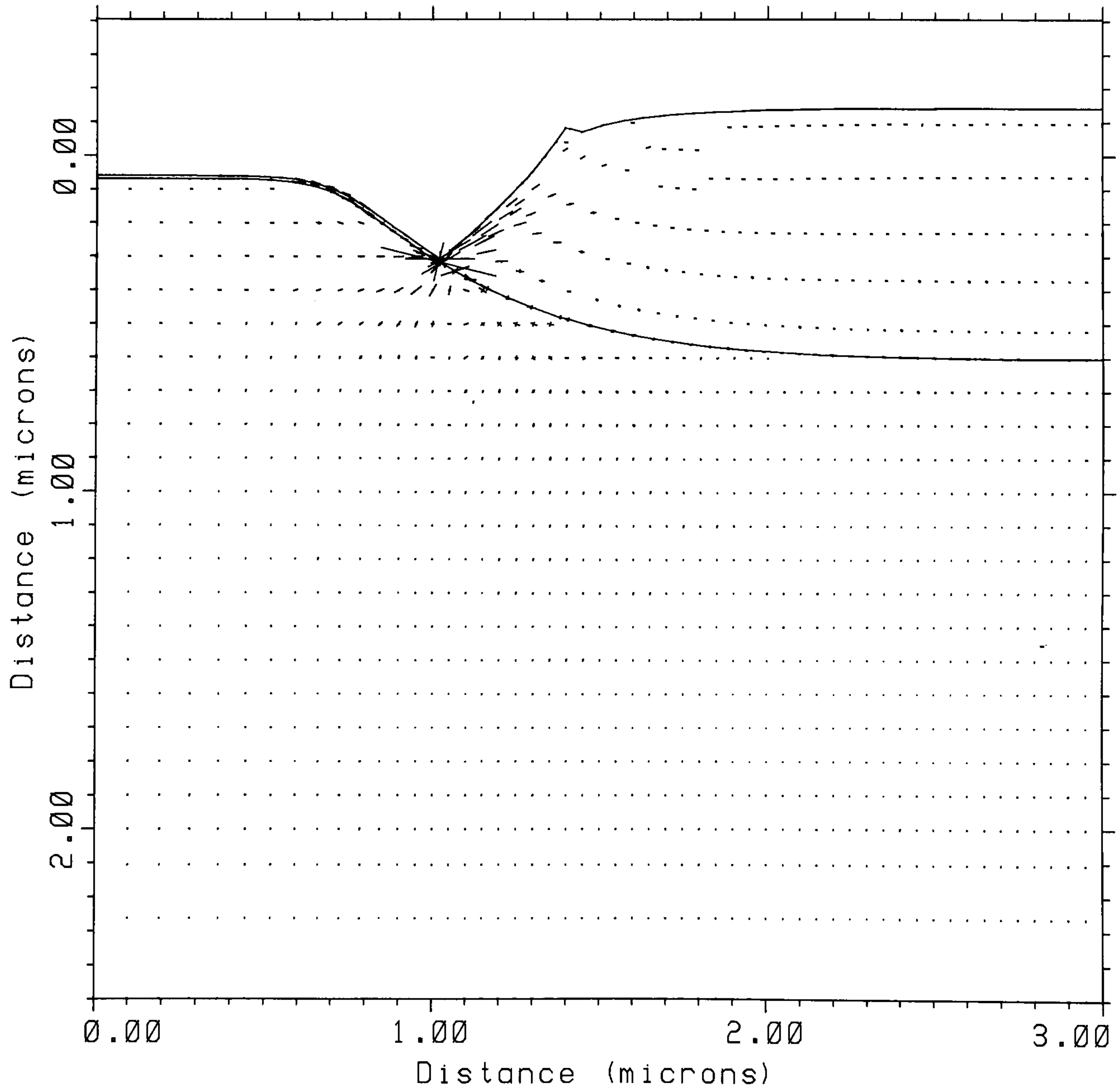
PRESSURE CONTOURS AFTER 5500A ETCH

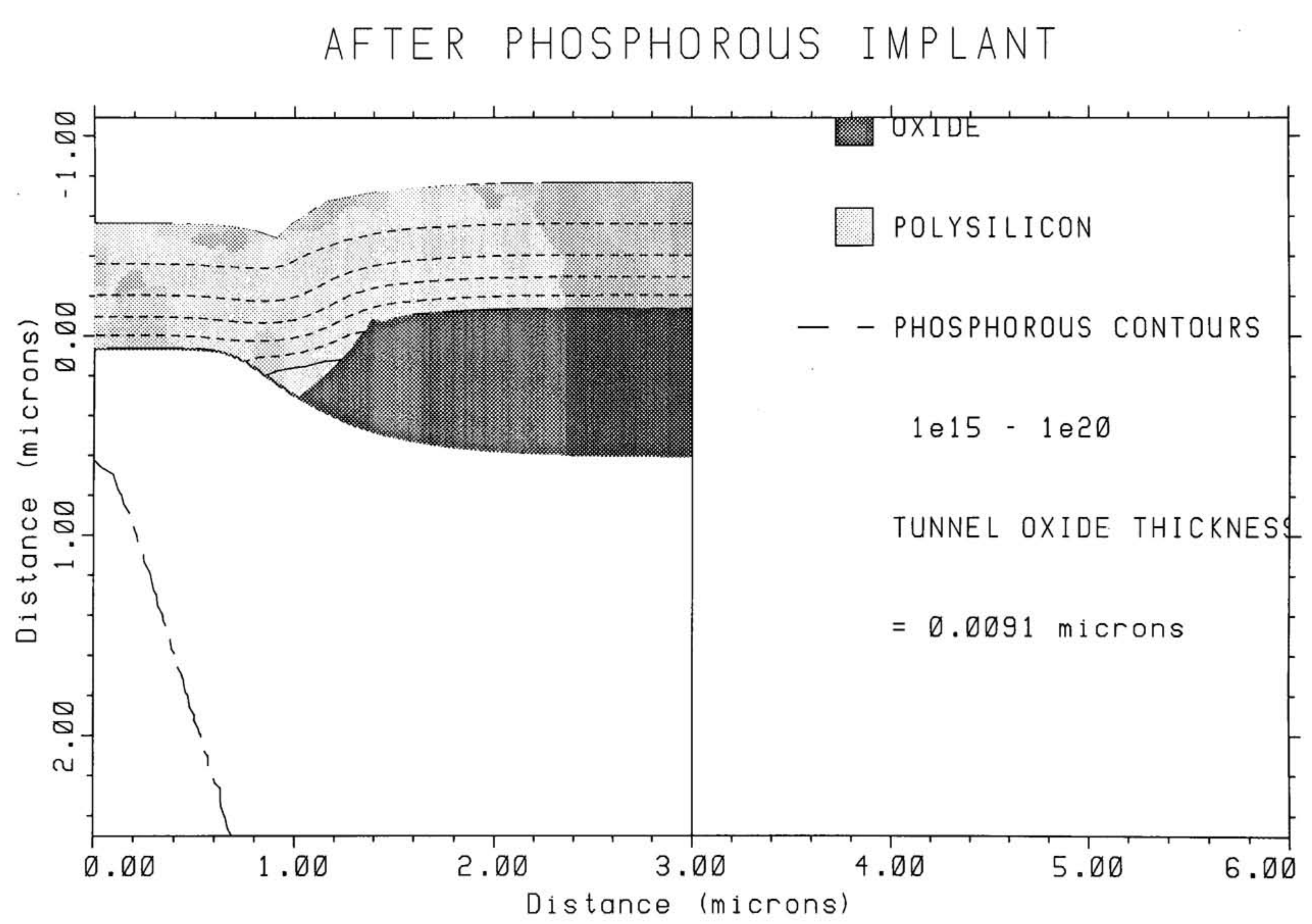



AFTER 5500A ETCH
OXIDE
0.00
1.00
2.00
3.00
Distance (microns)
0.00
1.00
2.00
Distance (microns)


PRESSURE CONTOURS AFTER TUNNEL-OX GROWTH
1e5
5e5
1e6
5e6
1e7
5e7
1e8
5e8
1e9
OXIDE THICKNESS
AT X=Ø.25
IS Ø.ØØ91 microns
OXIDE THICKNESS
AT X=Ø.65
IS Ø.Ø1Ø2 microns
Distance (microns)
Ø.ØØ
1.ØØ
2.ØØ
Distance (microns)
Ø.ØØ
2.ØØ
4.ØØ
6.ØØ

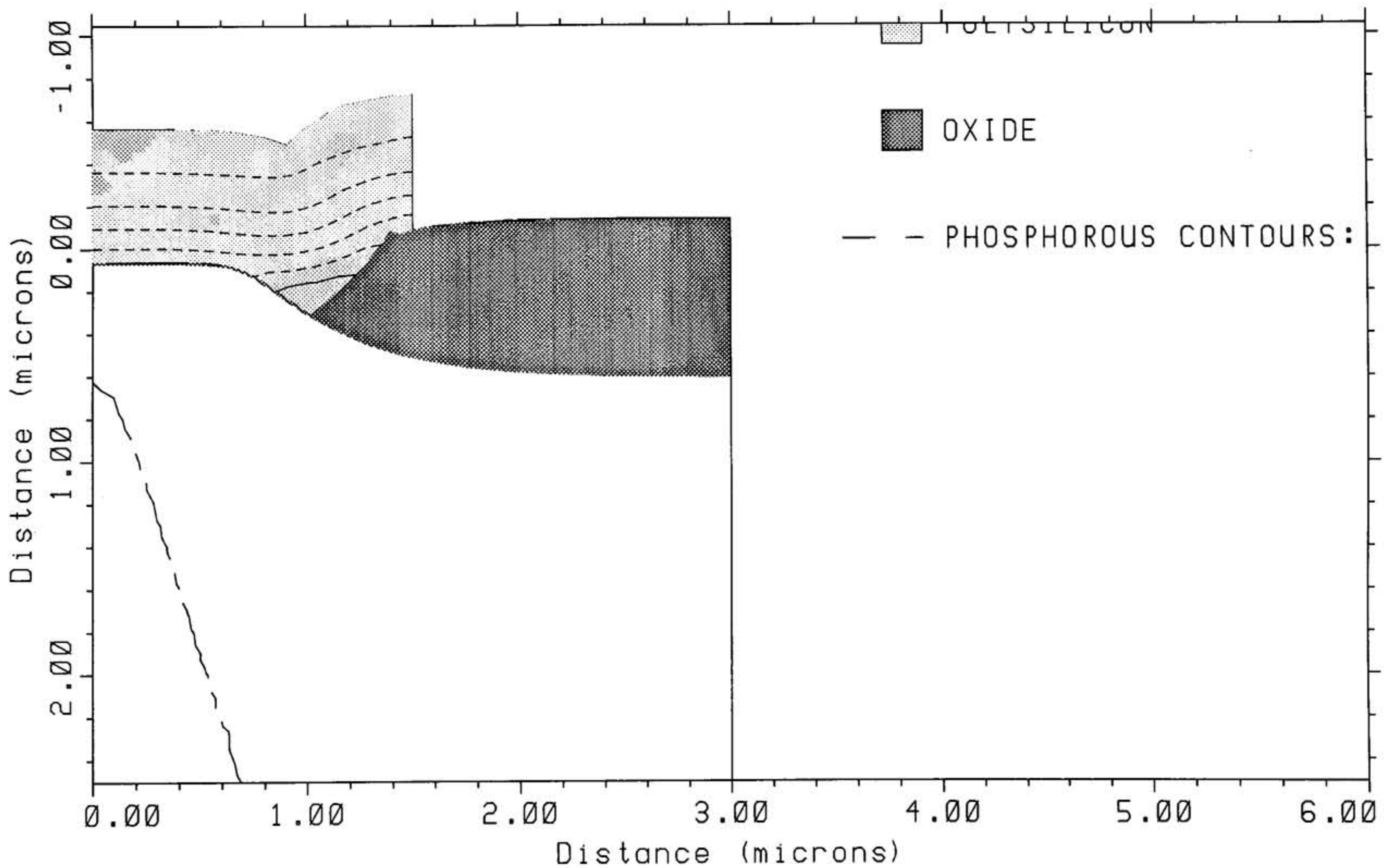
STRESS AFTER TUNNEL-OX GROWTH





AFTER PHOSPHOROUS IMPLANT
OXIDE
POLYSILICON
PHOSPHOROUS CONTOURS
1e15 - 1e20
TUNNEL OXIDE THICKNESS
= 0.0091 microns
Distance (microns)
-1.00
0.00
1.00
2.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
Distance (microns)

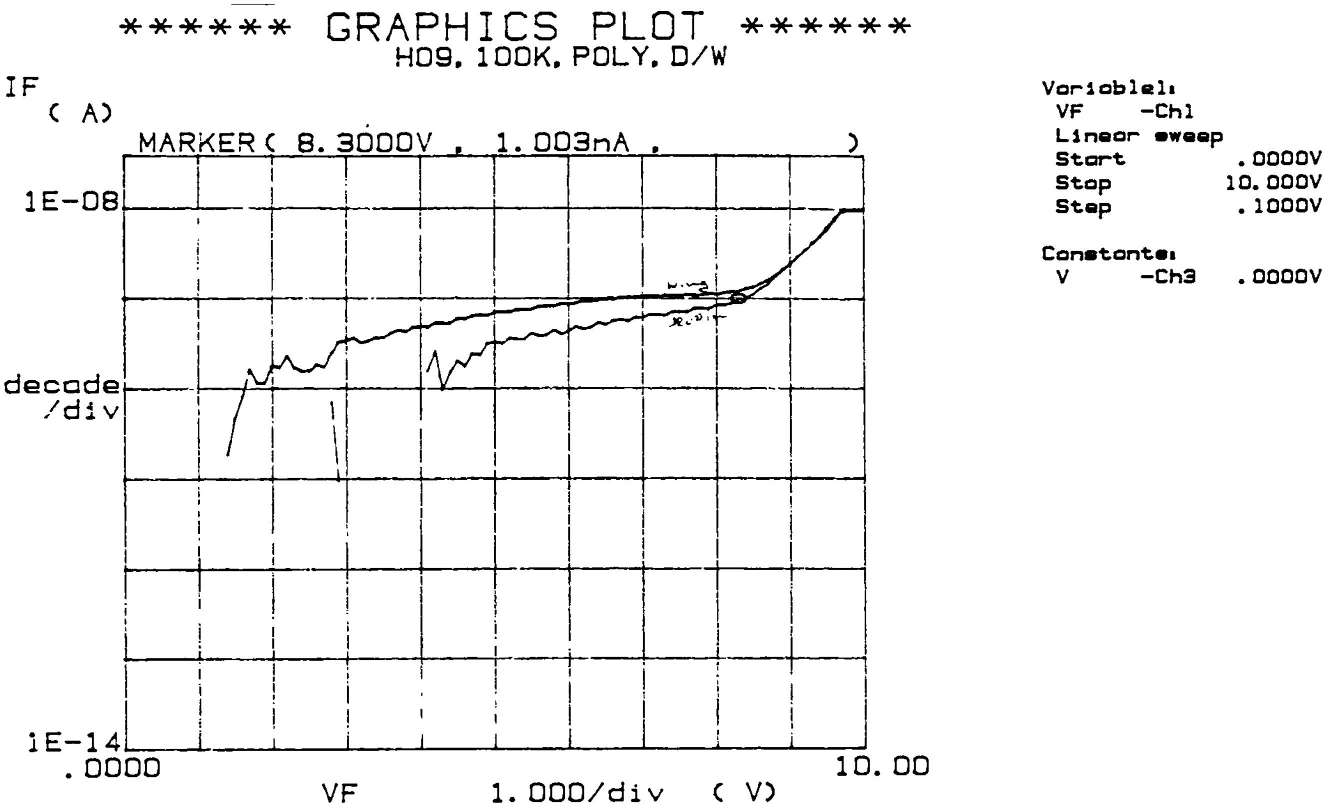
FINAL STRUCTURE



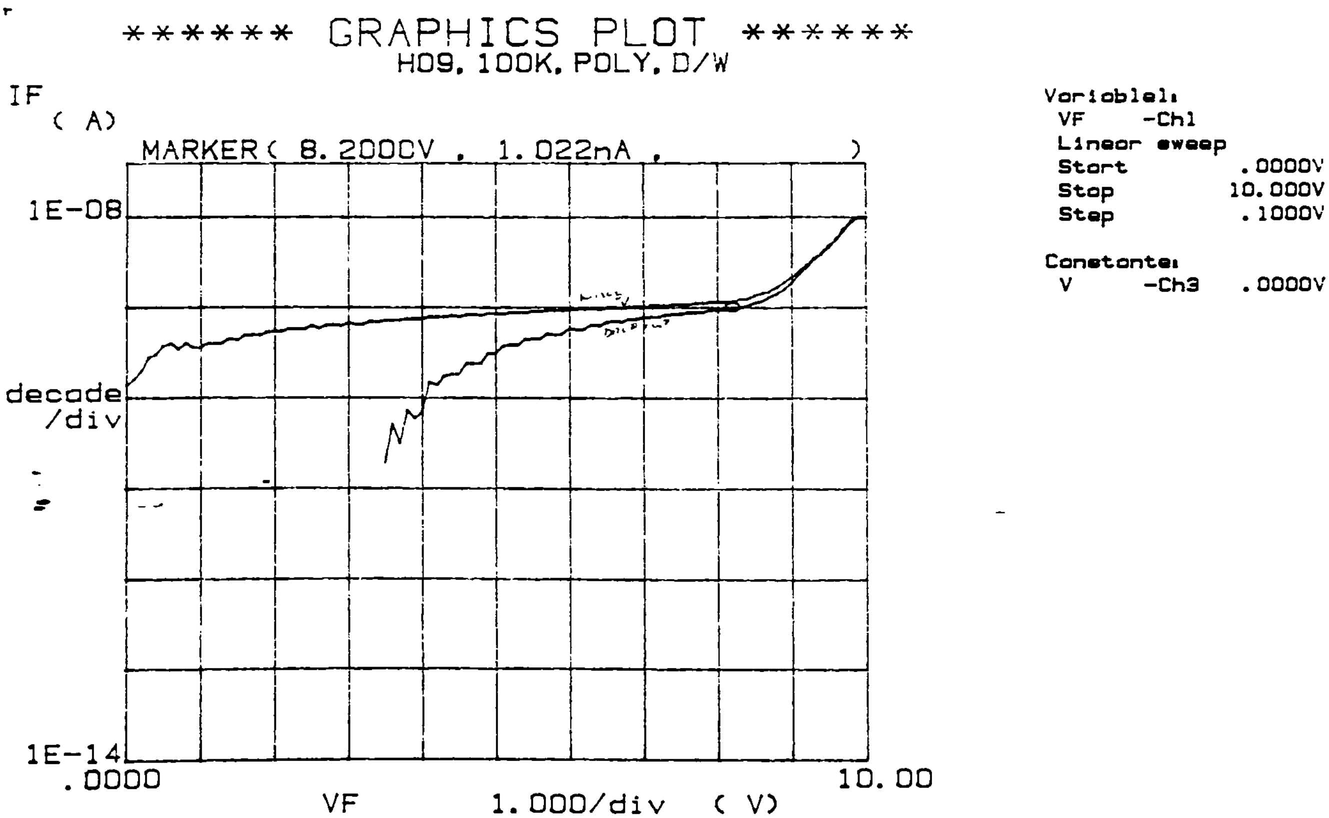
Appendix D

I(V) plots of Test devices

1500 Å Etch Back Results

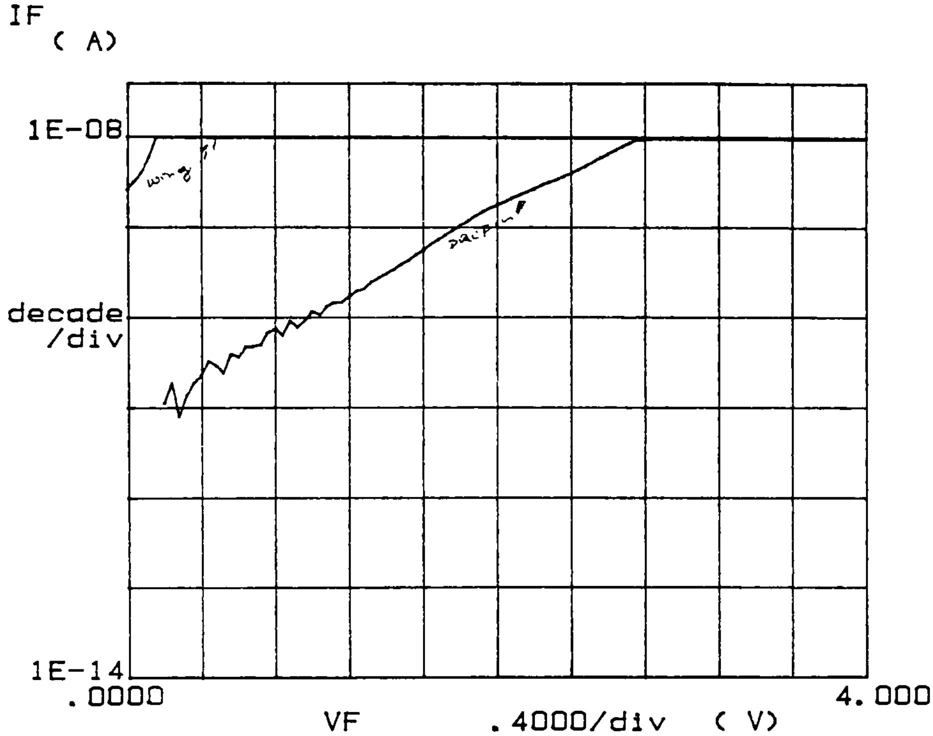


A= 10^{-3} cm^2, NO I^2
BOE ETCH BACK=1500 A



****** GRAPHICS PLOT ******

C05, 100K, AL, D/W

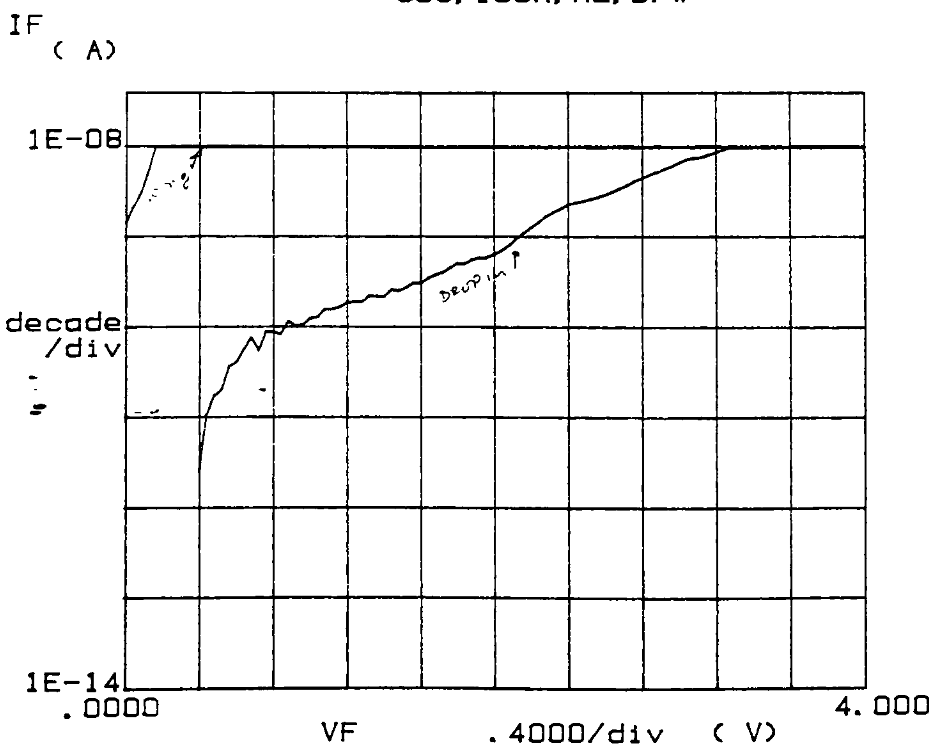


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

C05, 100K, AL, D/W

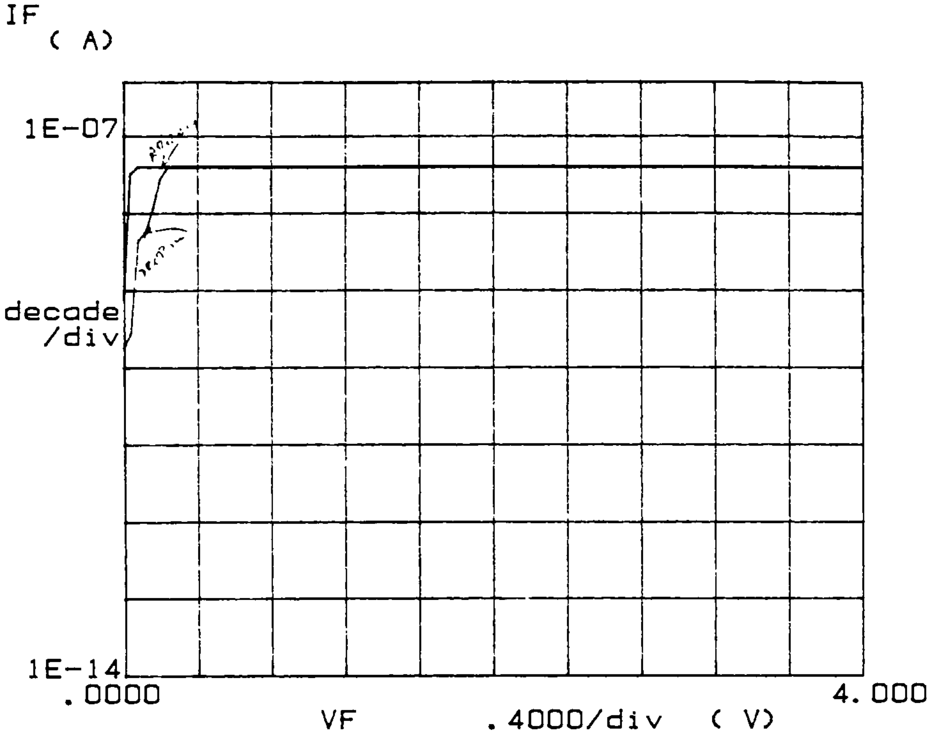


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

C05, 400K, AL, D/ARRY

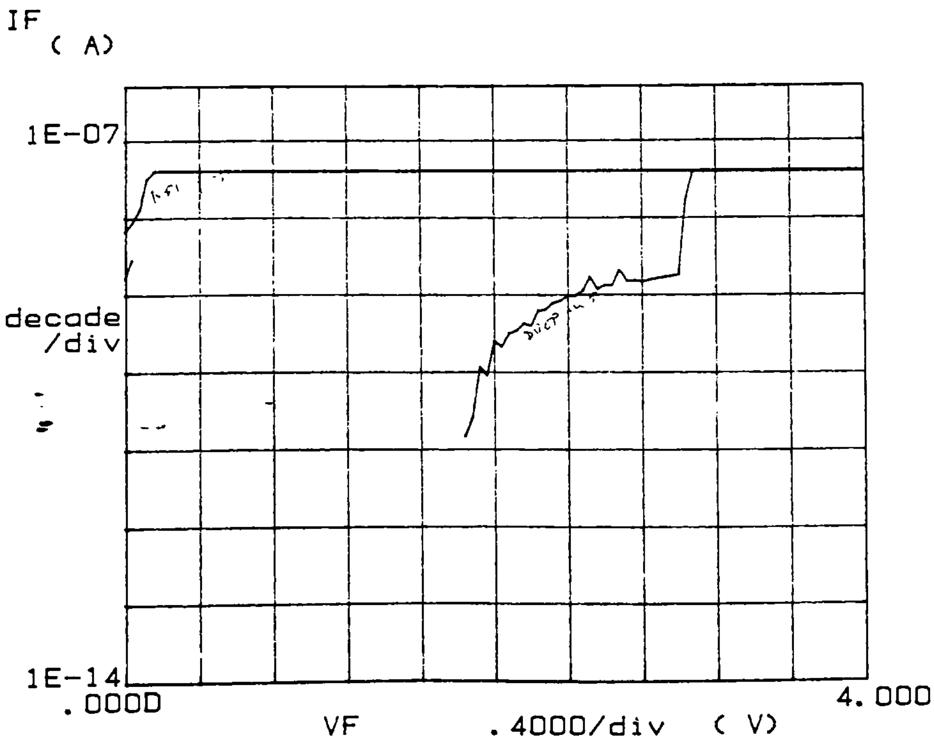


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

Constants:
V -Ch3 .0000V

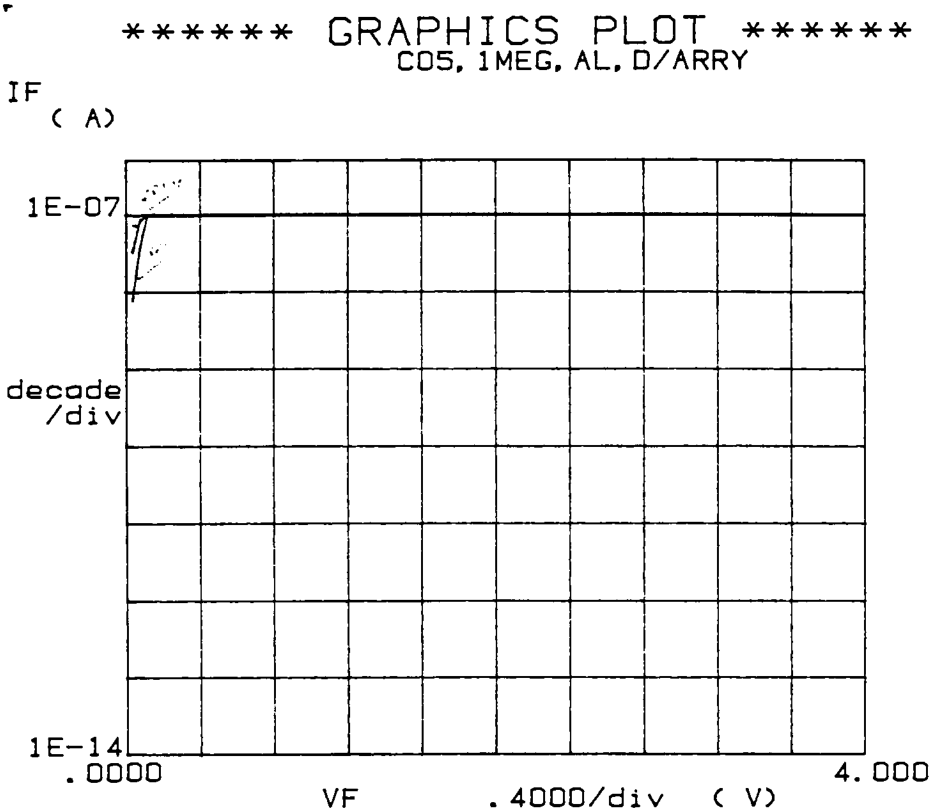
****** GRAPHICS PLOT ******

C05, 400K, AL, D/ARRY



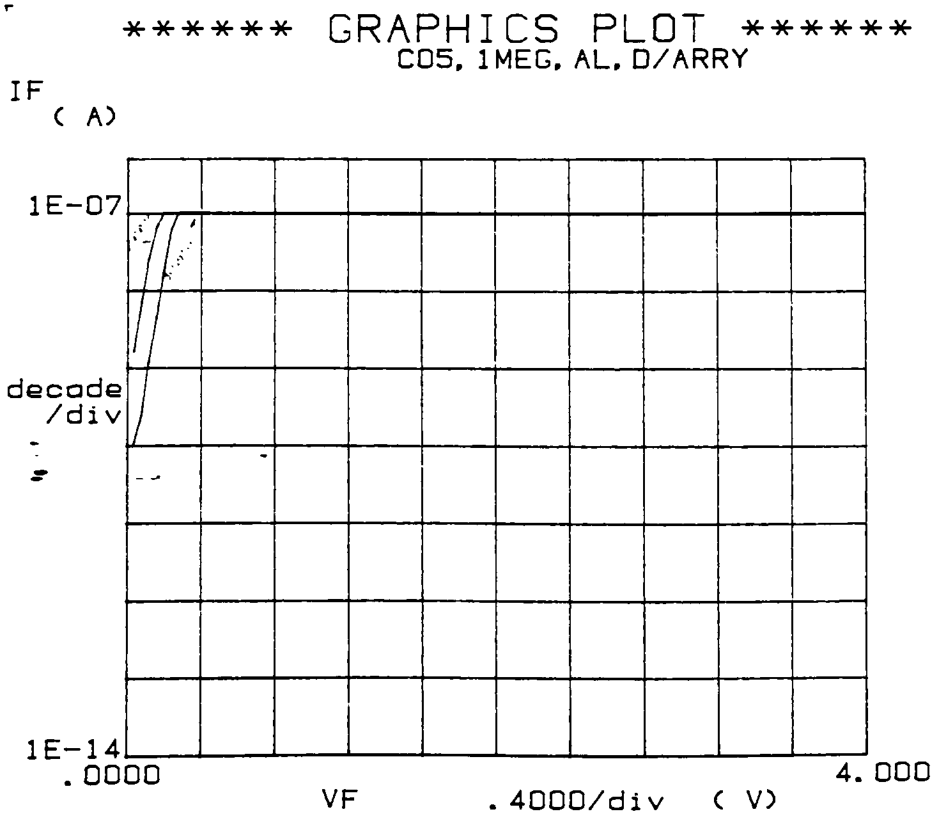
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

Constants:
V -Ch3 .0000V



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

Constants:
V -Ch3 .0000V

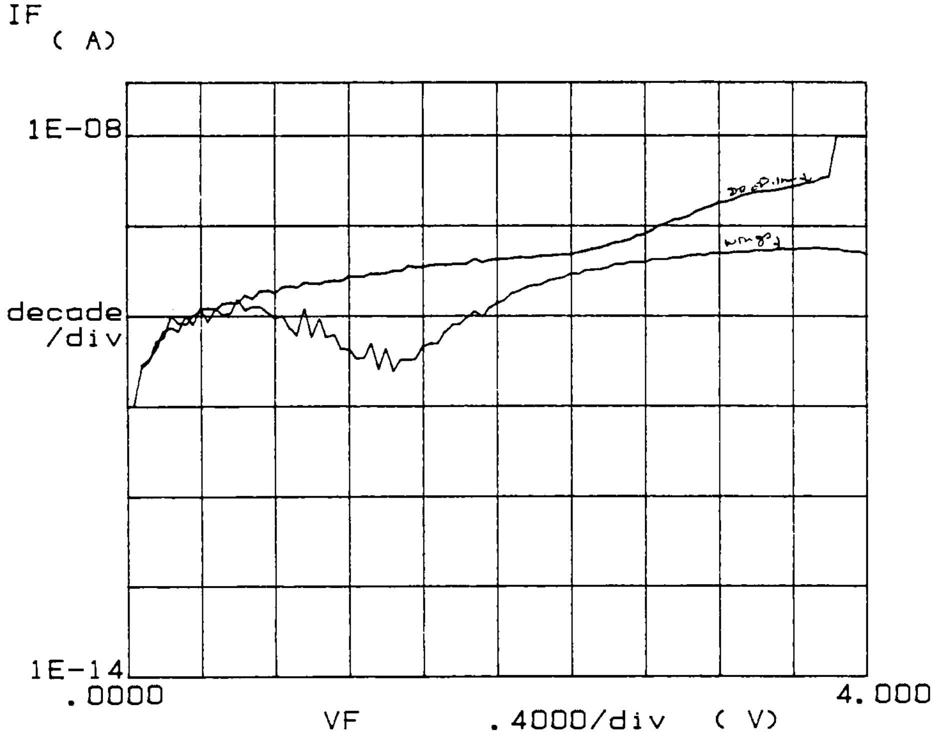


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

HO3, 100K, AL, D, W

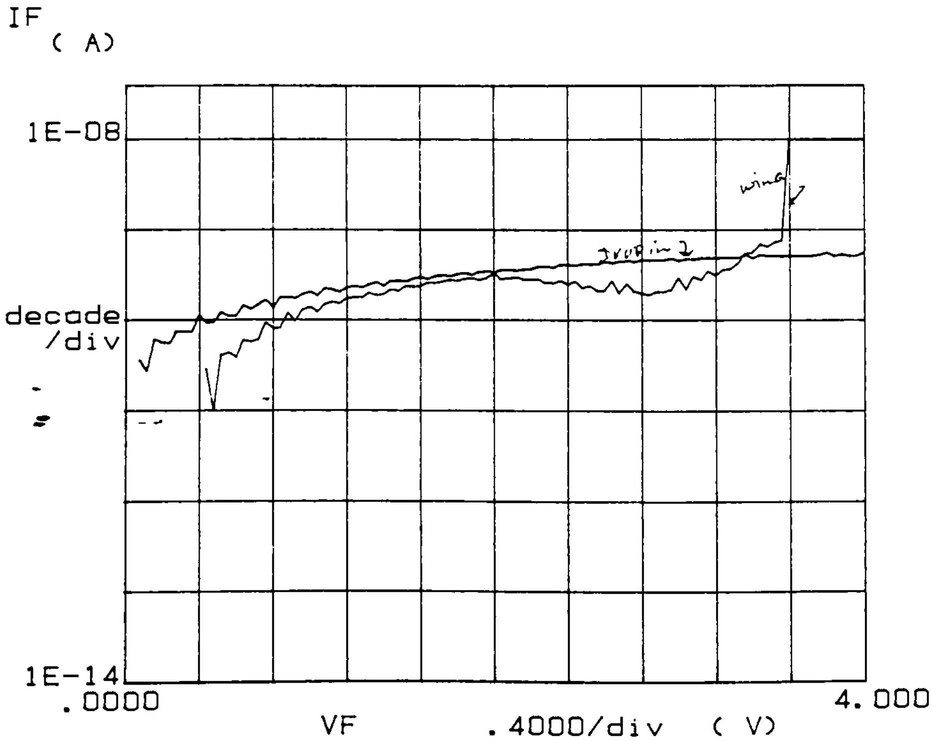


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

Constants:
V -Ch3 .0000V

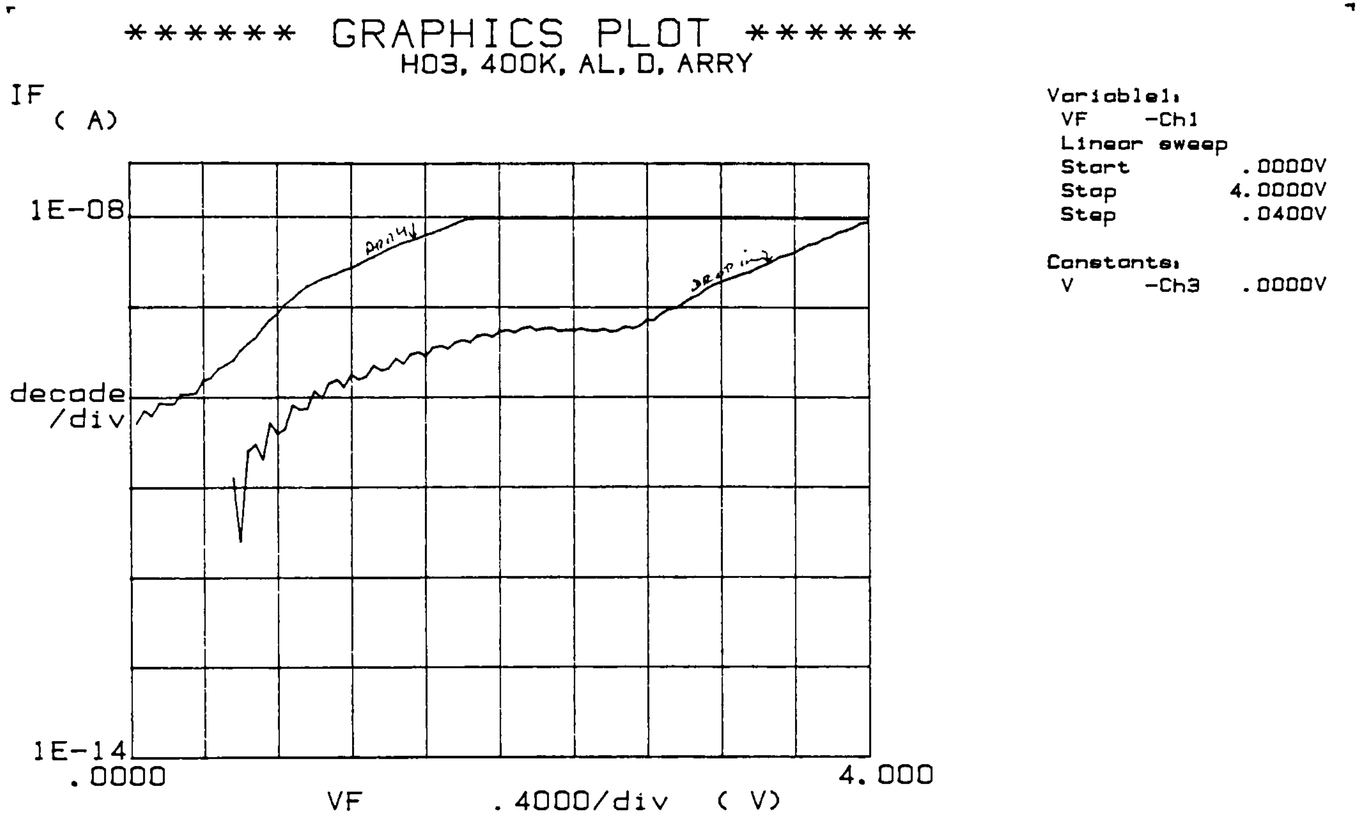
****** GRAPHICS PLOT ******

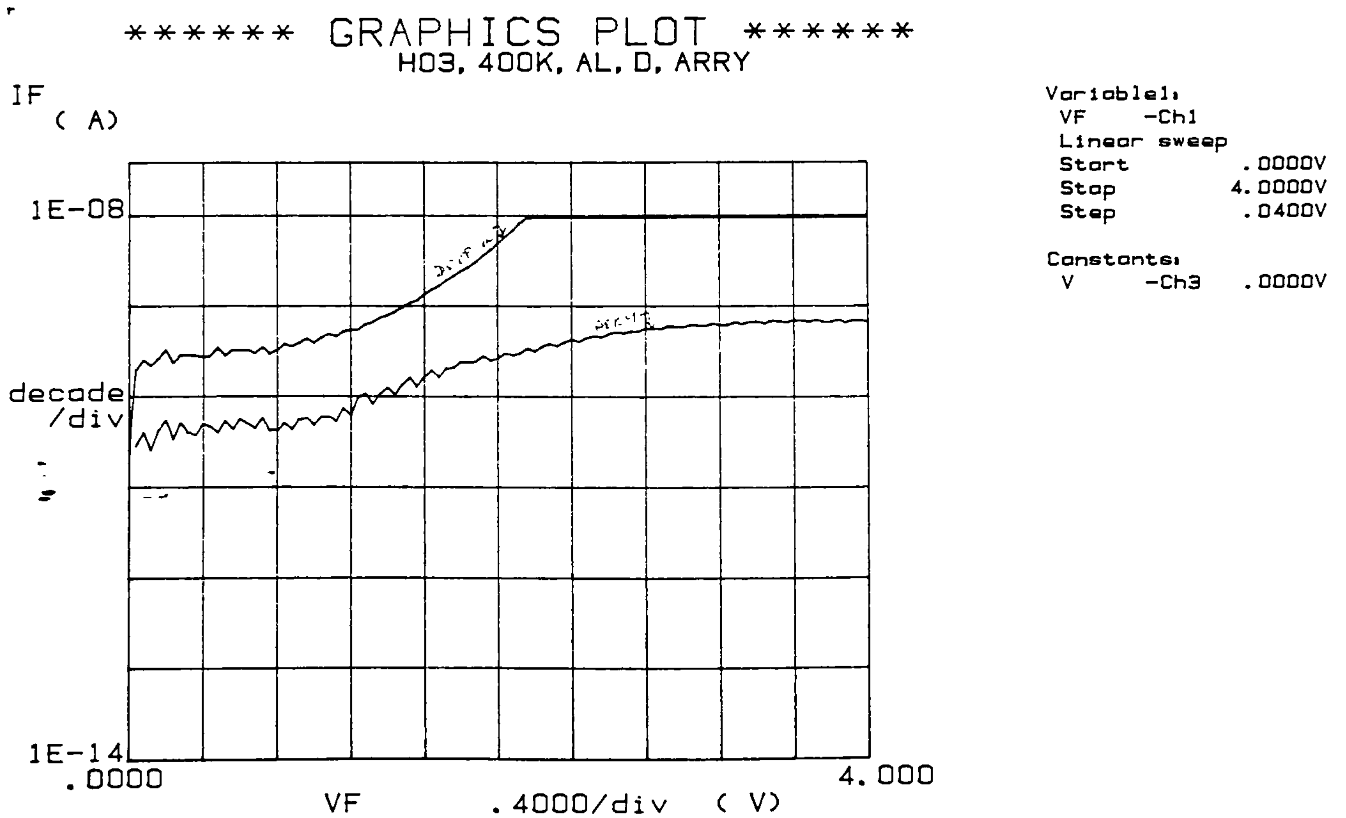
HO3, 100K, AL, D, W



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

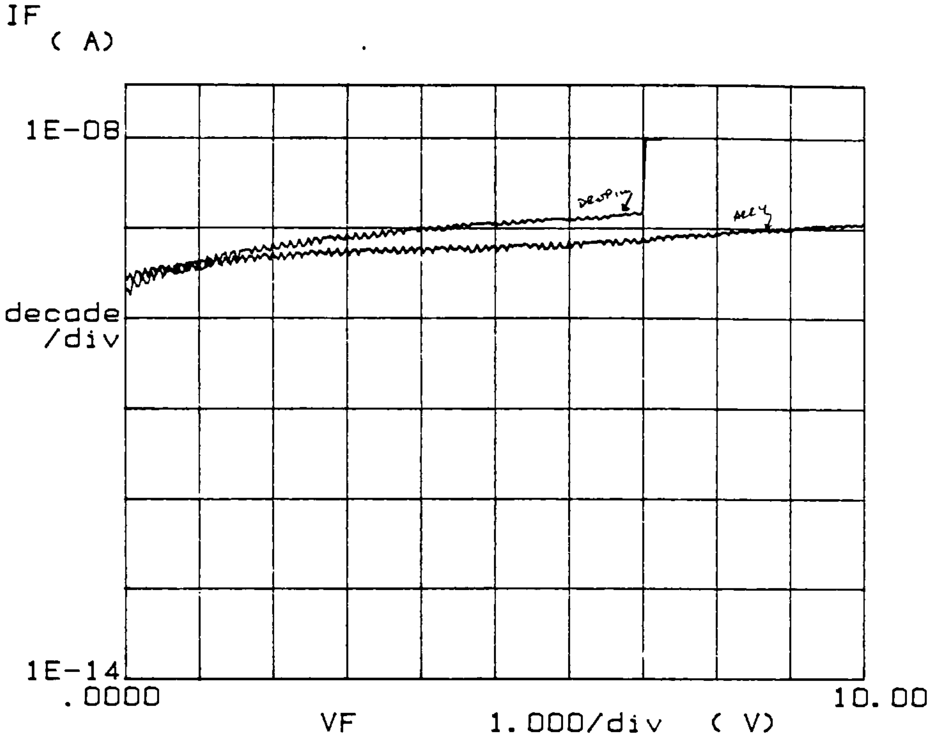
Constants:
V -Ch3 .0000V


****** GRAPHICS PLOT ******
H03, 400K, AL, D, ARRY
IF (A)
1E-08
decade /div
1E-14
.0000
4.000
VF .4000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V
Constants:
V -Ch3 .0000V


****** GRAPHICS PLOT ******
H03, 400K, AL, D, ARRY
IF (A)
1E-08
decade /div
1E-14
.0000
4.000
VF .4000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V
Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

H03, 1MEG, AL, D, ARRY

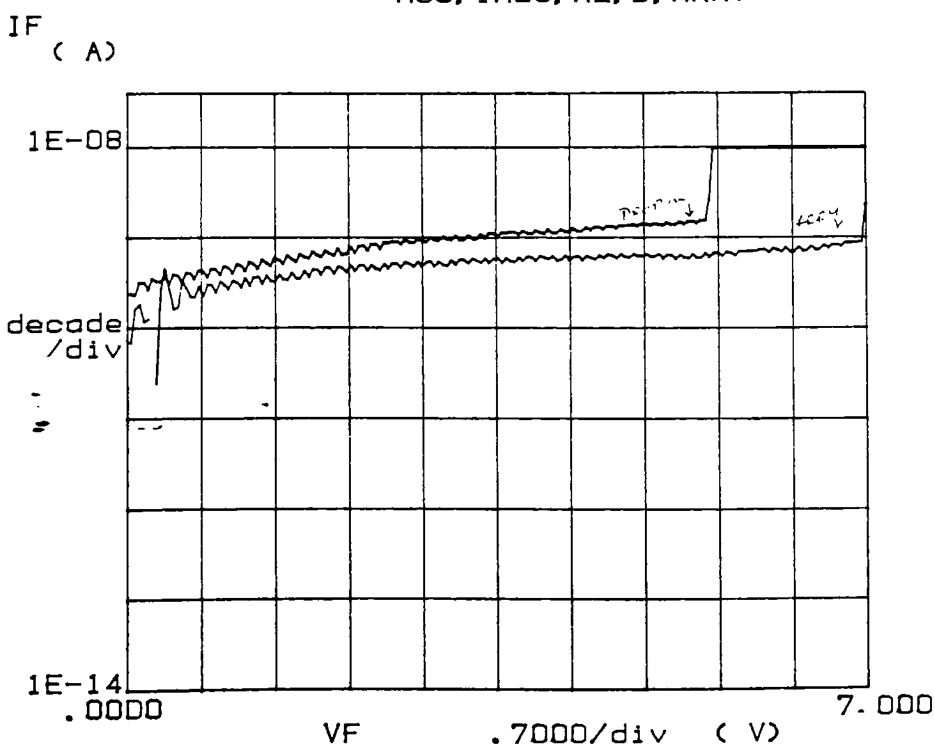


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .0400V

Constants:
V -Ch3 .0000V

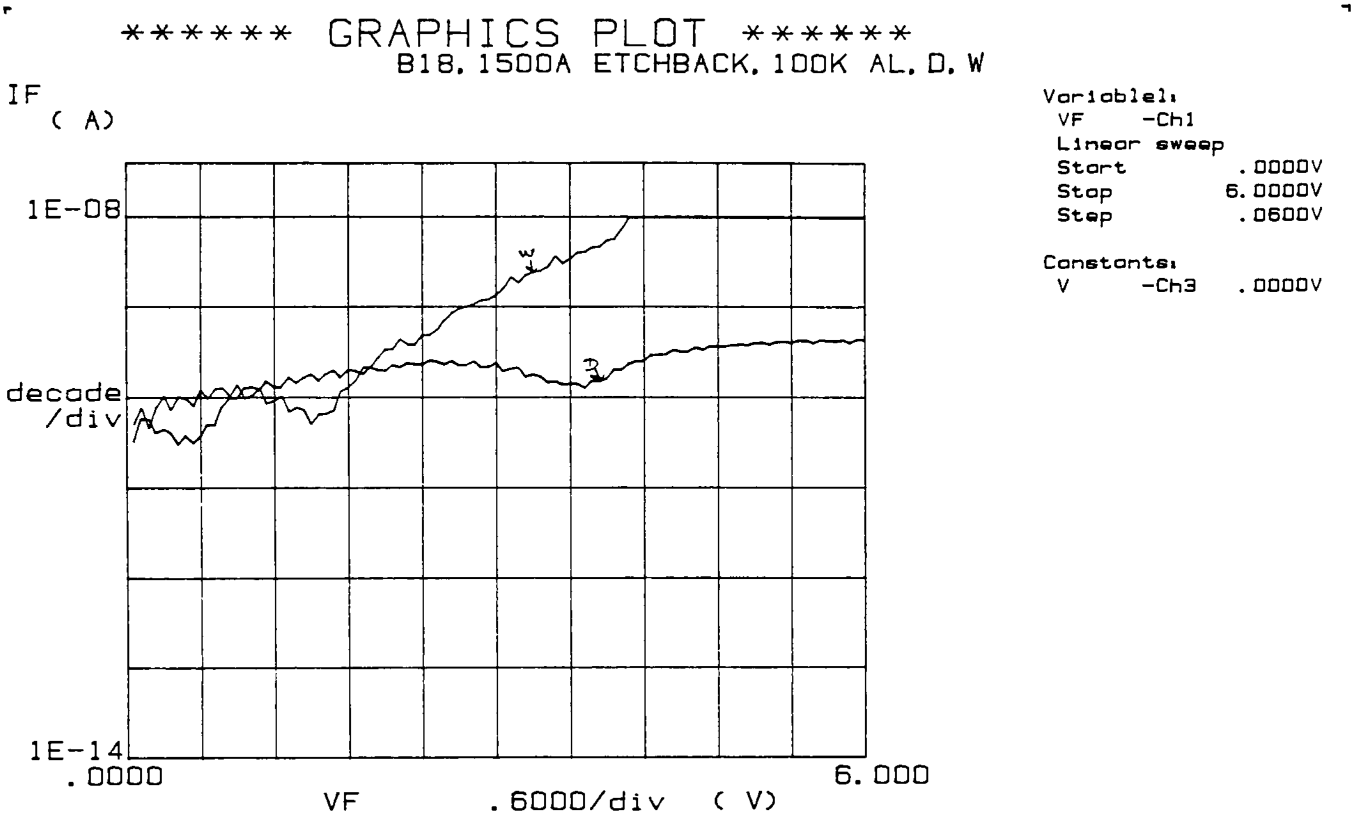
****** GRAPHICS PLOT ******

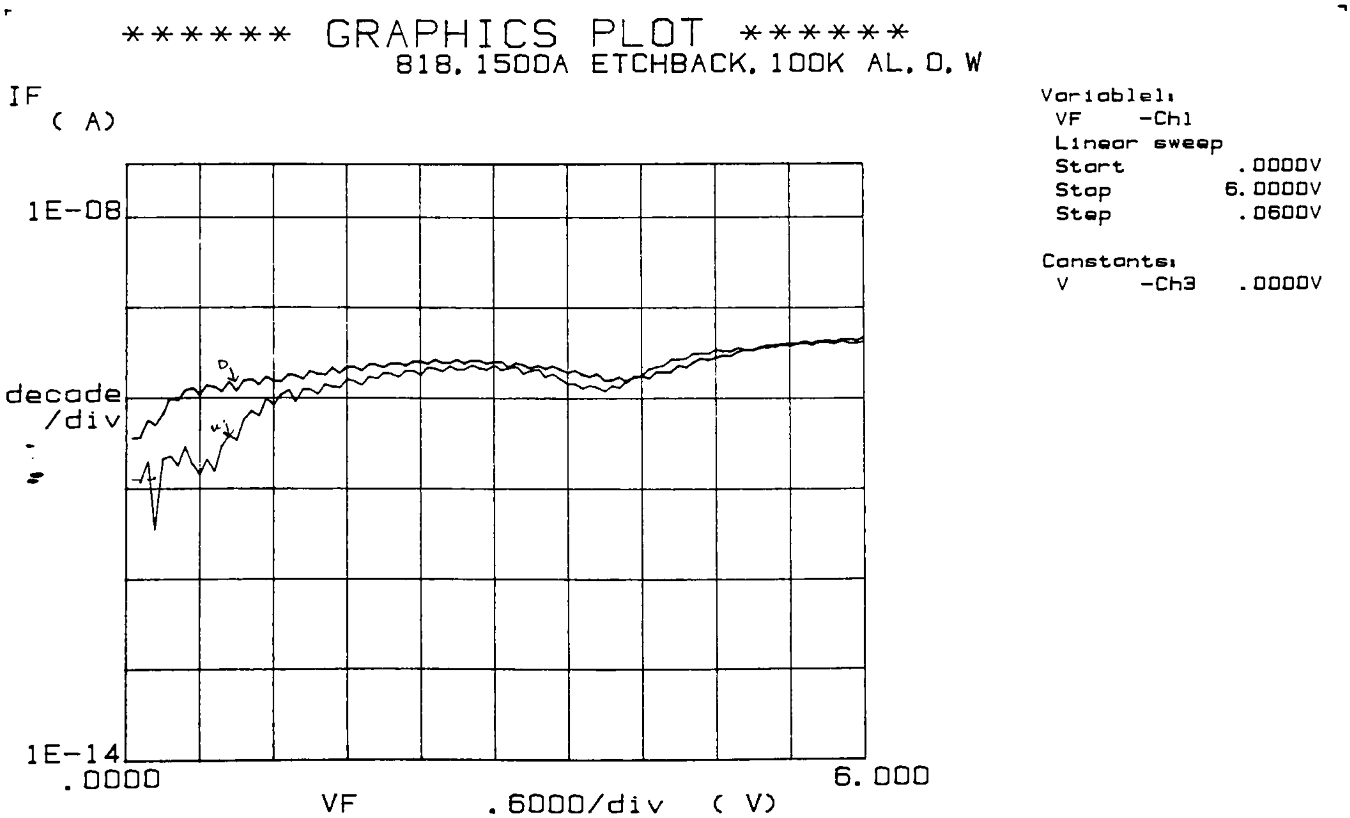
H03, 1MEG, AL, D, ARRY



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 7.0000V
Step .0400V

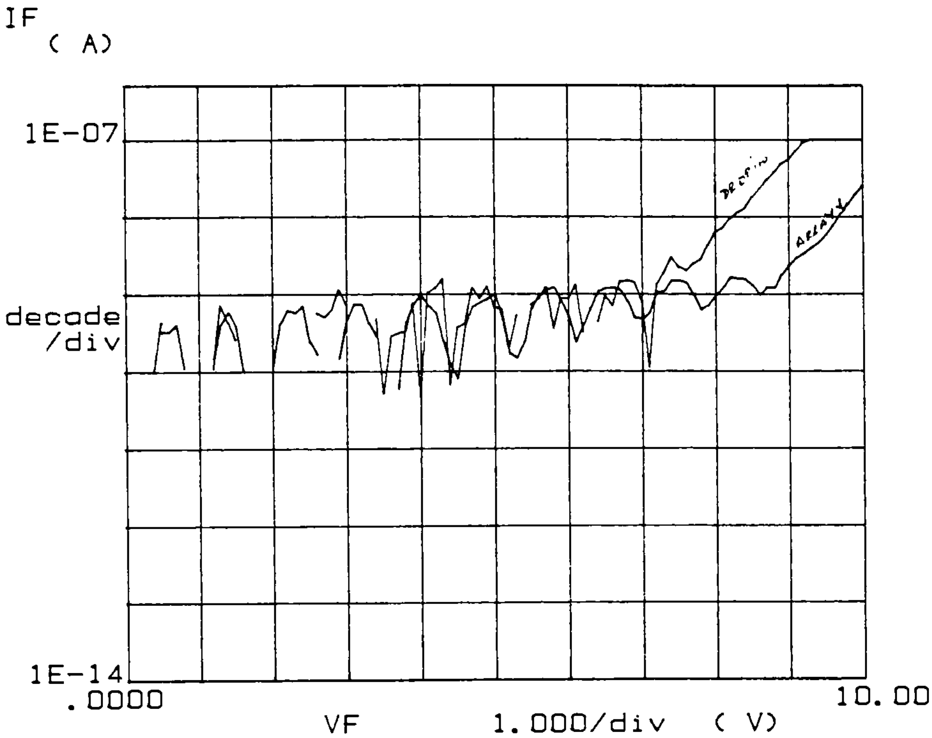
Constants:
V -Ch3 .0000V


****** GRAPHICS PLOT ******
818, 1500A ETCHBACK, 100K AL, D, W
IF (A)
1E-08
decade /div
1E-14
.0000
6.000
VF .6000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 6.0000V
Step .0600V
Constants:
V -Ch3 .0000V


****** GRAPHICS PLOT ******
818, 1500A ETCHBACK, 100K AL, D, W
IF (A)
1E-08
decade /div
1E-14
.0000
6.000
VF .6000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 6.0000V
Step .0600V
Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B18, 1500A ETCHBACK, 400K AL, D, A

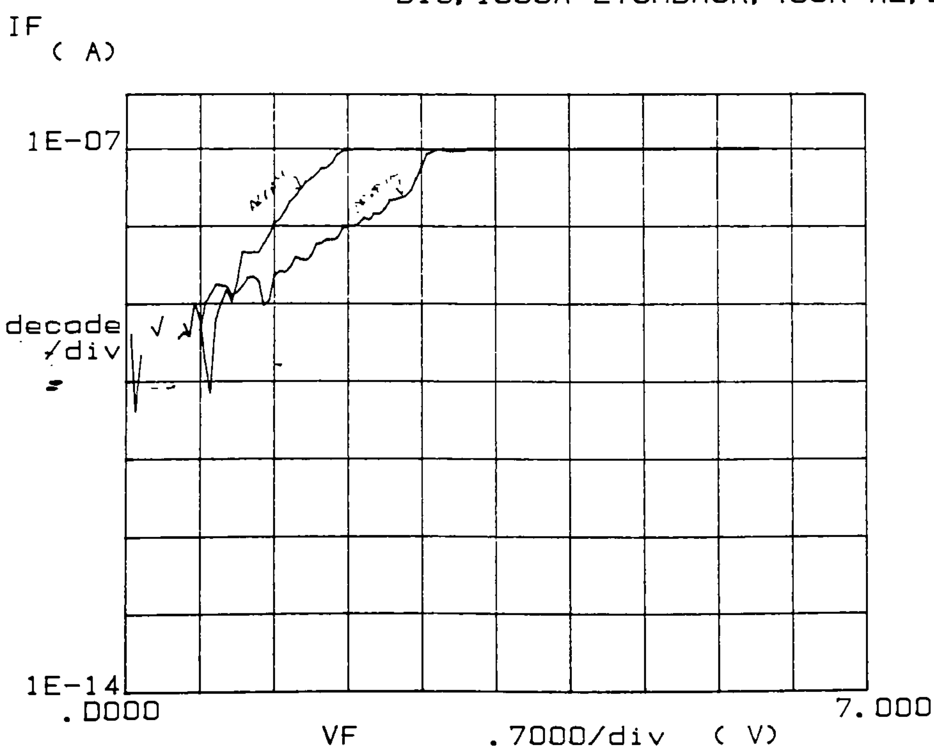


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B18, 1500A ETCHBACK, 400K AL, D, A

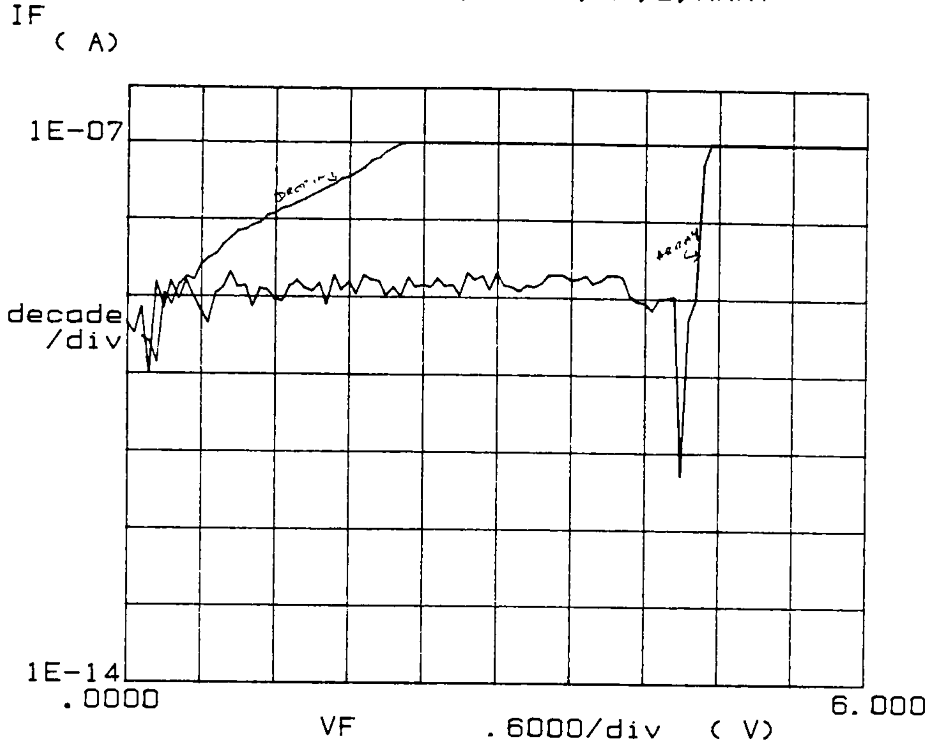


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 6.0000V
Step .0500V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B18, 1 MEG, AL, D, ARRY

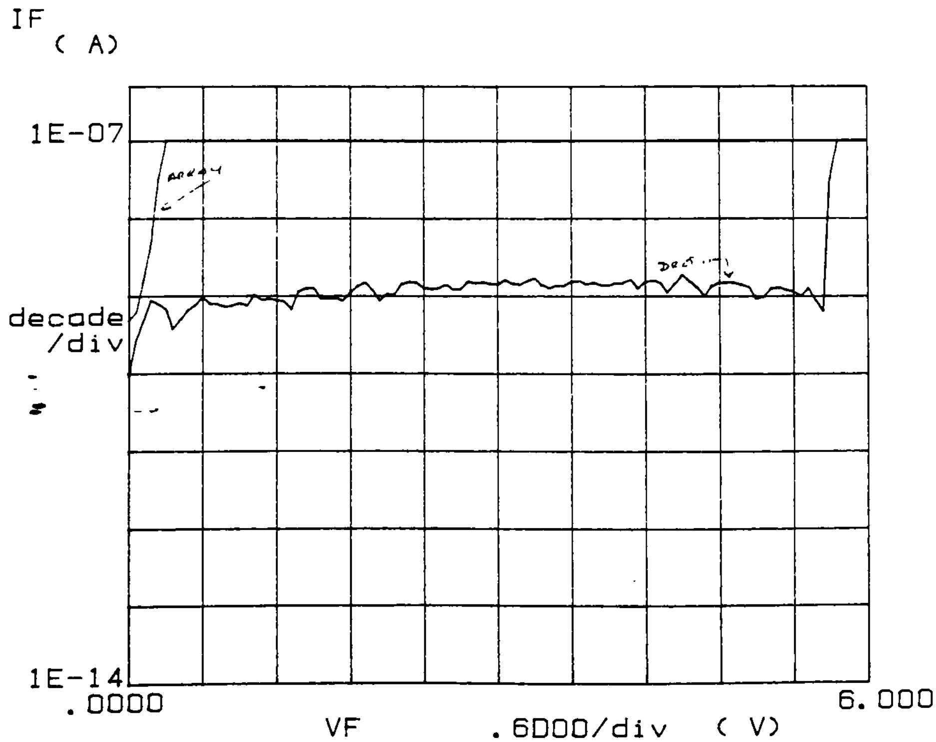


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 6.0000V
Step .0600V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B18, 1 MEG, AL, D, ARRY

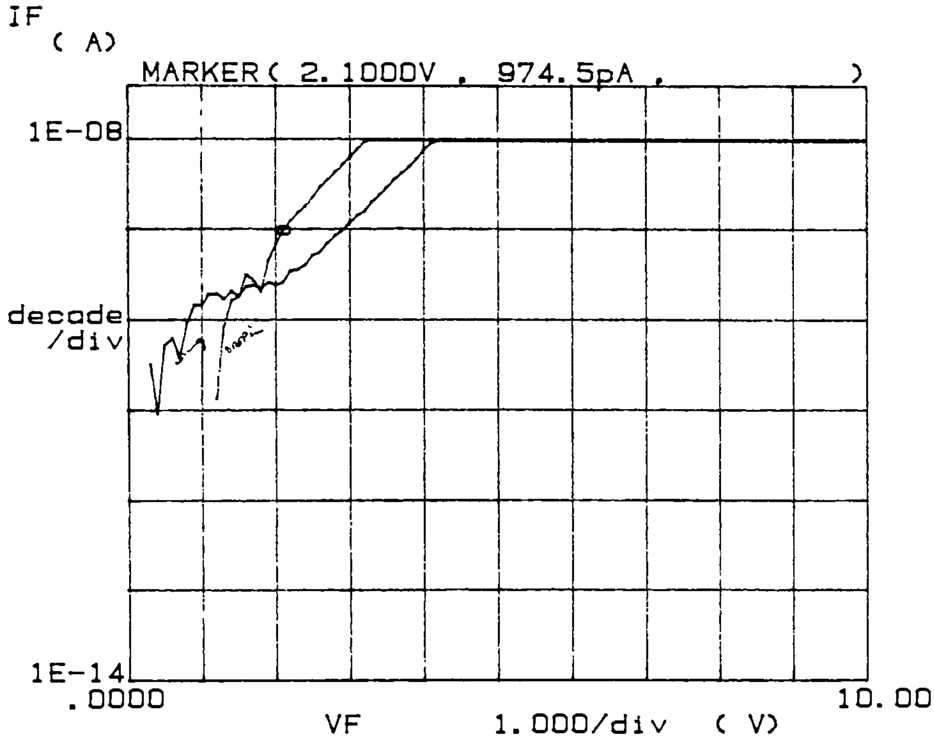


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 6.0000V
Step .0600V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

CD4, 100K, POLY, D/W

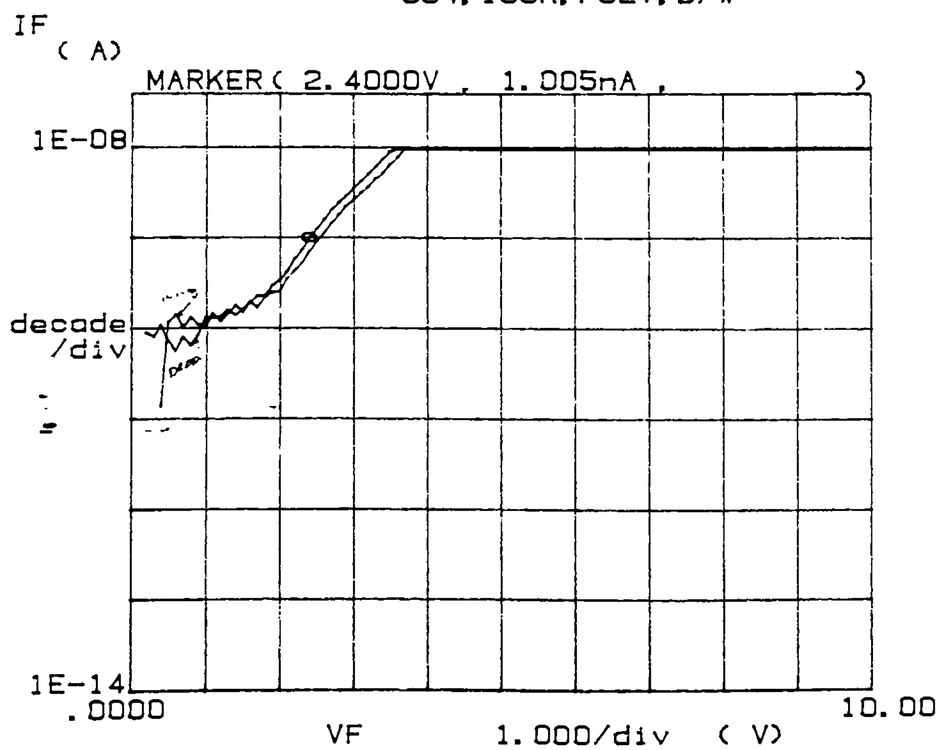


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

CD4, 100K, POLY, D/W

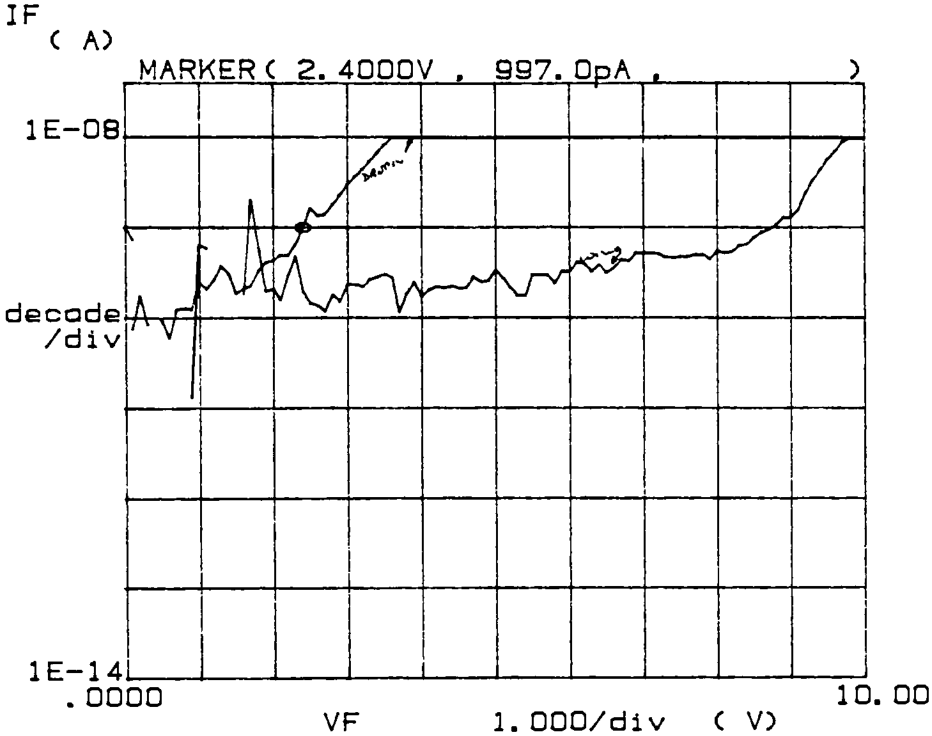


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

CO4, 100K, POLY, D/W

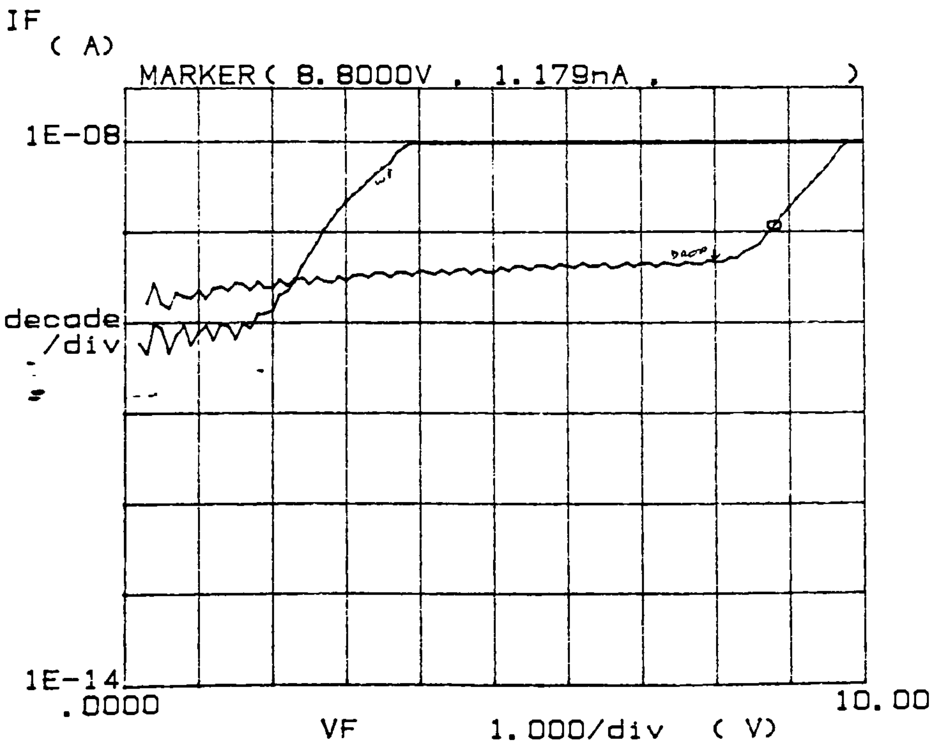


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

CO4, 100K, POLY, D/W

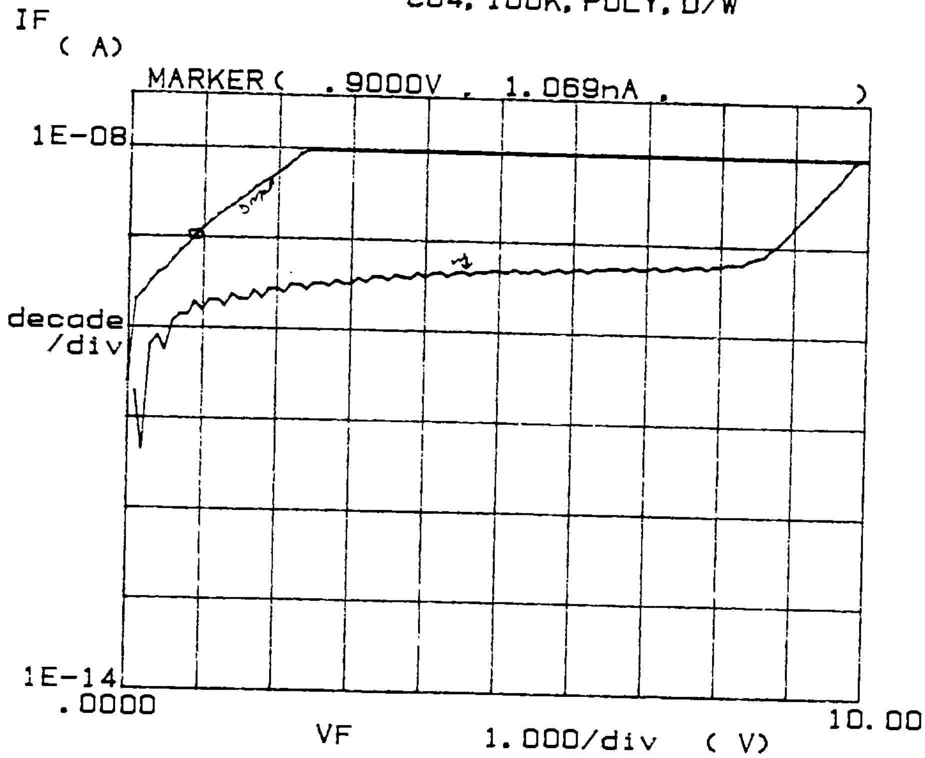


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

C04, 100K, POLY, D/W

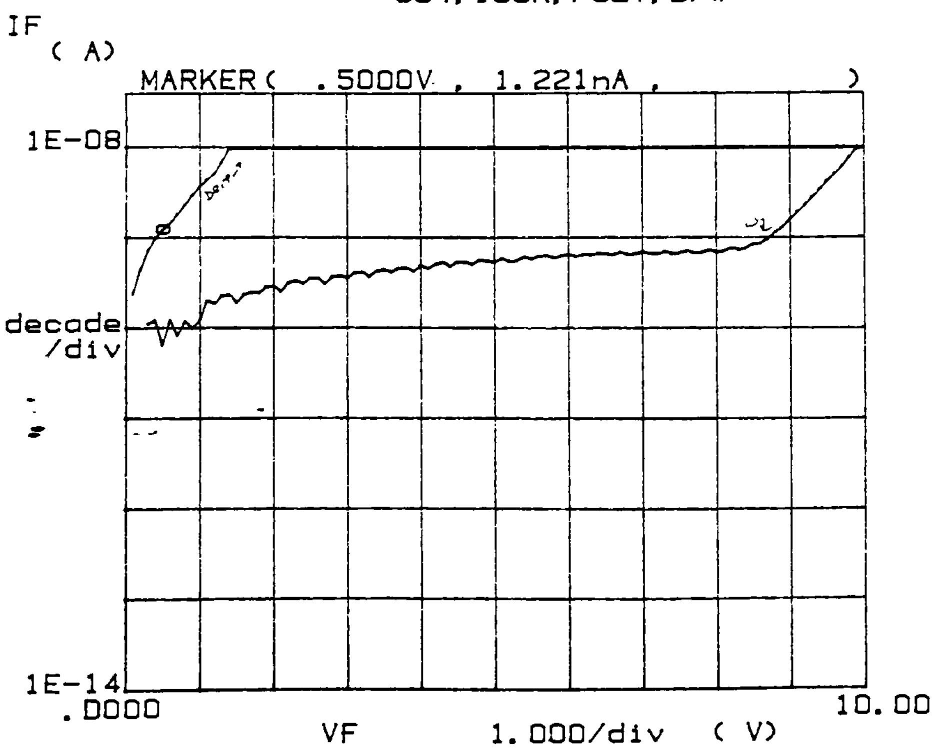


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

C04, 100K, POLY, D/W

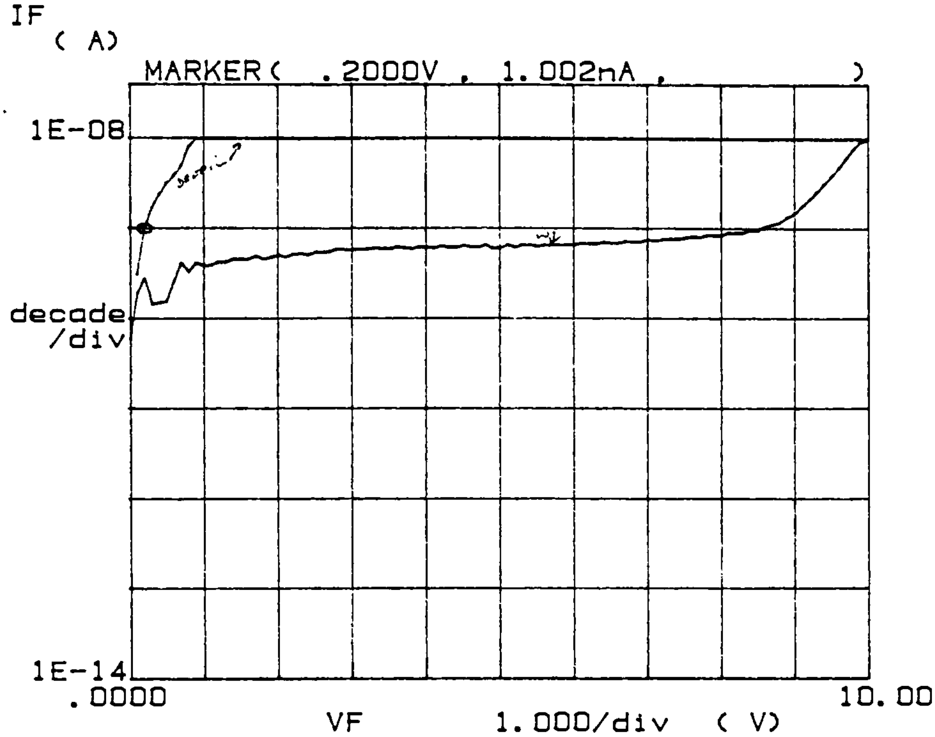


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

CO4, 100K, POLY, D/W

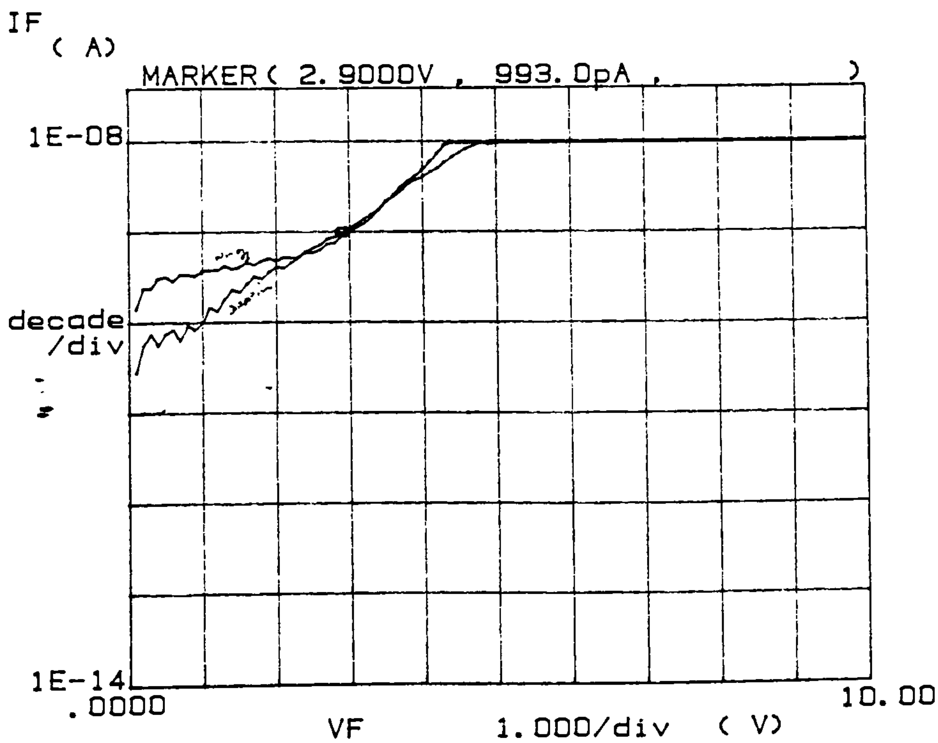


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

CO4, 100K, POLY, D/W

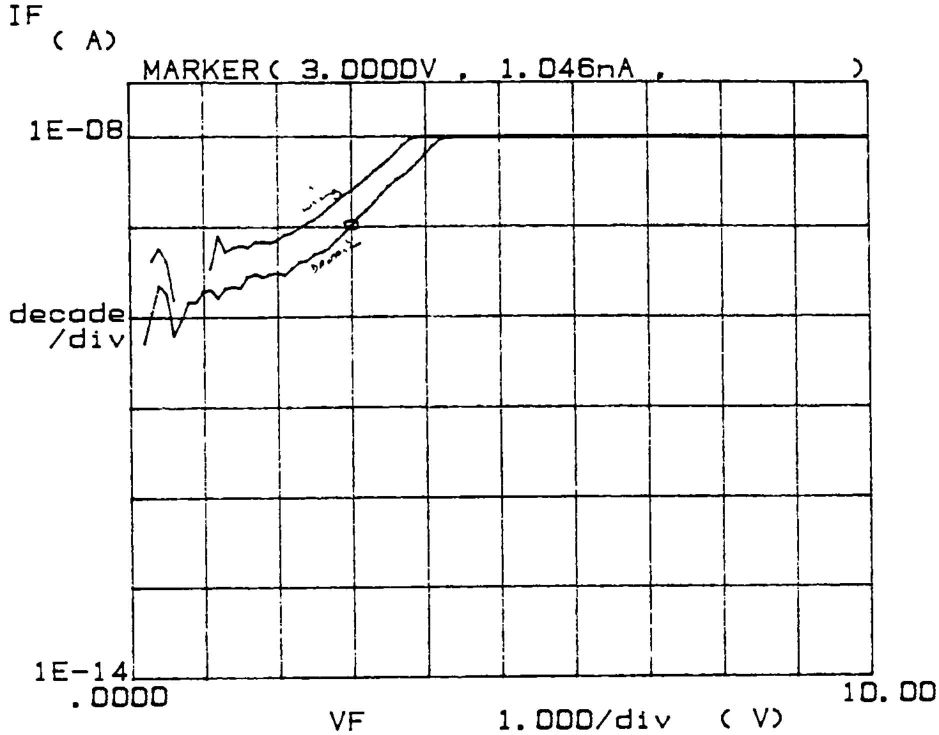


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

CD4, 100K, POLY, D/W

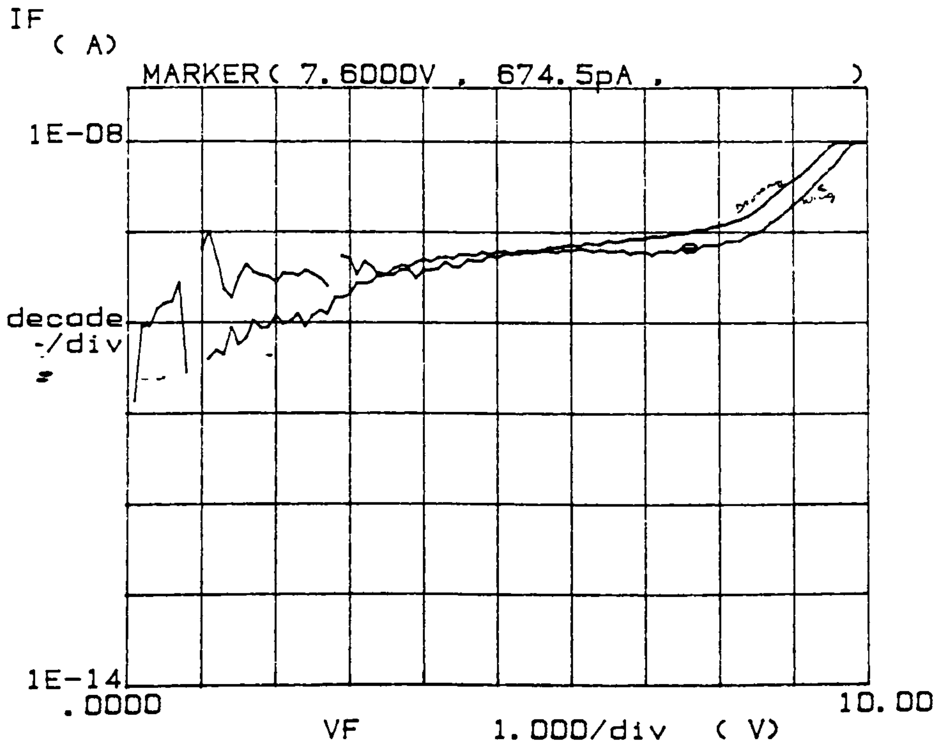


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

CD4, 100K, POLY, D/W

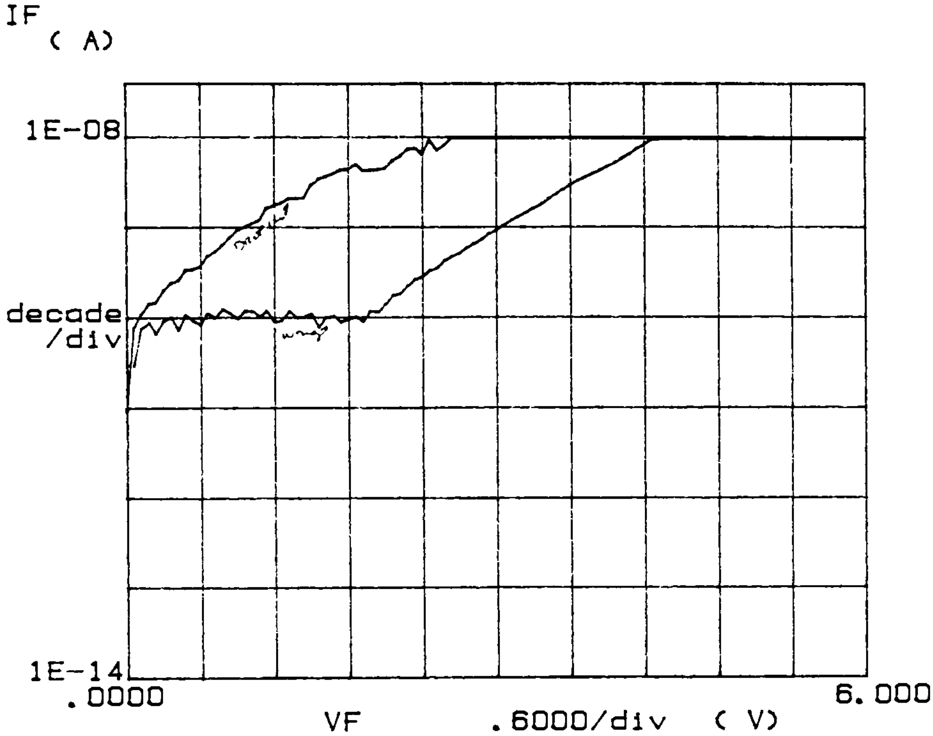


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

CO4, 100K, POLY, D/W

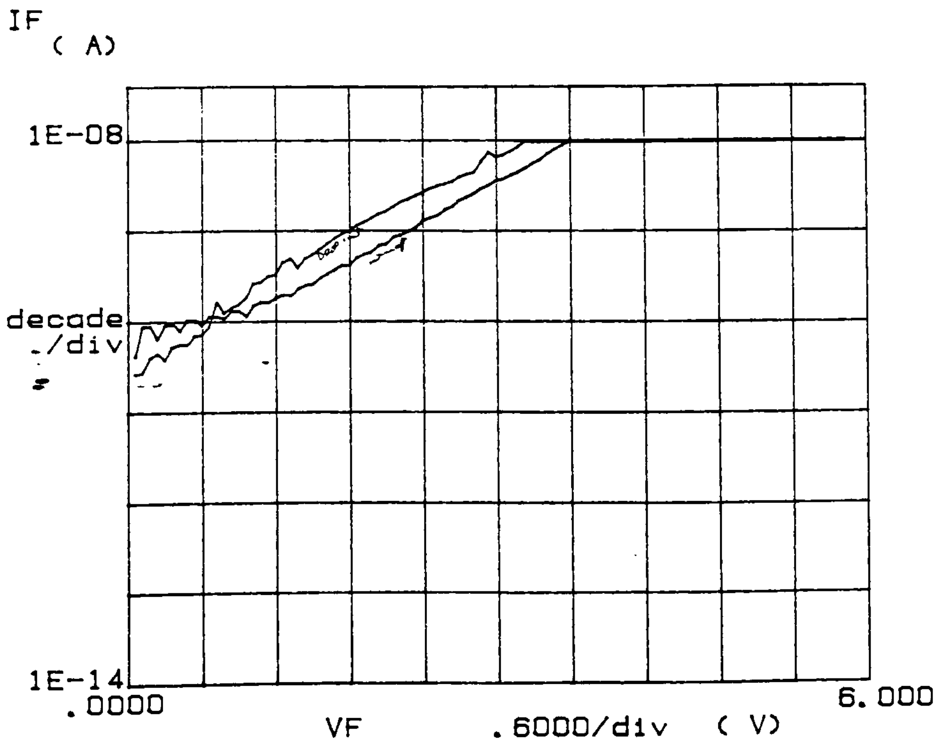


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 6.0000V
Step .0600V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

CO4, 100K, POLY, D/W

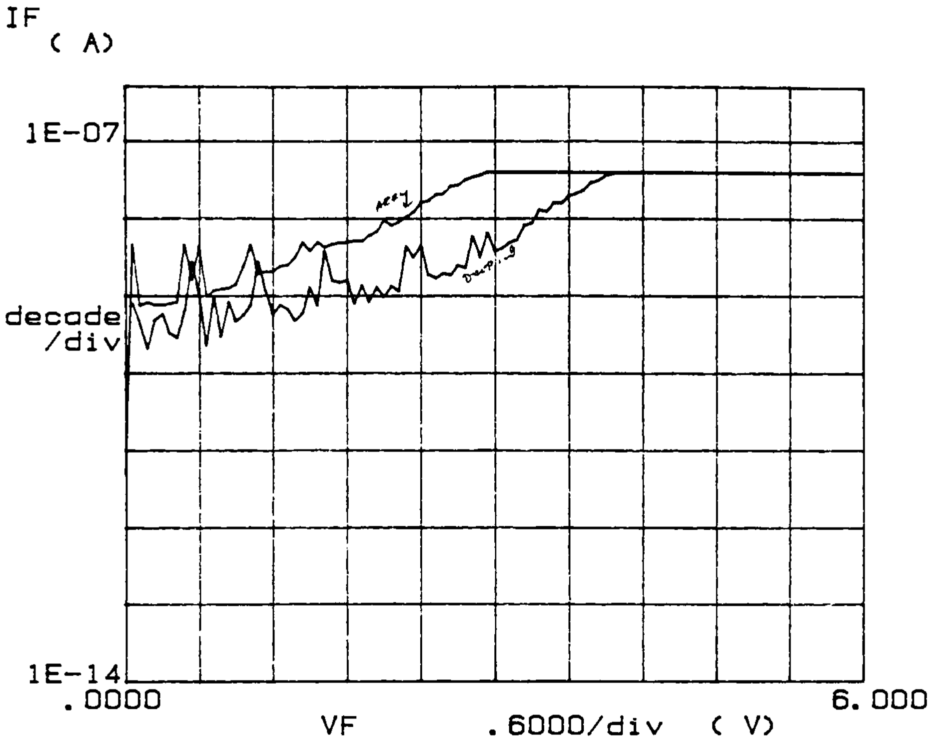


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 6.0000V
Step .0600V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

C04, 400K, POLY, D/ARRY

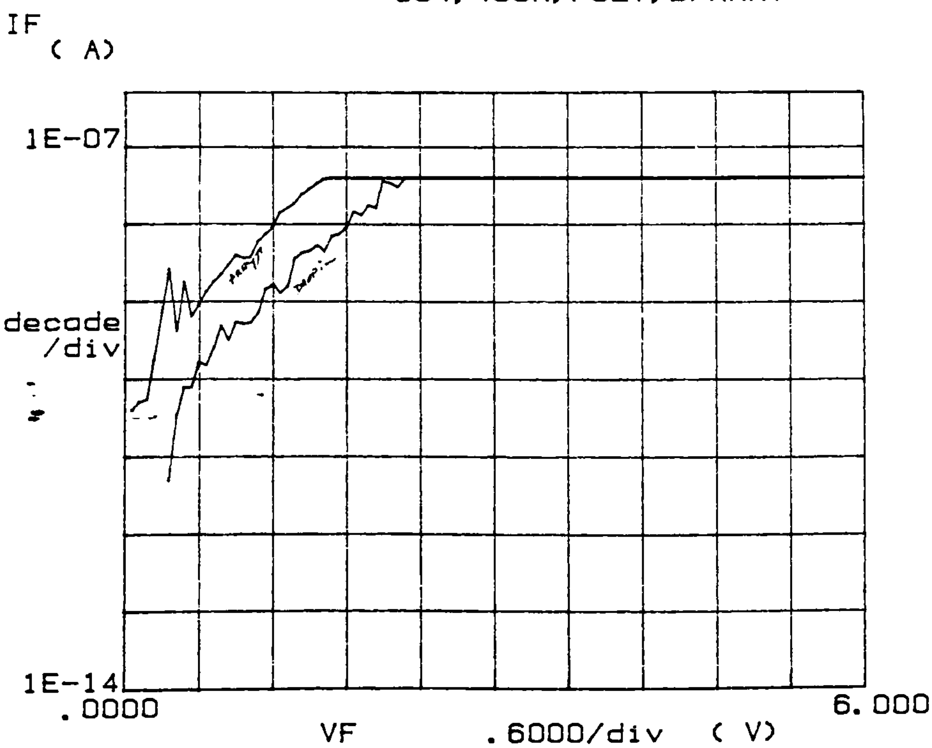


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 6.0000V
Step .0600V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

C04, 400K, POLY, D/ARRY

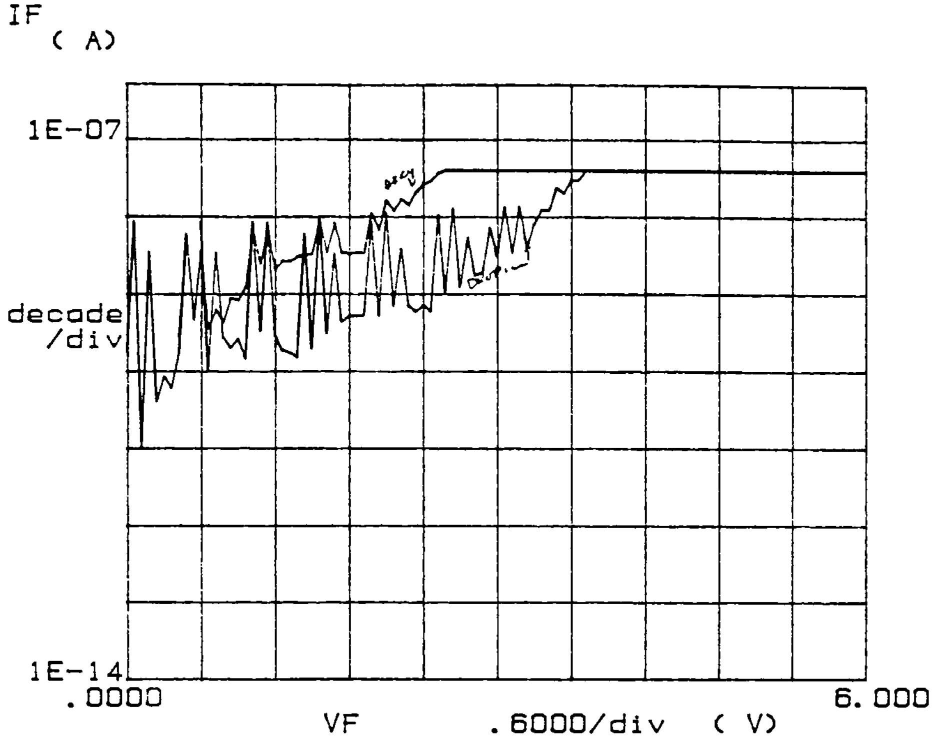


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 6.0000V
Step .0600V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

CO4, 1MEG, POLY, D/ARRY

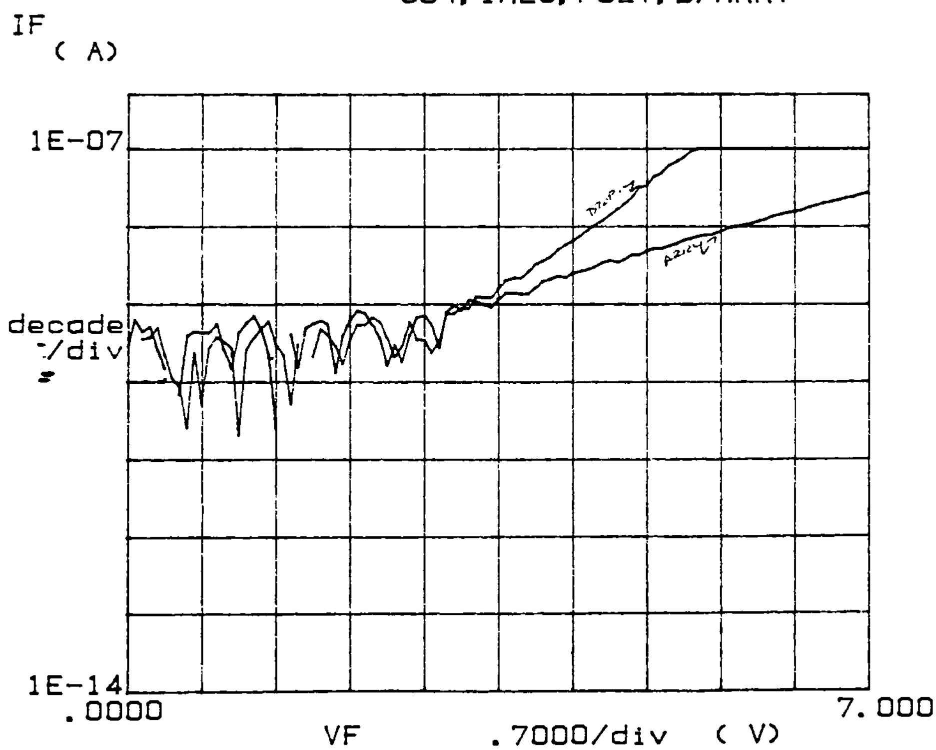


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 6.0000V
Step .0600V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

CO4, 1MEG, POLY, D/ARRY

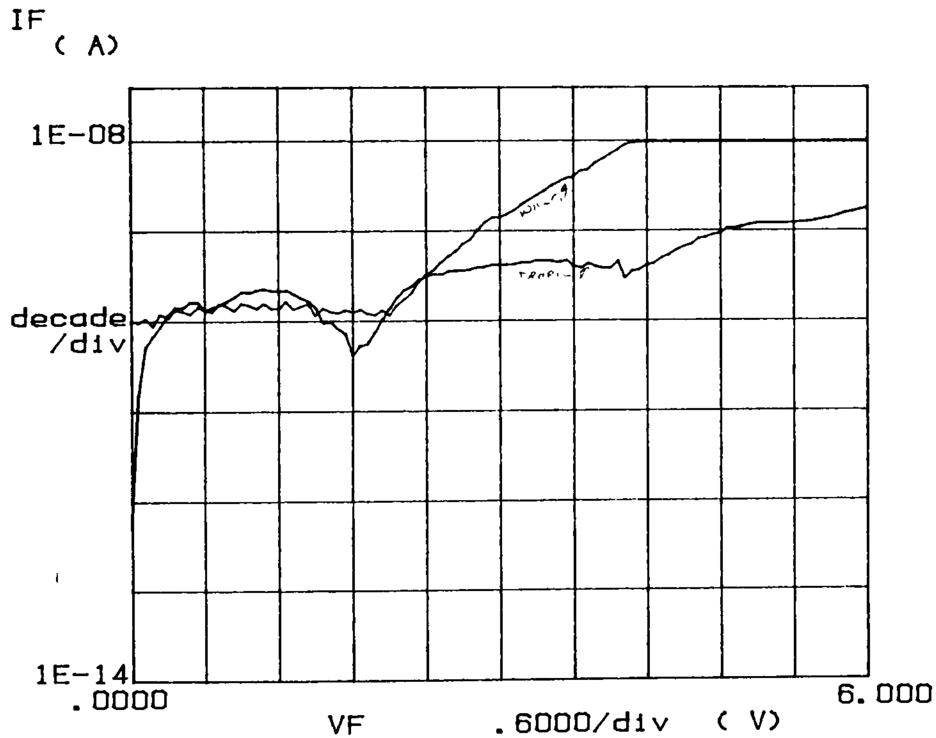


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 7.0000V
Step .0700V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B05, 100K, POLY, D/W

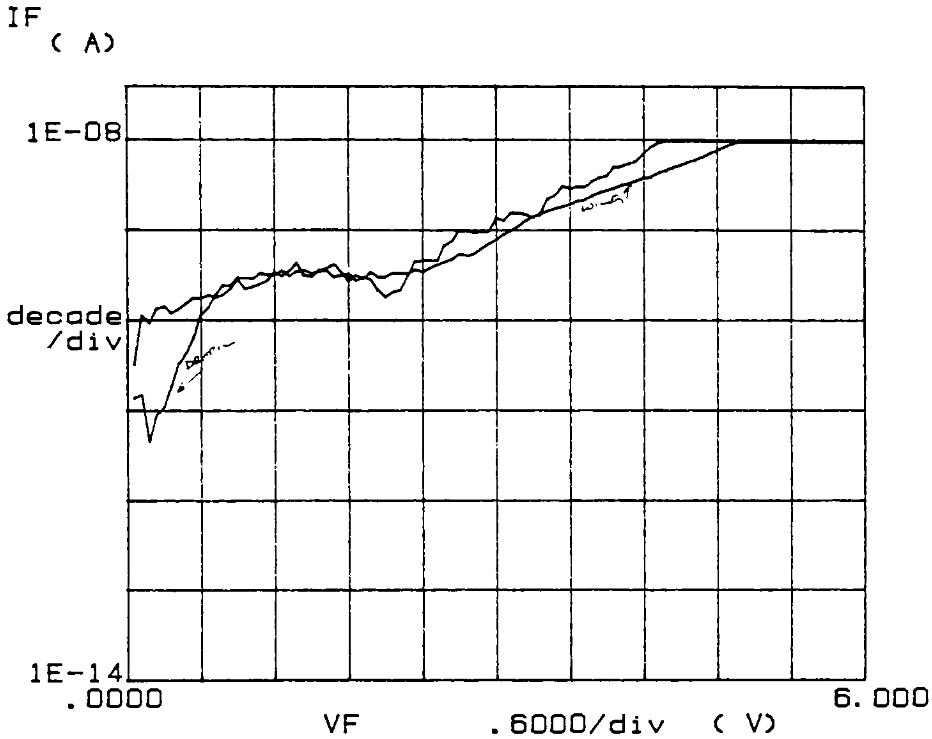


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 6.0000V
Step .0600V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B05, 100K, POLY, D/W

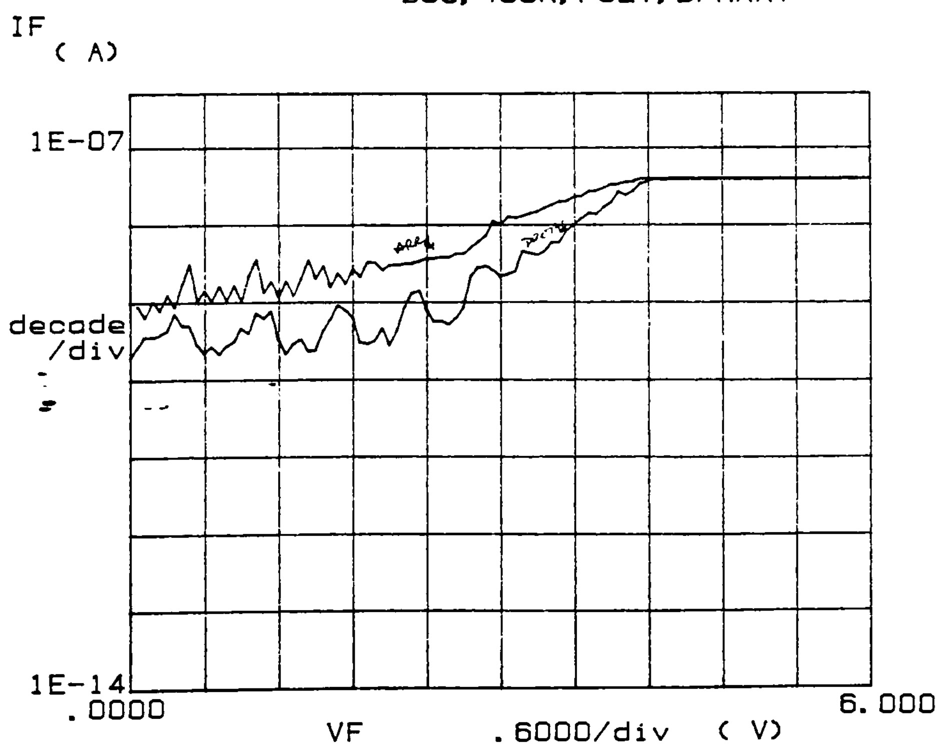


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 6.0000V
Step .0600V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B05, 400K, POLY, D/ARRY

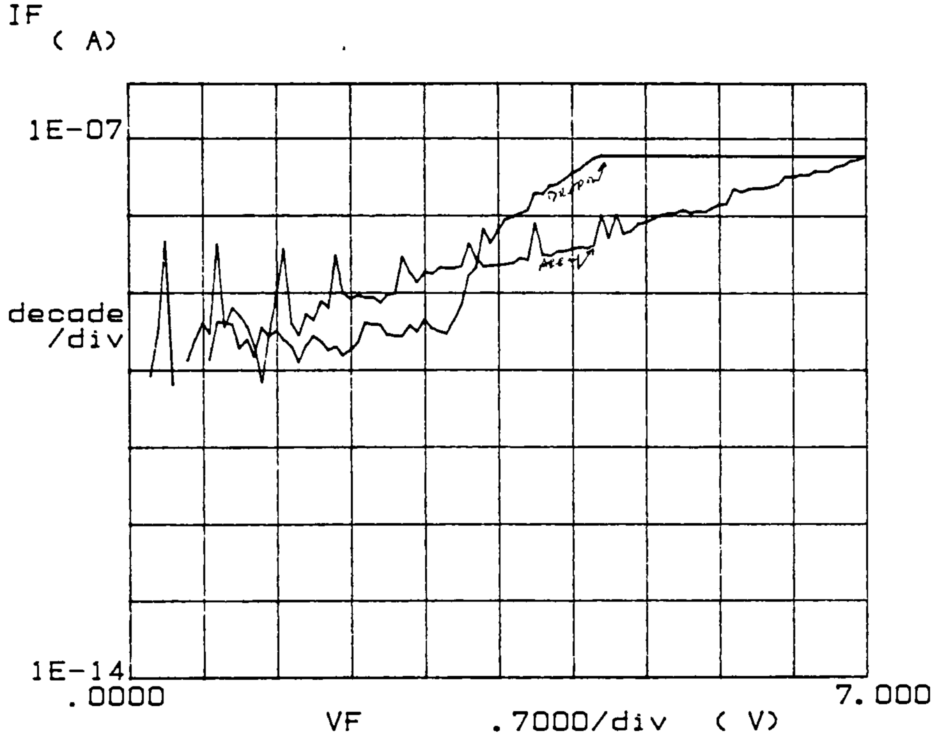


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 6.0000V
Step .0600V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B05, 400K, POLY, D/ARRY

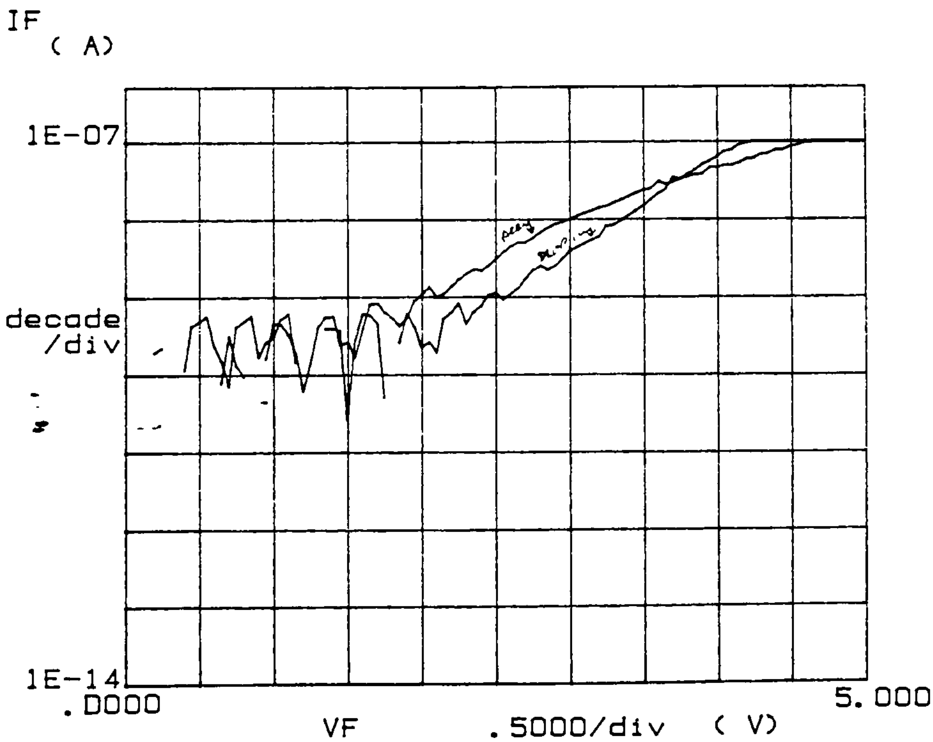


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 7.0000V
Step .0700V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B05, 1MEG, POLY, D/ARRY

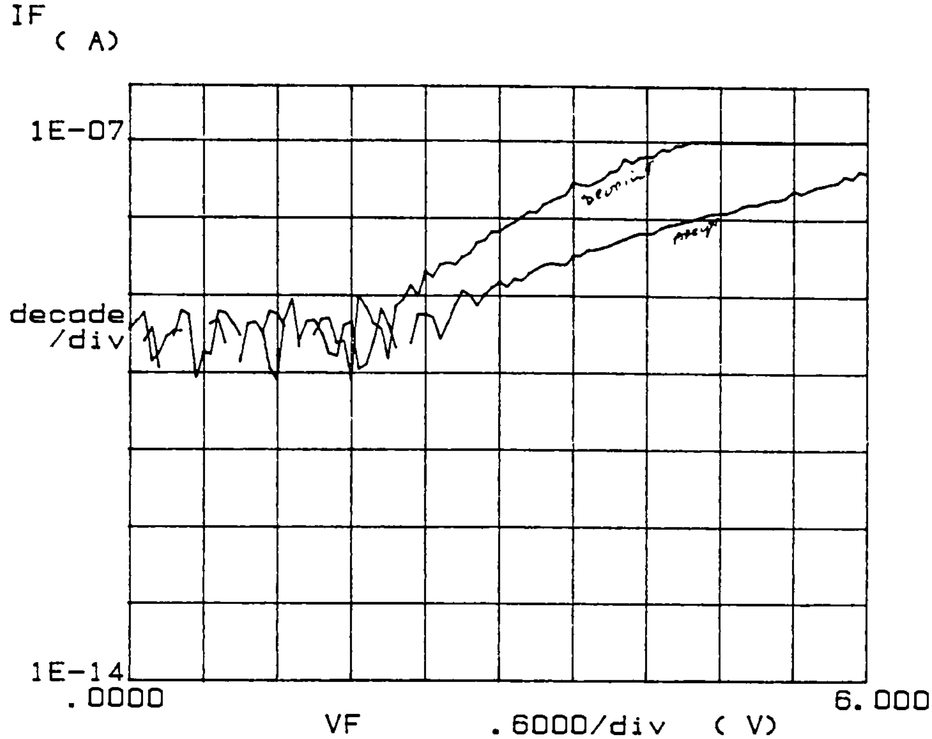


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 5.0000V
Step .0500V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B05, 1MEG, POLY, D/ARRY

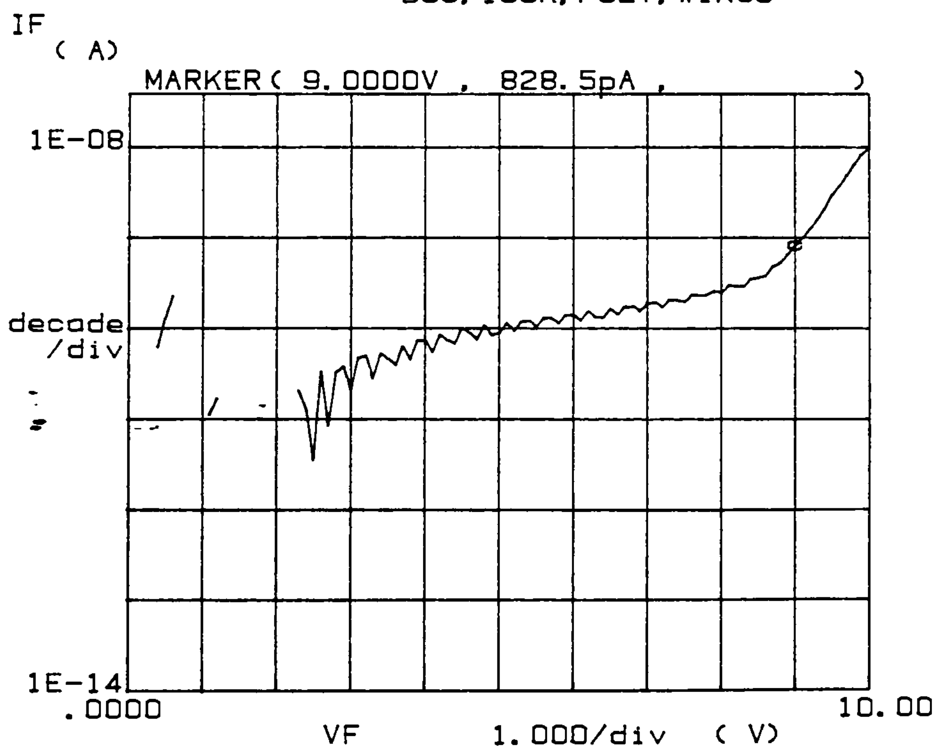


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 6.0000V
Step .0600V

Constants:
V -Ch3 .0000V

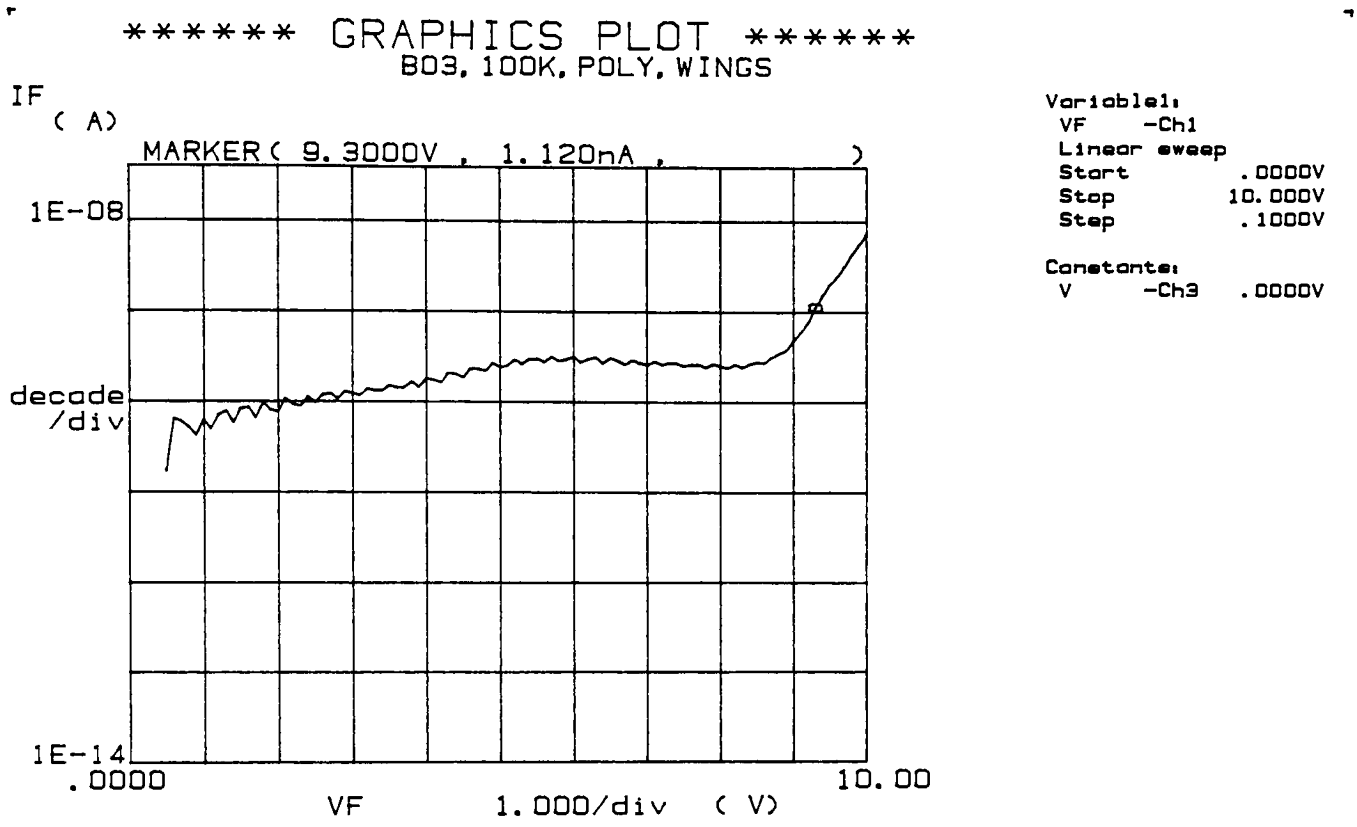
****** GRAPHICS PLOT ******

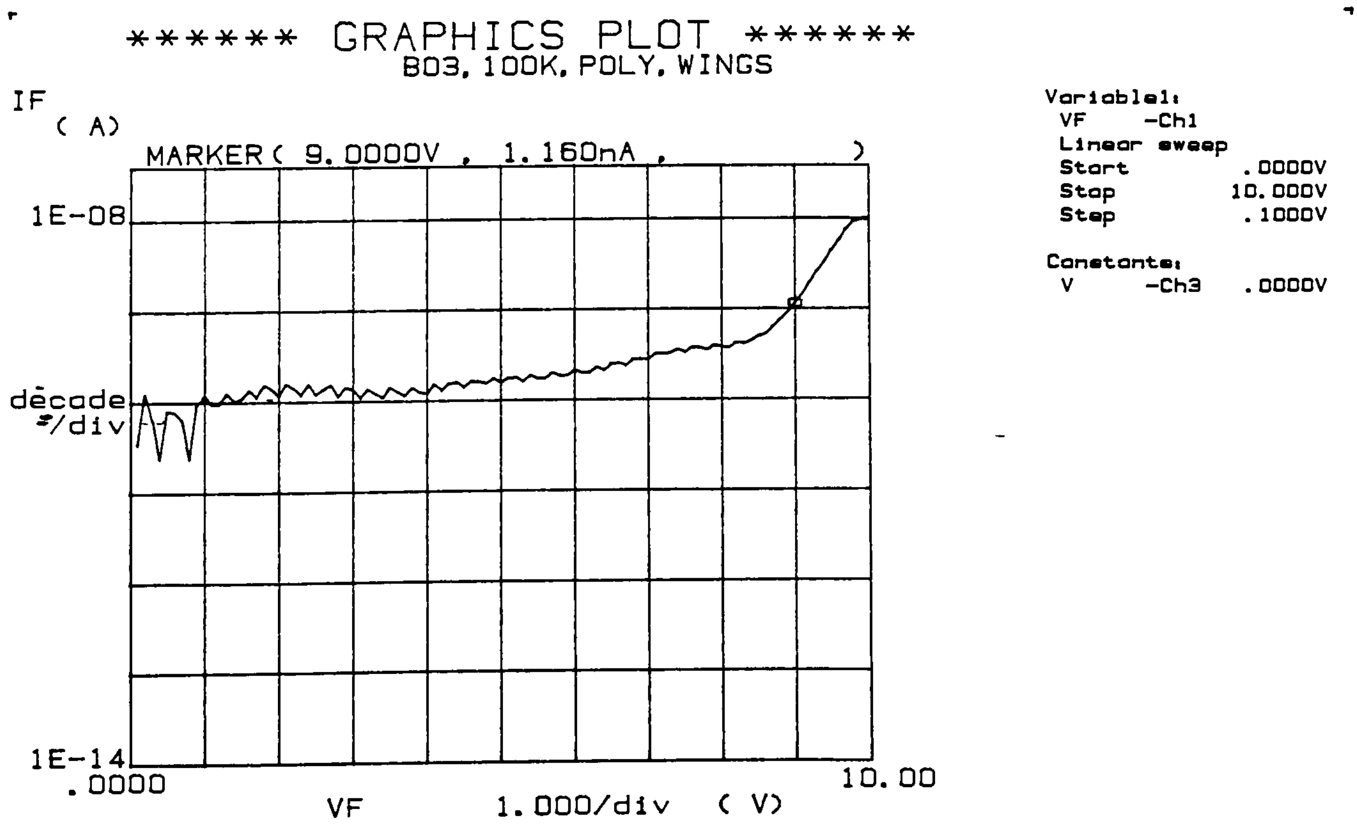
B03, 100K, POLY, WINGS



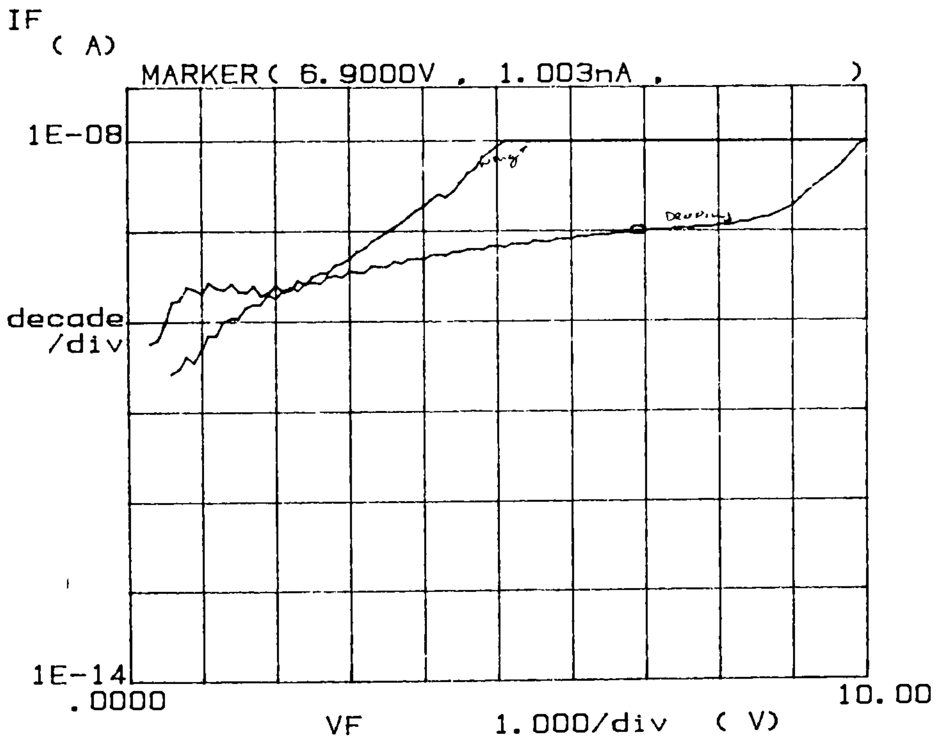
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V


****** GRAPHICS PLOT ******
B03, 100K, POLY, WINGS
IF (A)
MARKER (9.3000V , 1.120nA ,)
1E-08
decade /div
1E-14
.0000
10.00
VF 1.000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V
Constants:
V -Ch3 .0000V


****** GRAPHICS PLOT ******
B03, 100K, POLY, WINGS
IF (A)
MARKER (9.0000V , 1.160nA ,)
1E-08
decade /div
1E-14
.0000
10.00
VF 1.000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V
Constants:
V -Ch3 .0000V

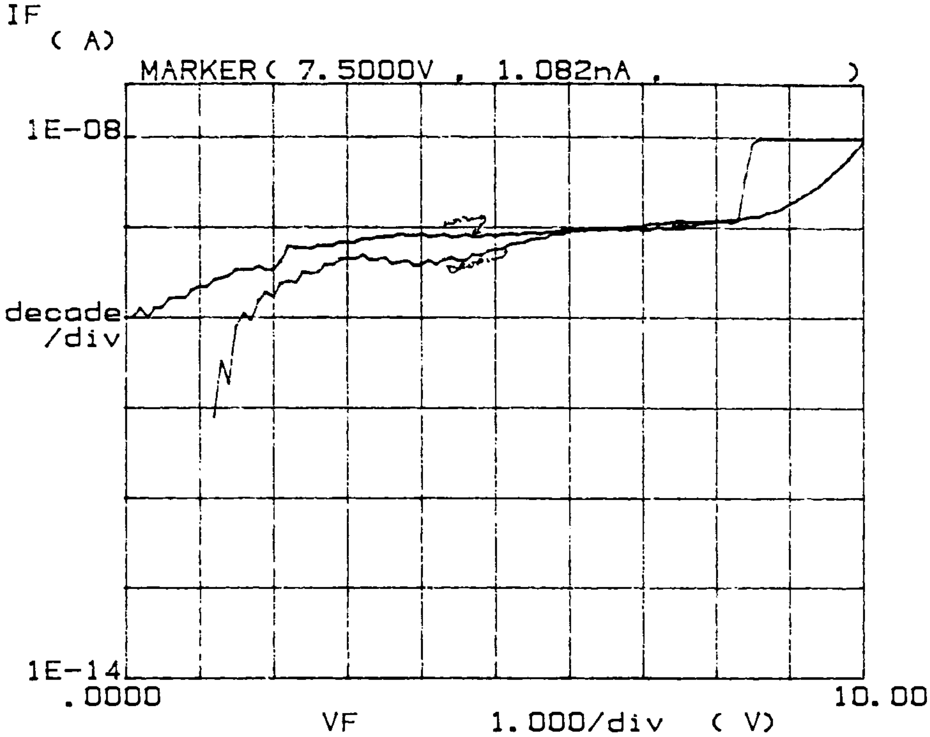
****** GRAPHICS PLOT ******
H09, 100K, POLY, D/W



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

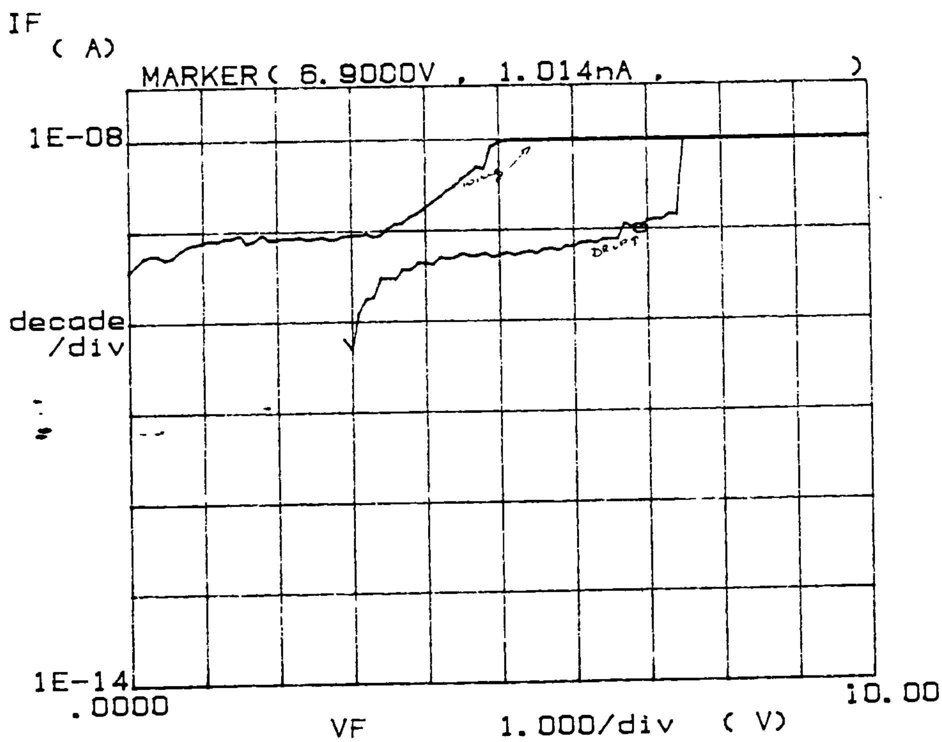
****** GRAPHICS PLOT ******
H09, 100K, POLY, D/W



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

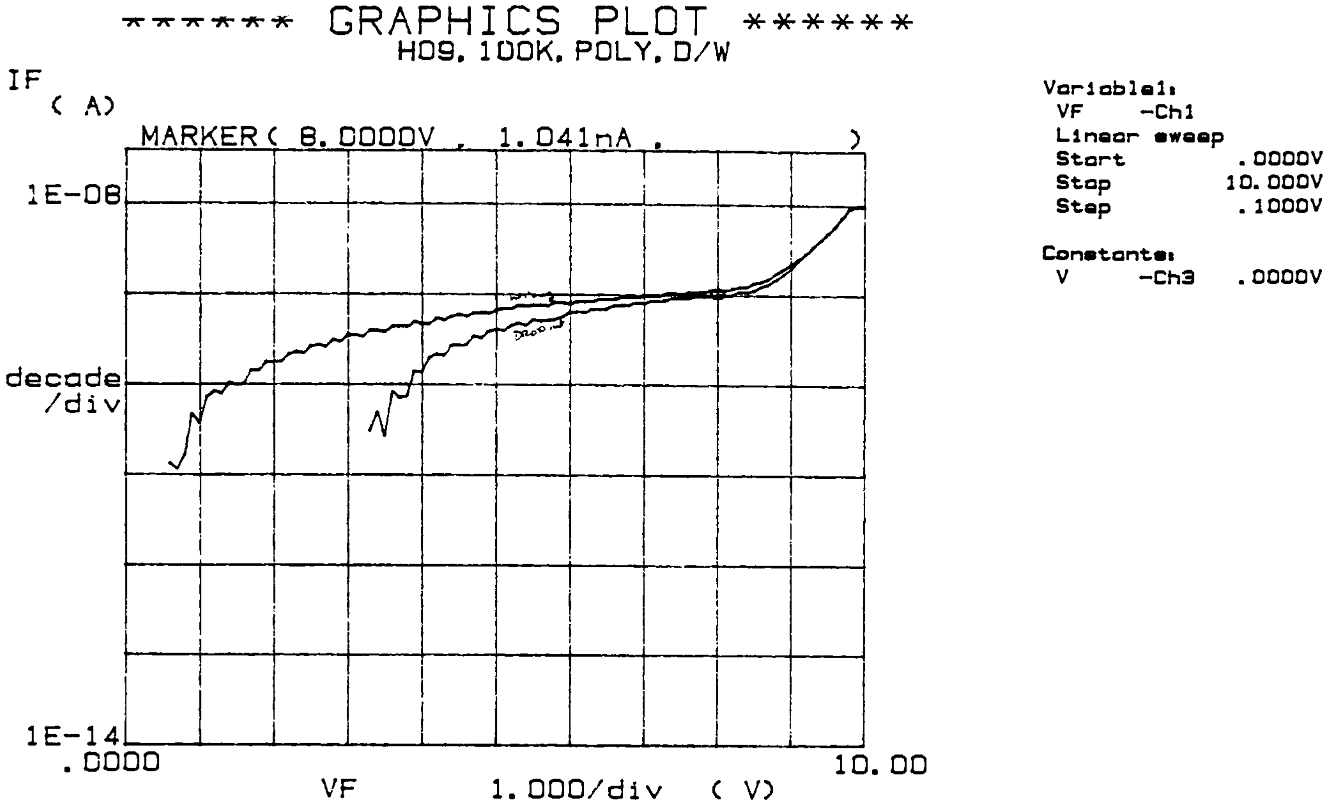
Constants:
V -Ch3 .0000V

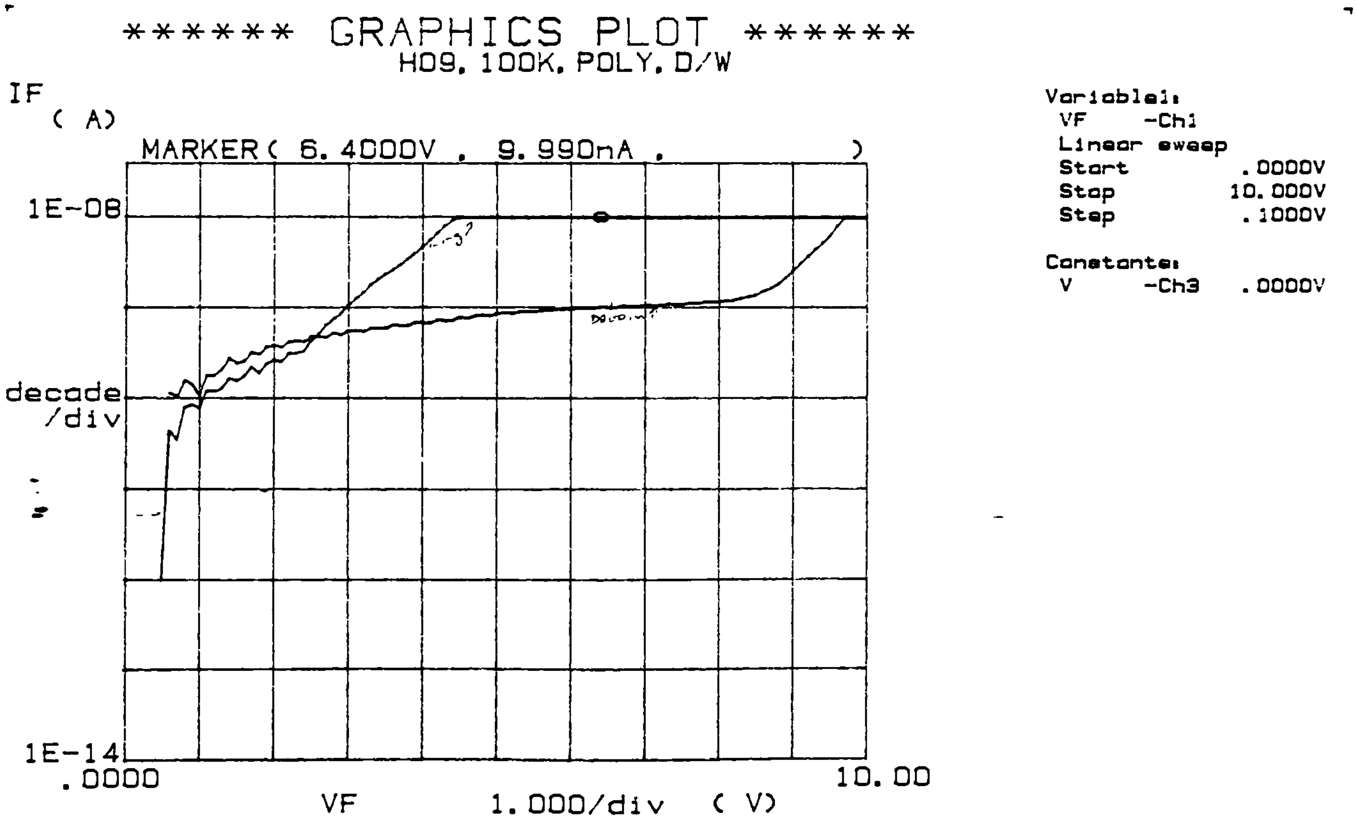
****** GRAPHICS PLOT ******
H09, 100K, POLY, D/W



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

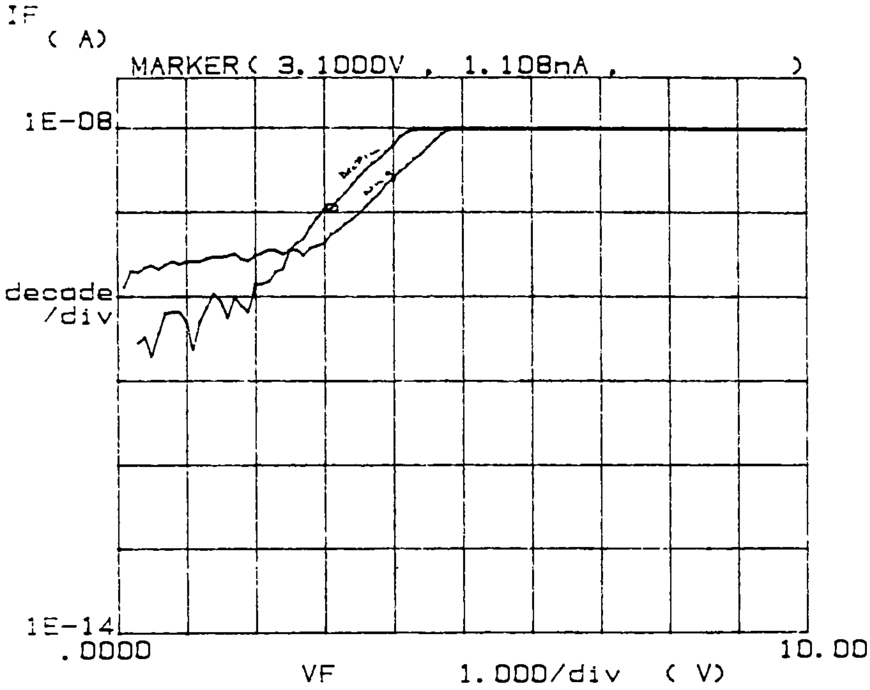

****** GRAPHICS PLOT ******
H09, 100K, POLY, D/W
IF (A)
MARKER (8.0000V , 1.041nA ,)
1E-08
decade /div
1E-14
.0000
10.00
VF 1.000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V
Constants:
V -Ch3 .0000V


****** GRAPHICS PLOT ******
H09, 100K, POLY, D/W
IF (A)
MARKER (6.4000V , 9.990nA ,)
1E-08
decade /div
1E-14
.0000
10.00
VF 1.000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V
Constants:
V -Ch3 .0000V

2500 Å Etch Back Results

****** GRAPHICS PLOT ******

HD5, 100K, POLY, D/W

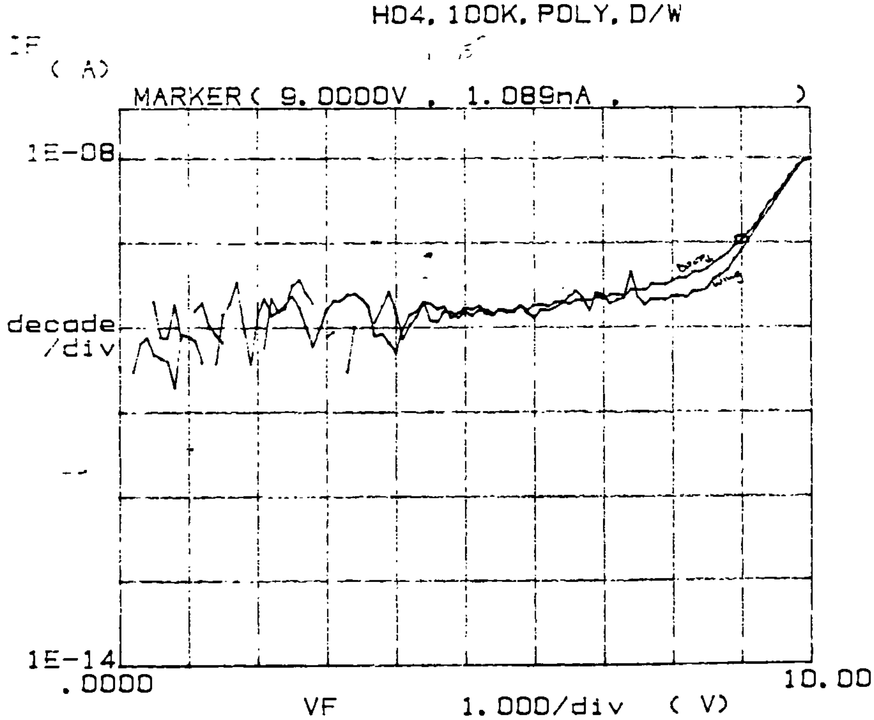


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

HD4, 100K, POLY, D/W

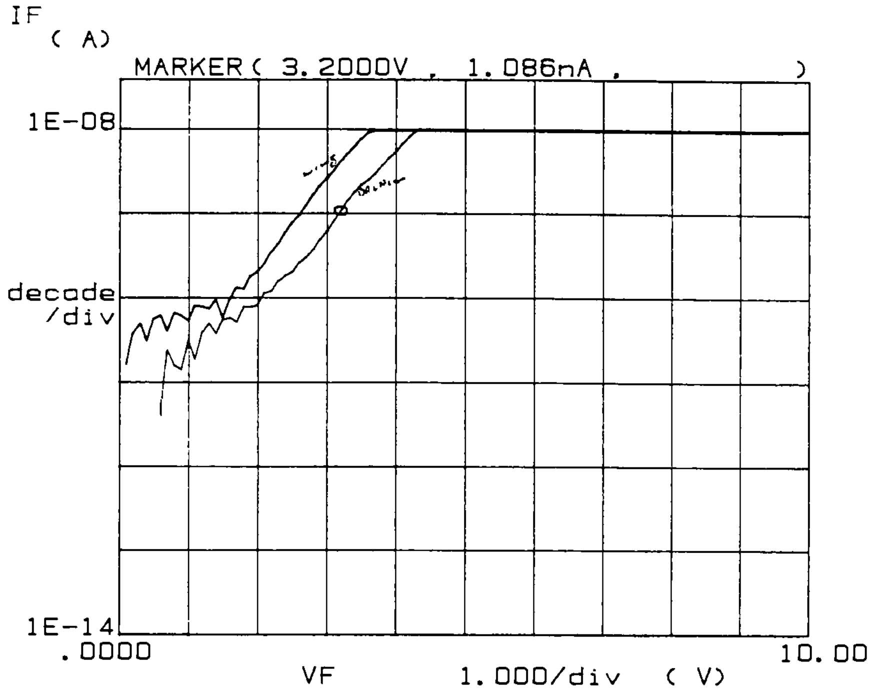


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

HD5, 100K, POLY, D/W

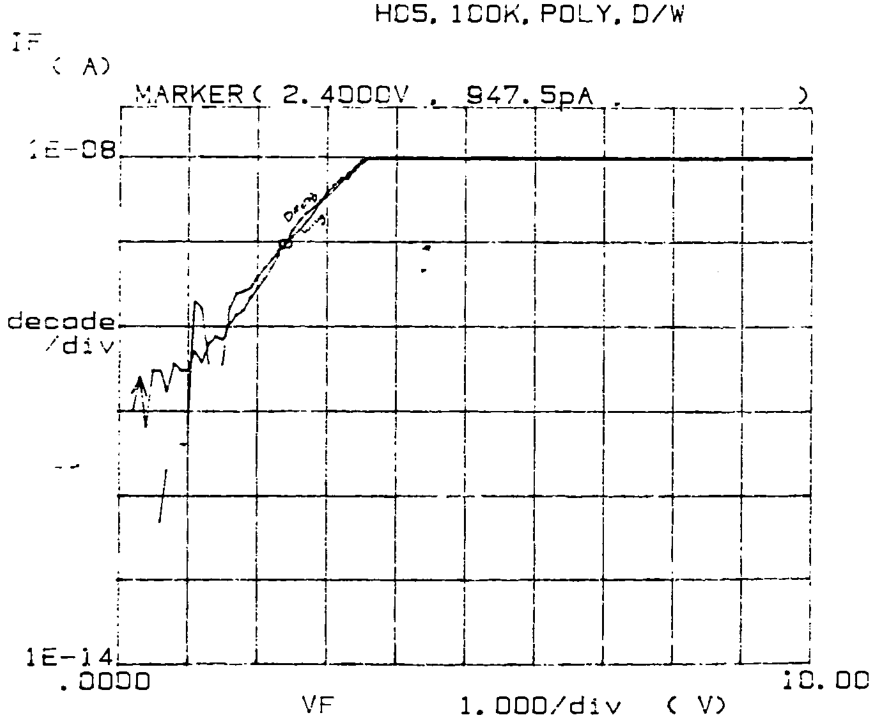


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

HD5, 100K, POLY, D/W

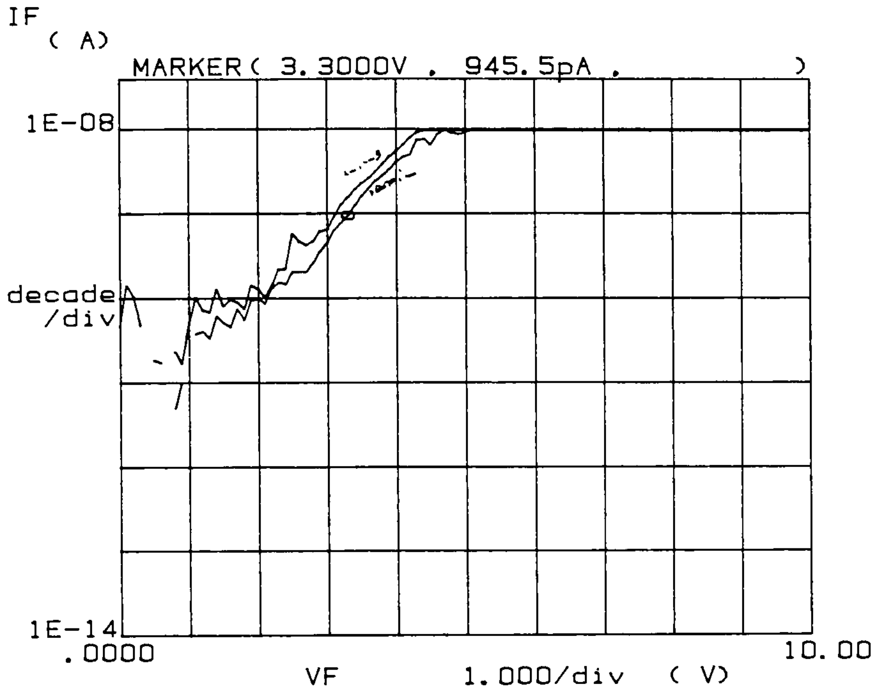


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

HO5. 100K. POLY. D/W

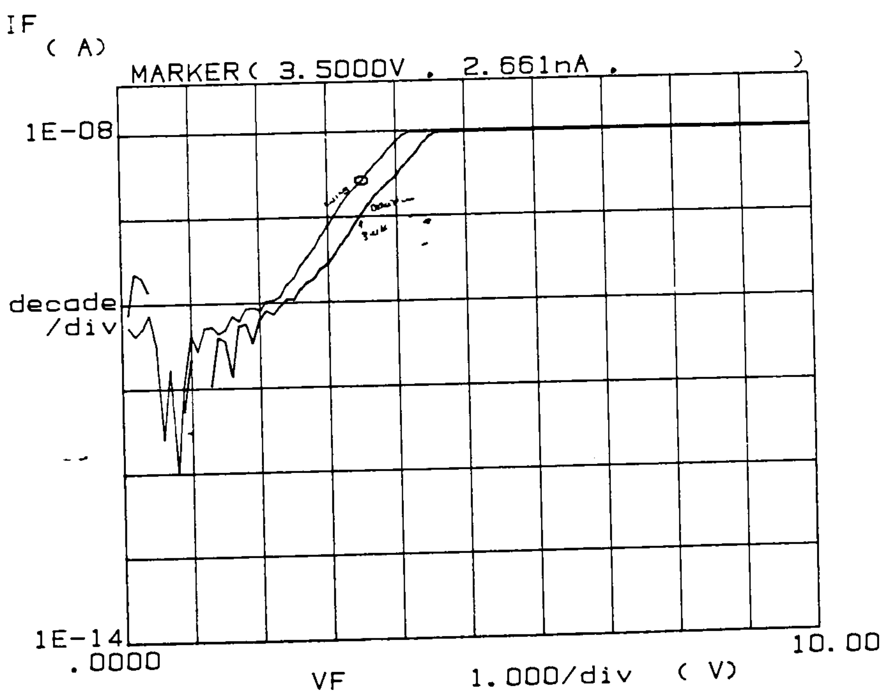


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

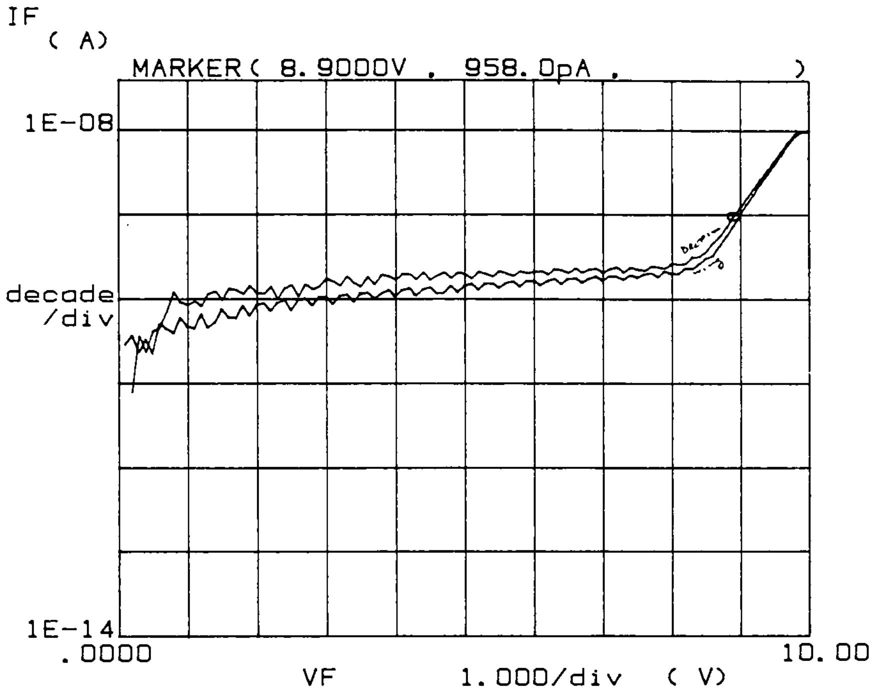
HO5. 100K. POLY. D/W



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

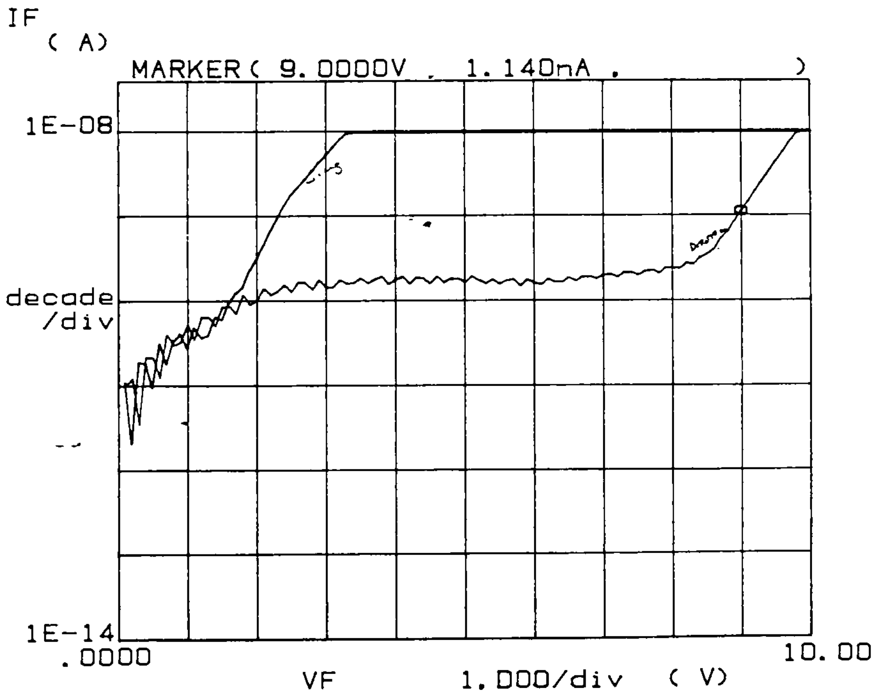
****** GRAPHICS PLOT ******
HO5. 100K. POLY. D/W



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******
HO5. 100K. POLY. D/W

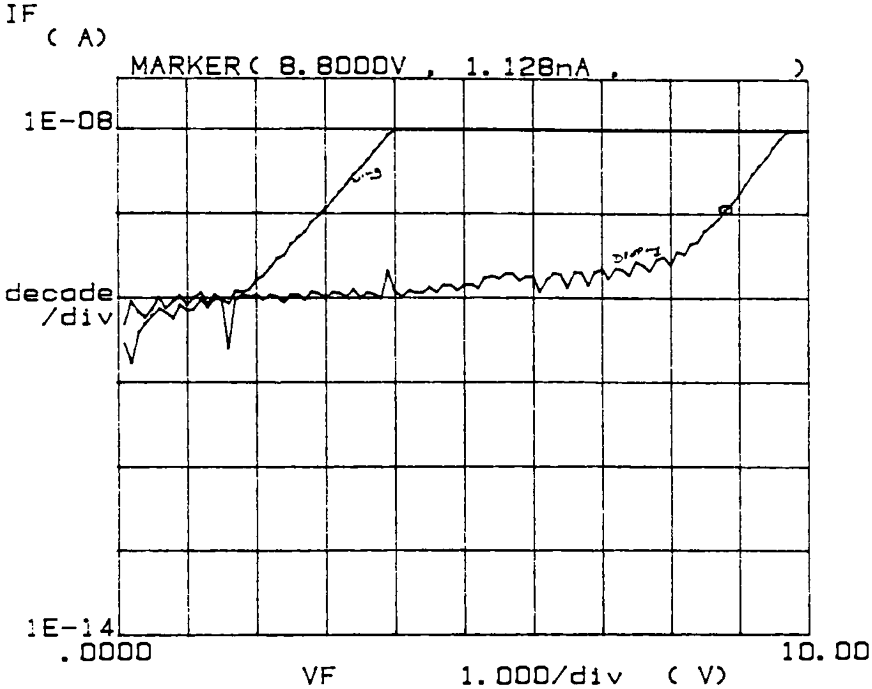


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

HD4, 100K, POLY, D/W

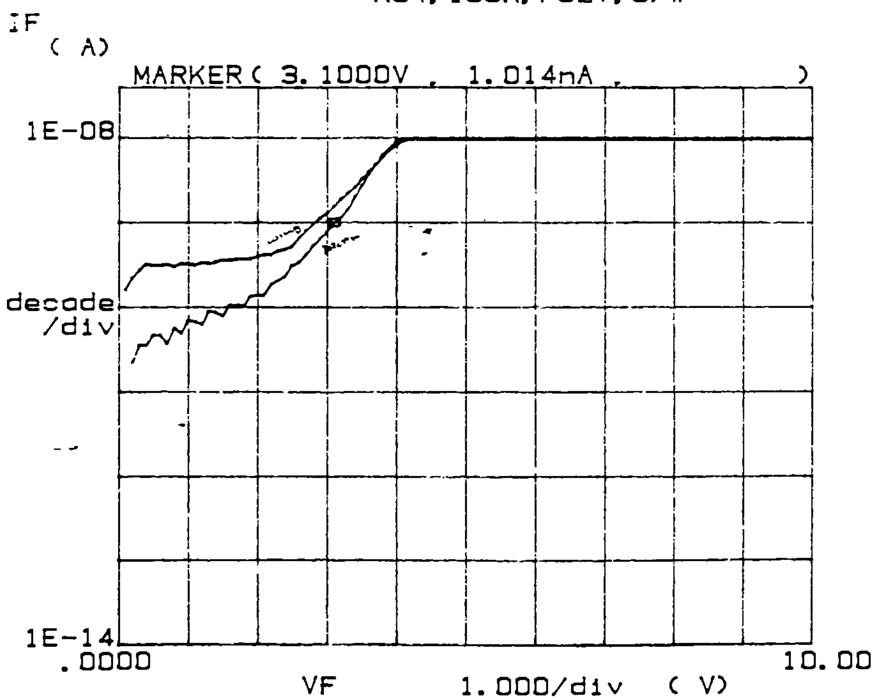


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

HD4, 100K, POLY, D/W

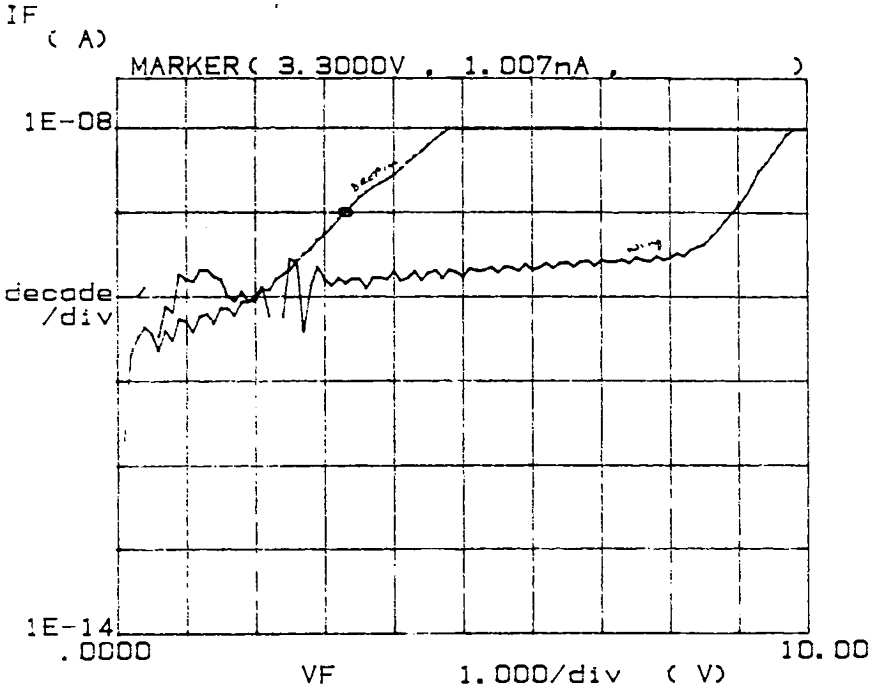


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

H04, 100K, POLY, D/W

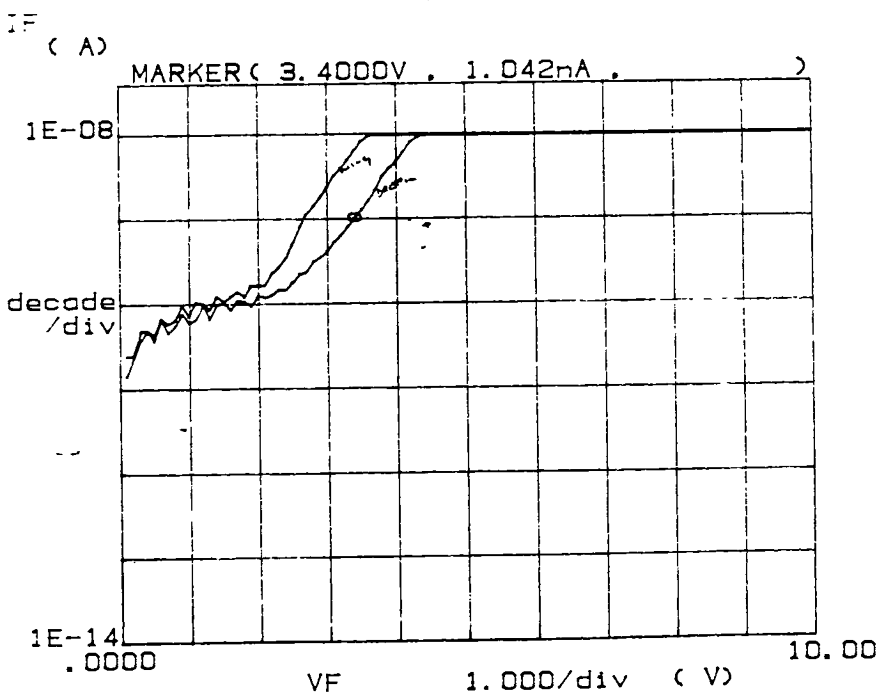


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

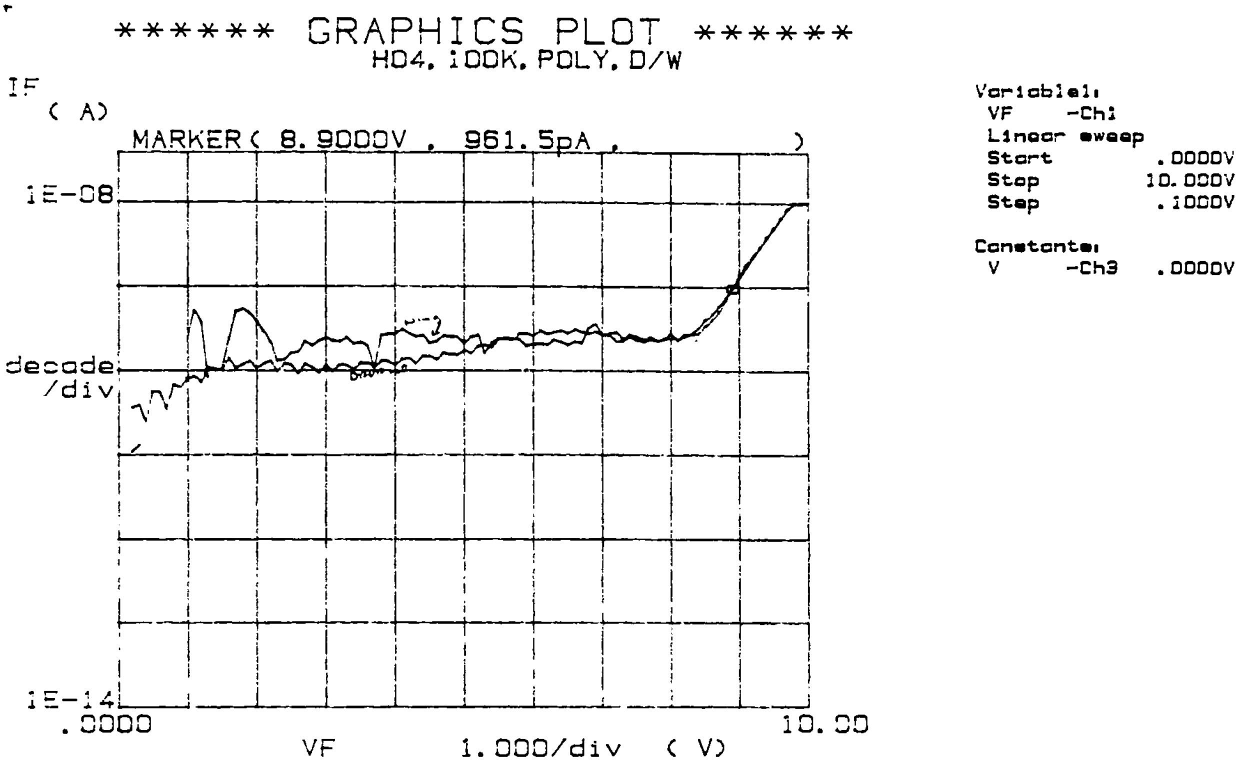
****** GRAPHICS PLOT ******

H04, 100K, POLY, D/W

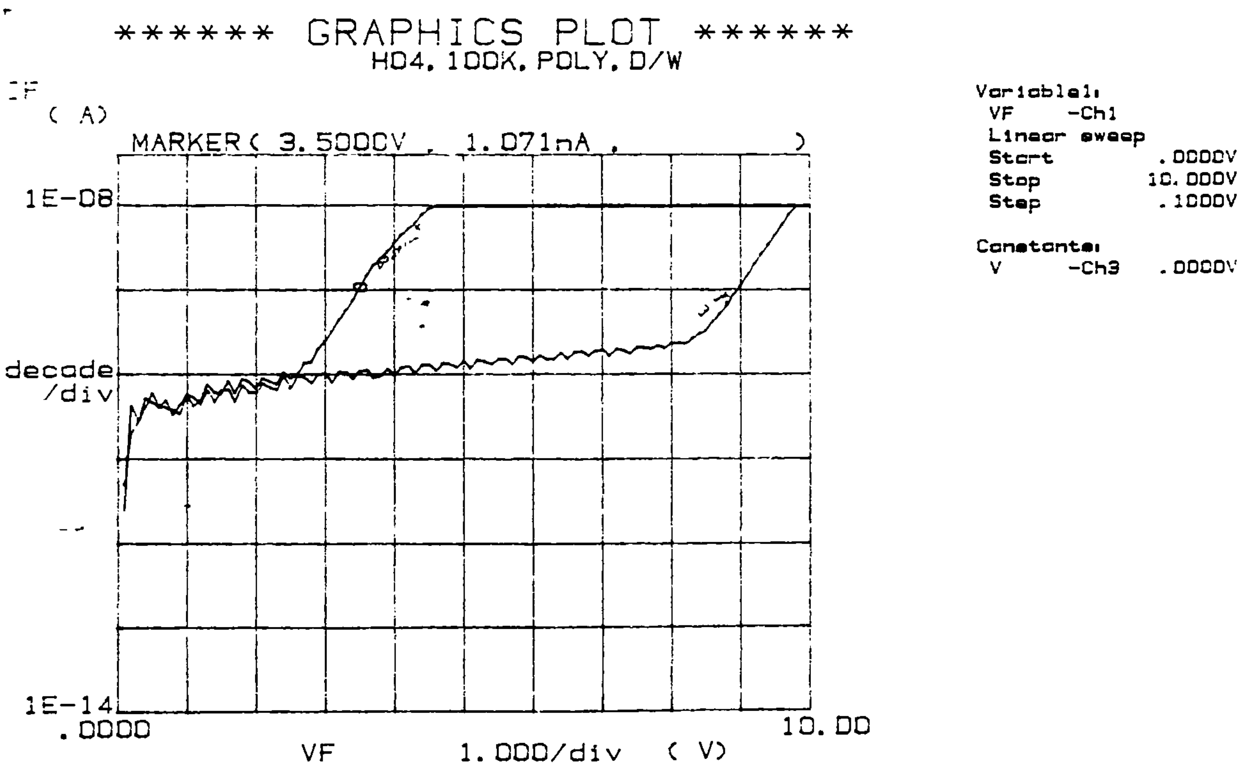


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

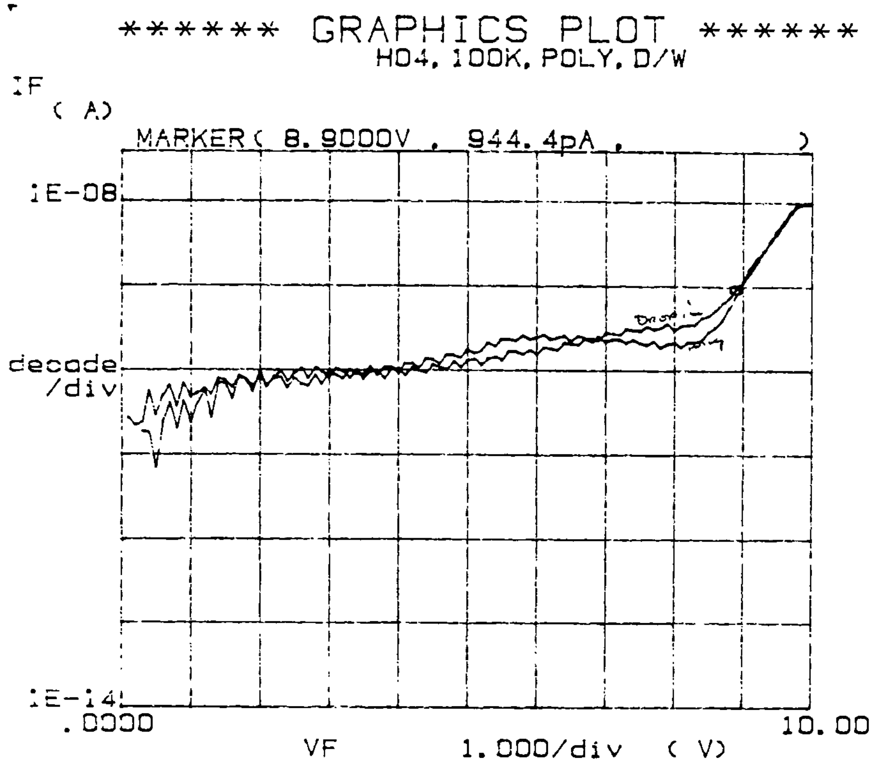
Constants:
V -Ch3 .0000V



****** GRAPHICS PLOT ******
HD4. 100K. POLY. D/W
IF
(A)
MARKER (8.9000V , 961.5pA ,)
1E-08
decade
/div
1E-14
.0000
10.00
VF 1.000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V
Constants:
V -Ch3 .0000V

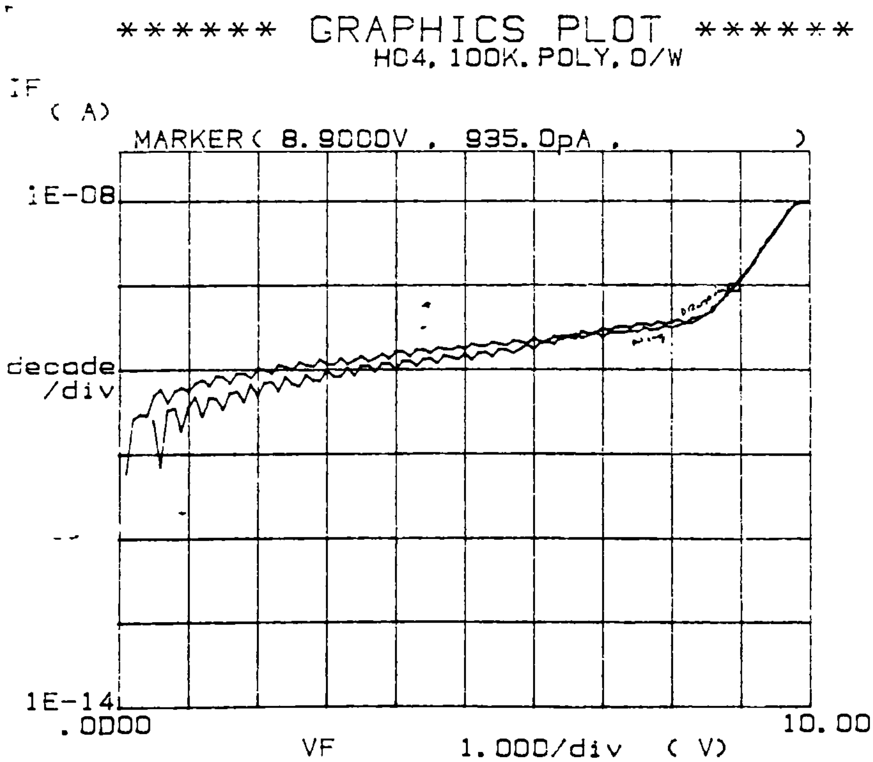


****** GRAPHICS PLOT ******
HD4. 100K. POLY. D/W
IF
(A)
MARKER (3.5000V , 1.071nA ,)
1E-08
decade
/div
1E-14
.0000
10.00
VF 1.000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V
Constants:
V -Ch3 .0000V



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

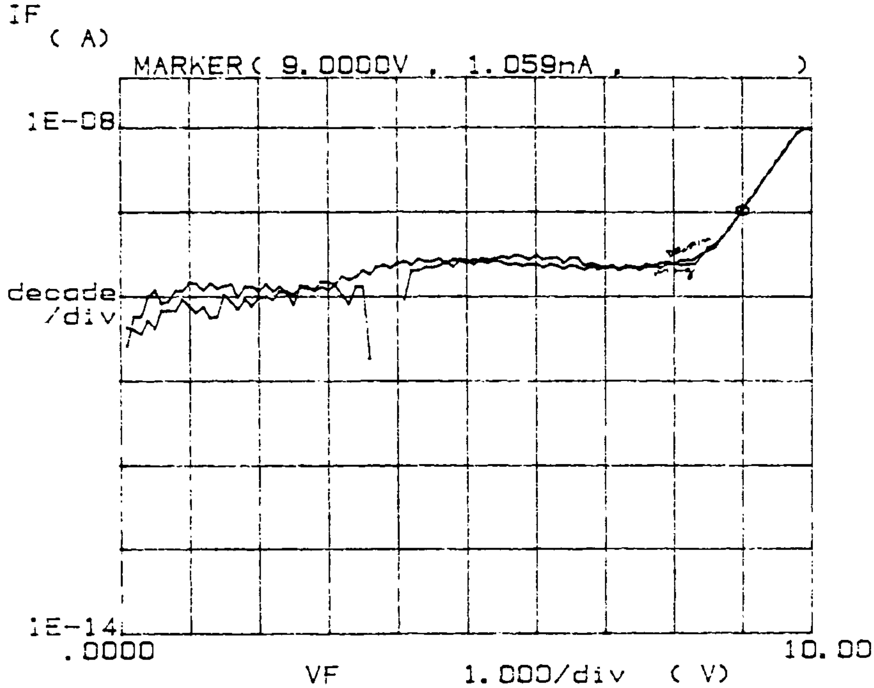


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

HD4, 100K, POLY, D/W

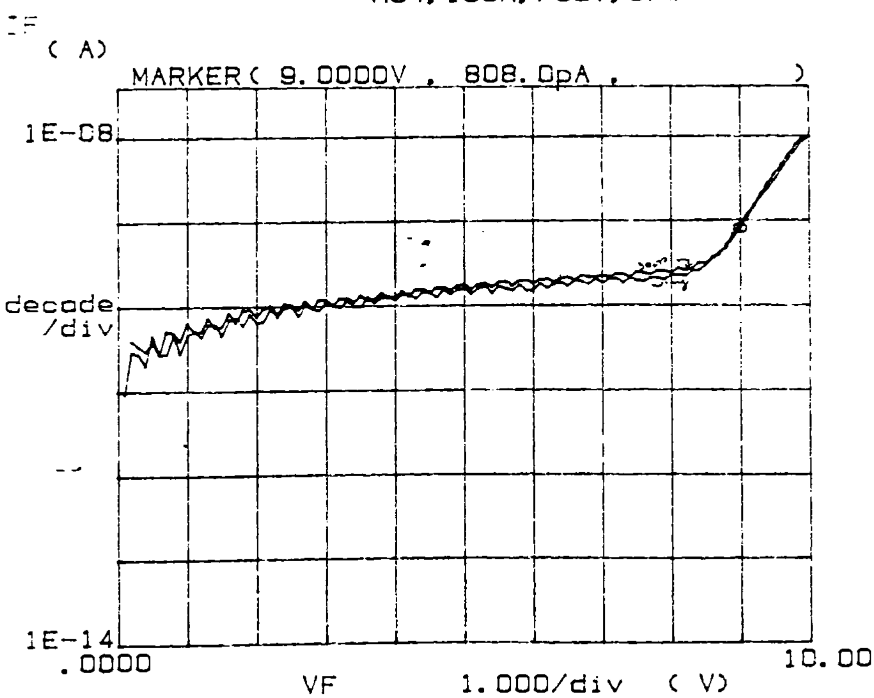


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

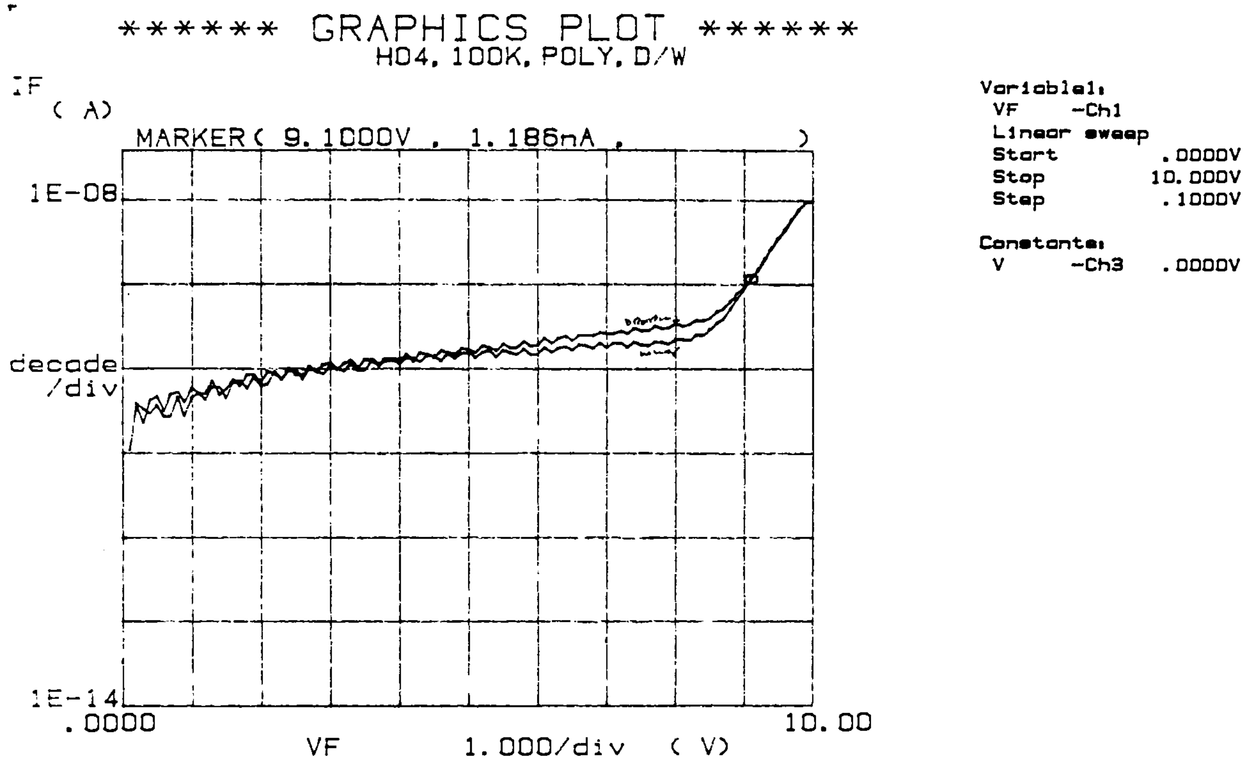
****** GRAPHICS PLOT ******

HD4, 100K, POLY, D/W

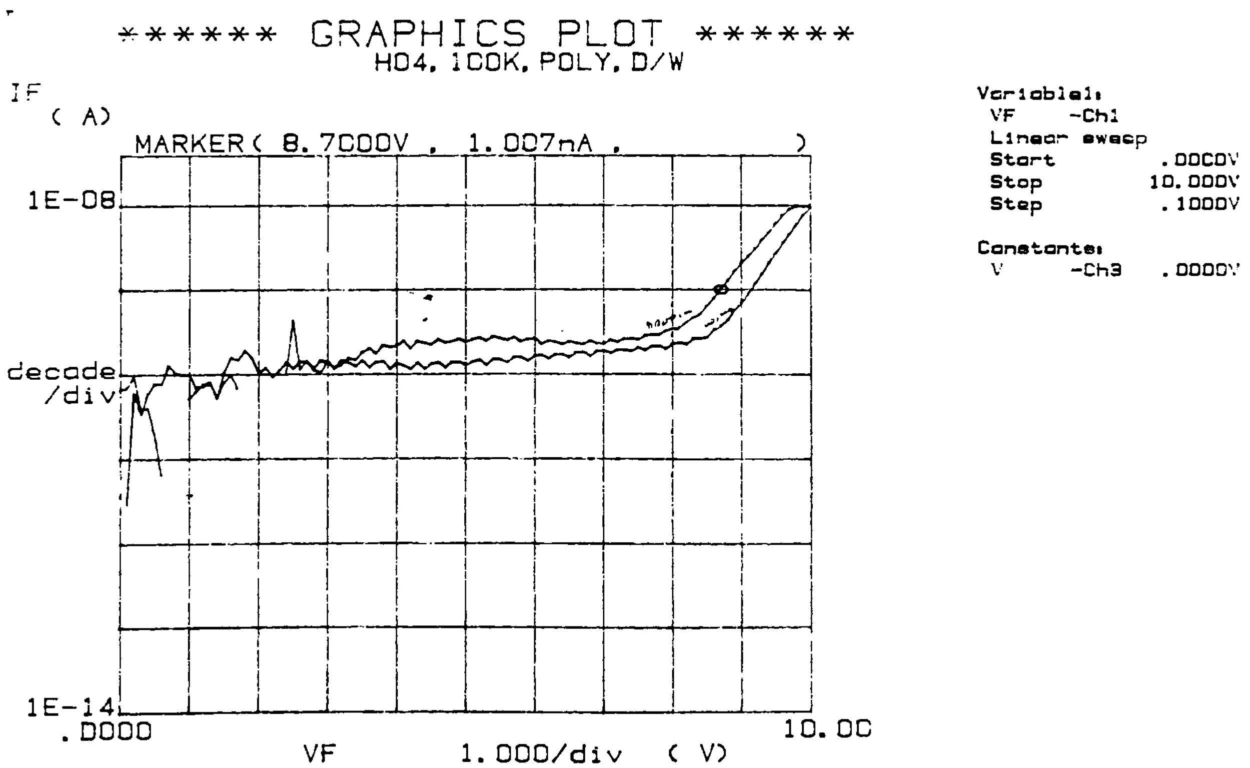


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V



****** GRAPHICS PLOT ******
H04, 100K, POLY, D/W
IF
(A)
MARKER (9.1000V , 1.186nA ,)
1E-08
decade
/div
1E-14
.0000
10.00
VF 1.000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V
Constants:
V -Ch3 .0000V

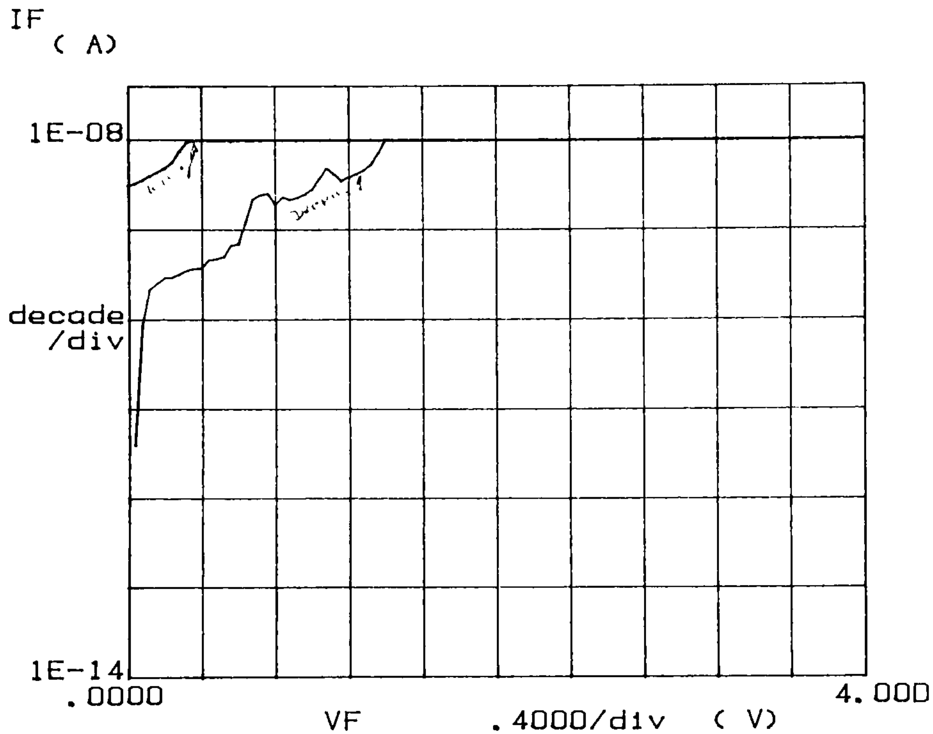


****** GRAPHICS PLOT ******
H04, 100K, POLY, D/W
IF
(A)
MARKER (8.7000V , 1.007nA ,)
1E-08
decade
/div
1E-14
.0000
10.00
VF 1.000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V
Constants:
V -Ch3 .0000V

3500 Å Etch Back Results

****** GRAPHICS PLOT ******

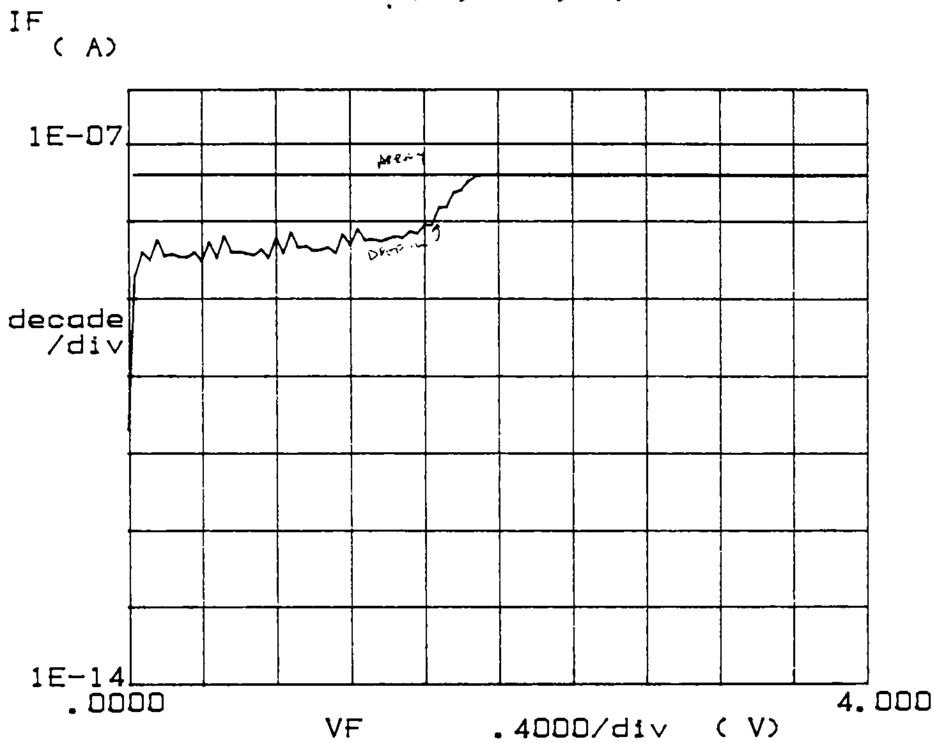
H02, 100K, AL, D/W



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

Constants:
V -Ch3 .0000V

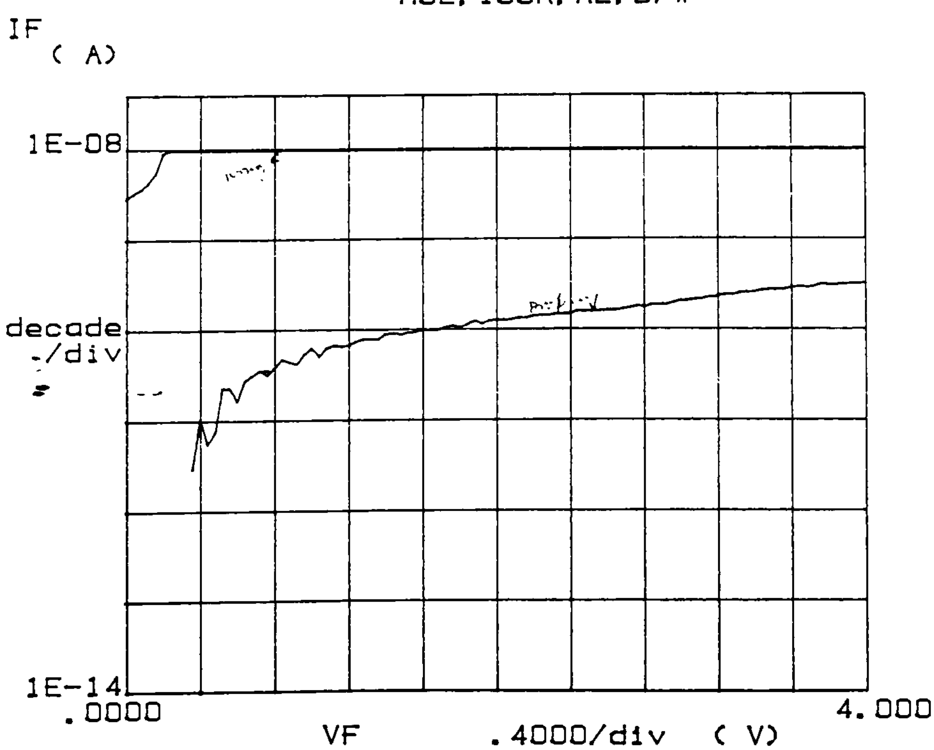
****** GRAPHICS PLOT ******
HO2, 400K, AL, D/ARRY



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

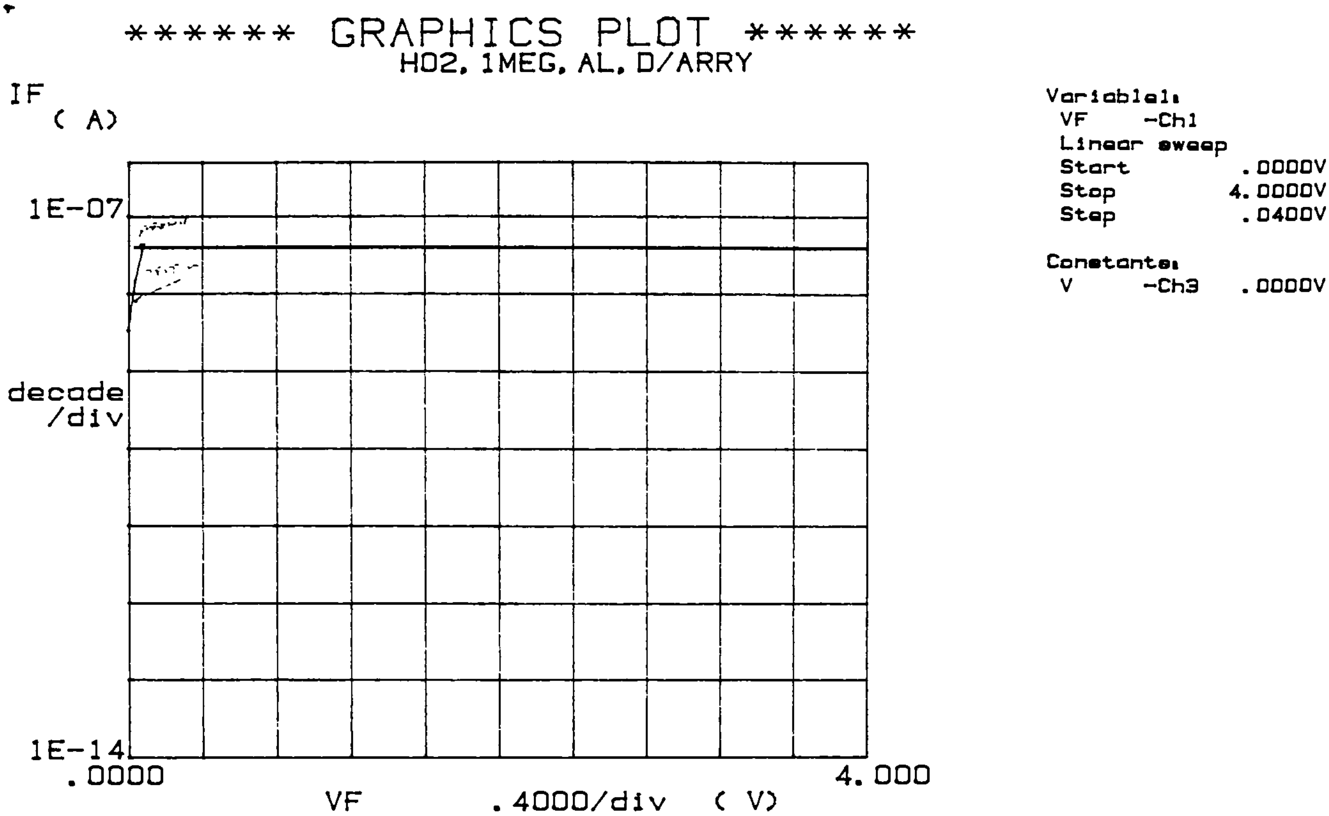
Constants:
V -Ch3 .0000V

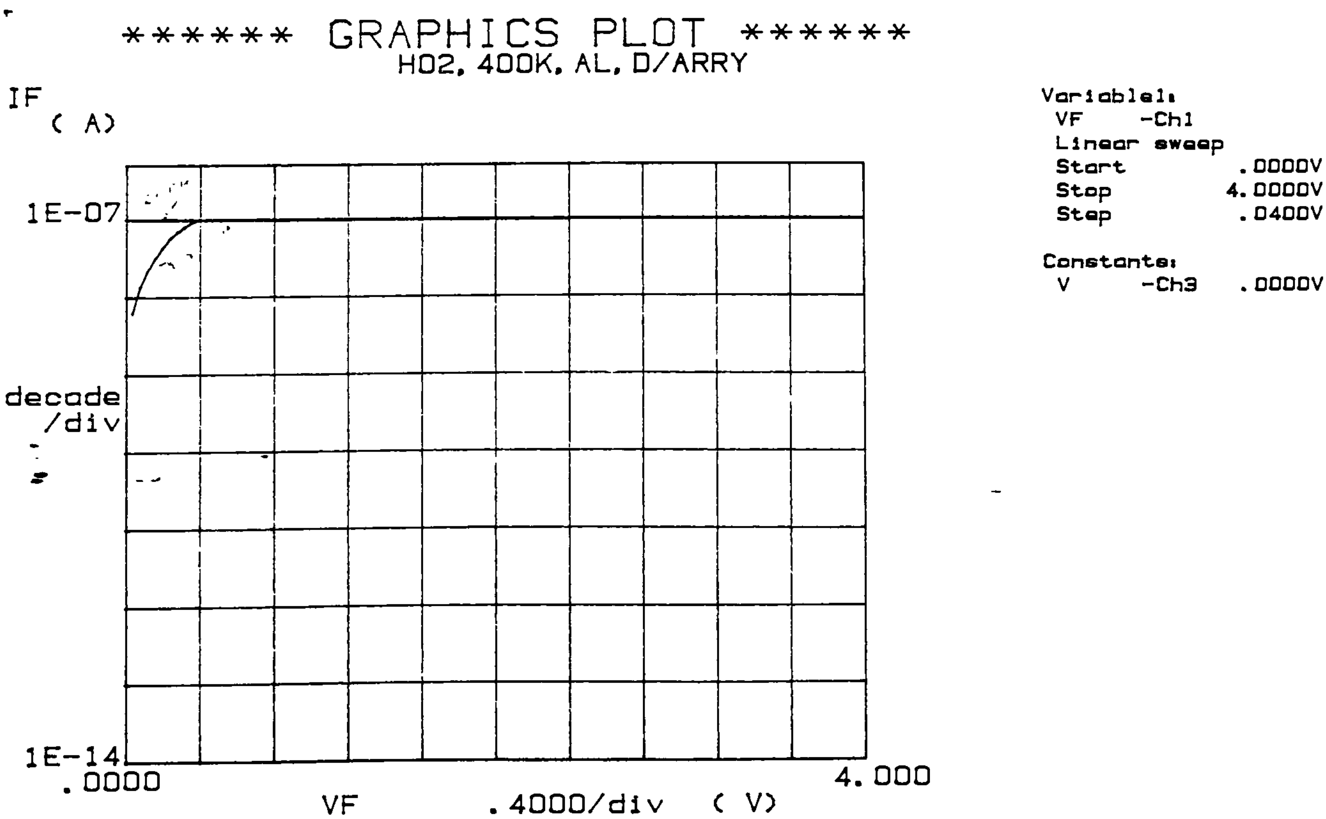
****** GRAPHICS PLOT ******
HO2, 100K, AL, D/W

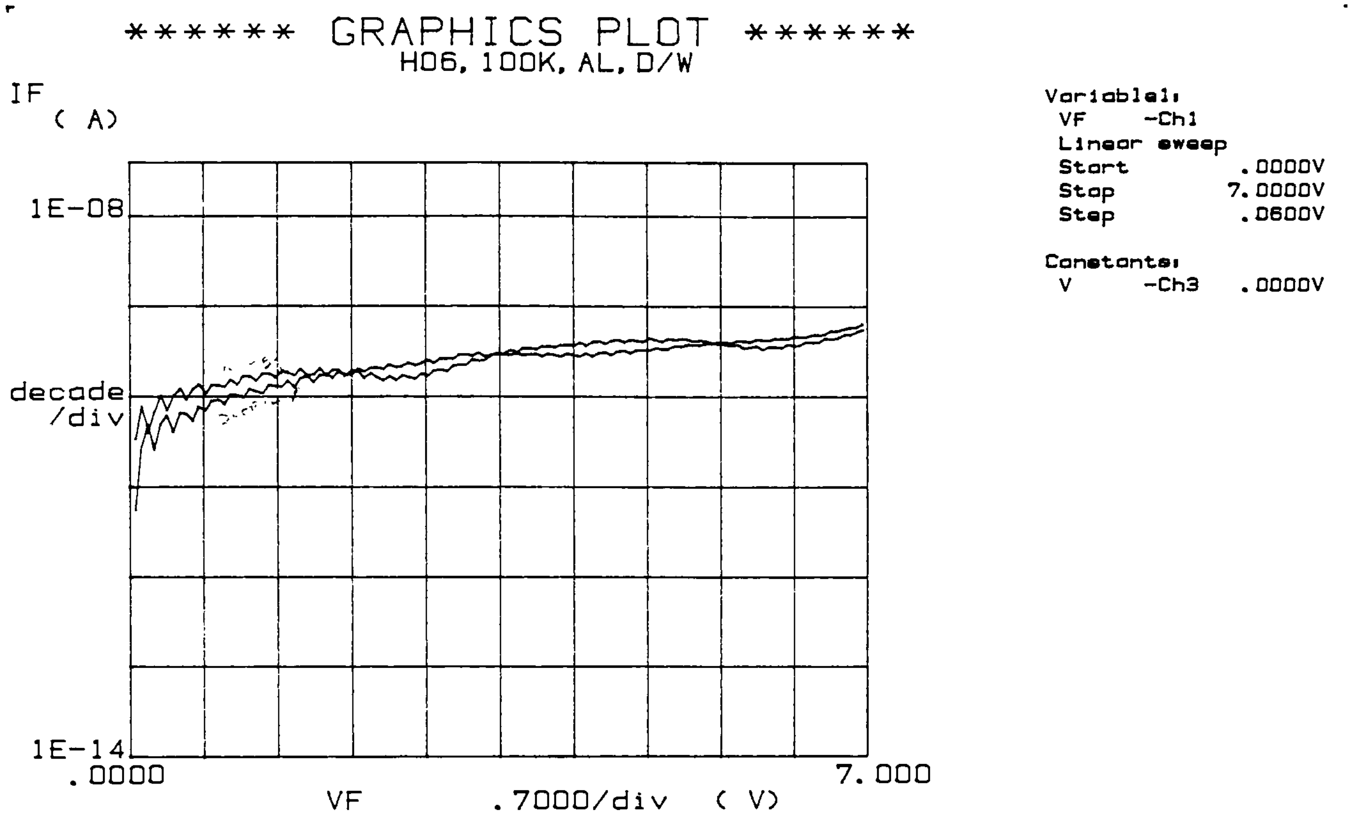


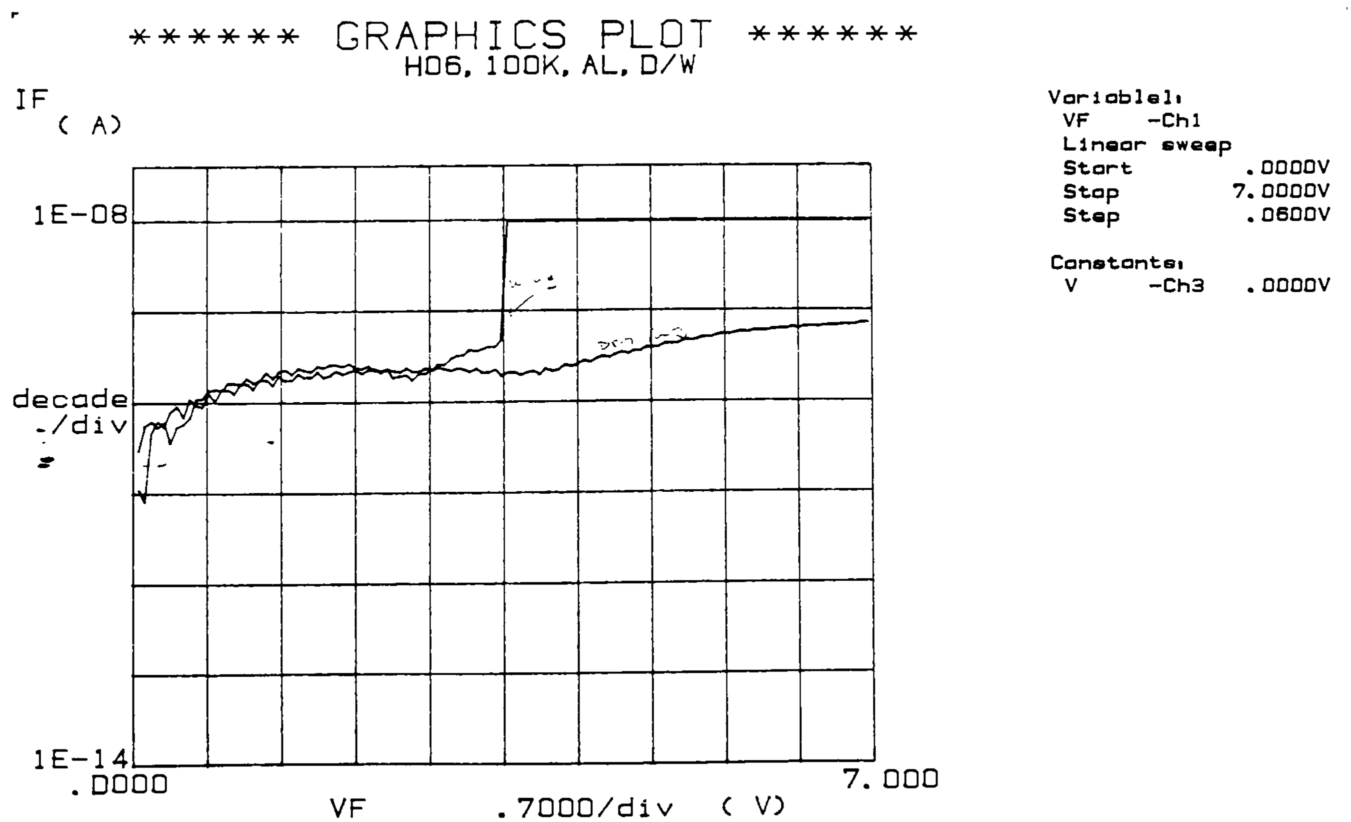
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

Constants:
V -Ch3 .0000V


****** GRAPHICS PLOT ******
H02, 1MEG, AL, D/ARRY
IF (A)
1E-07
decade /div
1E-14
.0000
4.000
VF .4000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V
Constants:
V -Ch3 .0000V

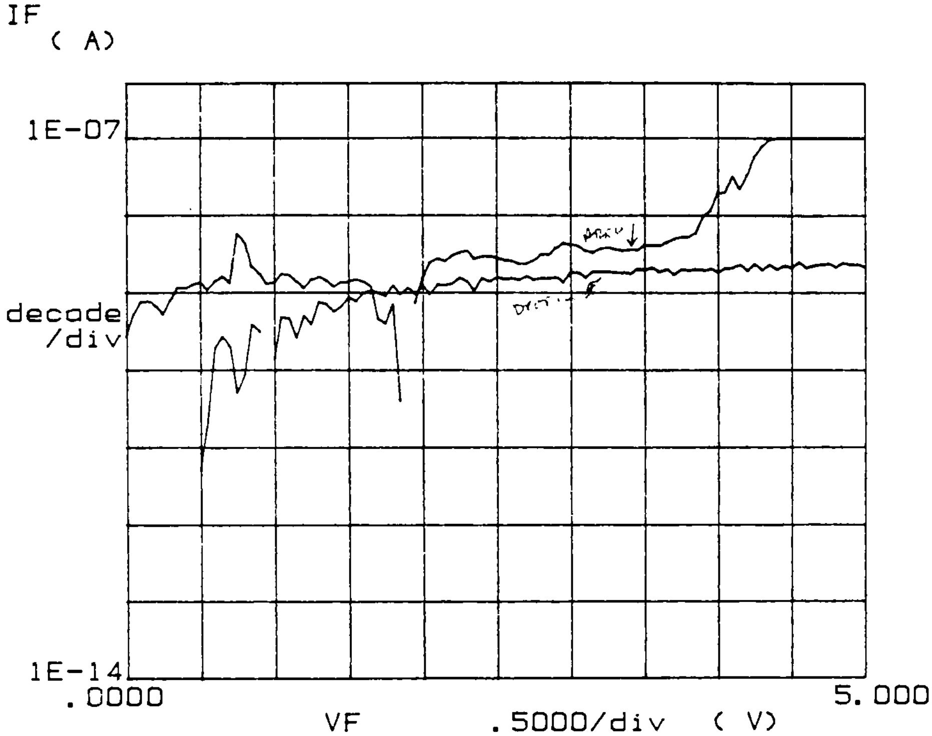

****** GRAPHICS PLOT ******
H02, 400K, AL, D/ARRY
IF (A)
1E-07
decade /div
1E-14
.0000
4.000
VF .4000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V
Constants:
V -Ch3 .0000V


****** GRAPHICS PLOT ******
H06, 100K, AL, D/W
IF (A)
1E-08
decade /div
1E-14
.0000
7.000
VF .7000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 7.0000V
Step .0600V
Constants:
V -Ch3 .0000V


****** GRAPHICS PLOT ******
H06, 100K, AL, D/W
IF (A)
1E-08
decade /div
1E-14
.0000
7.000
VF .7000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 7.0000V
Step .0600V
Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

HO6, 1MEG, AL, D/ARRY

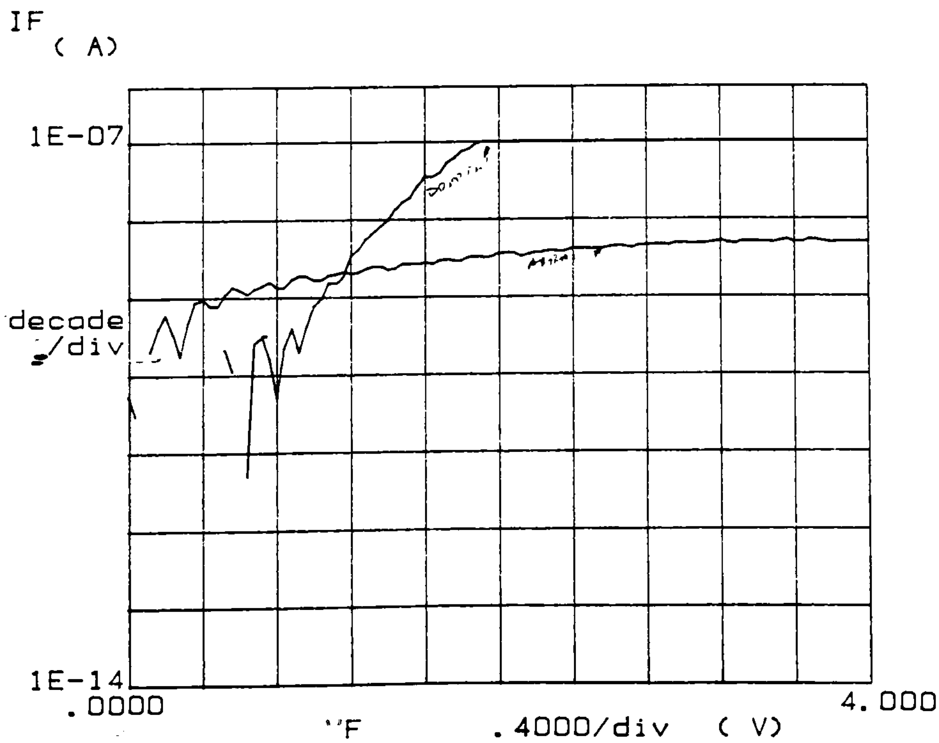


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 5.0000V
Step .0500V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

HO6, 1MEG, AL, D/ARRY

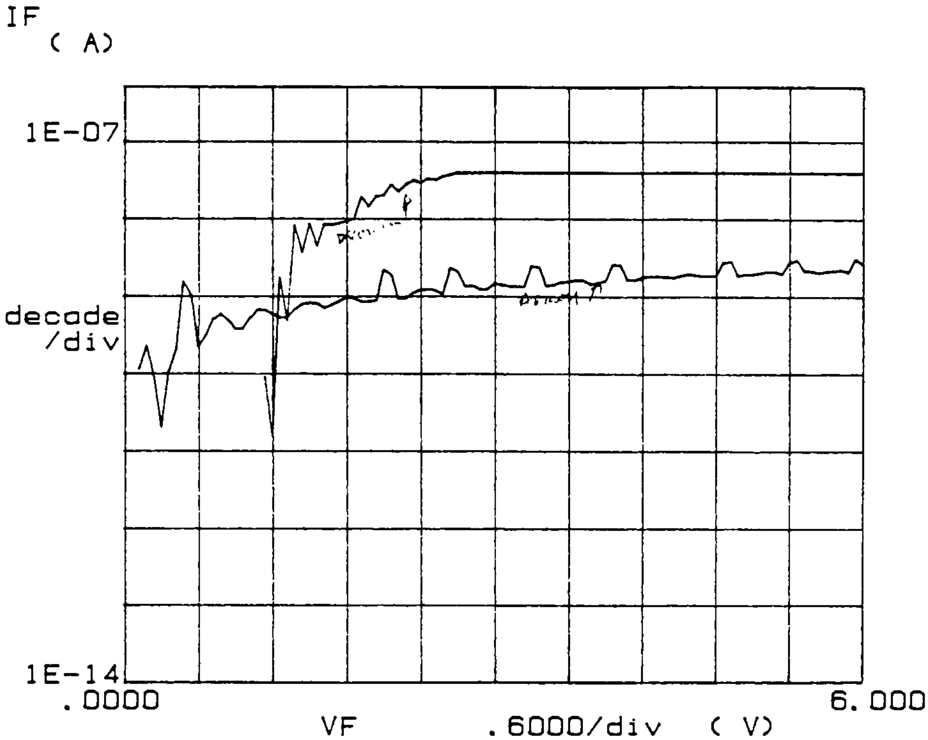


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

.H06, 400K, AL, D/ARRY

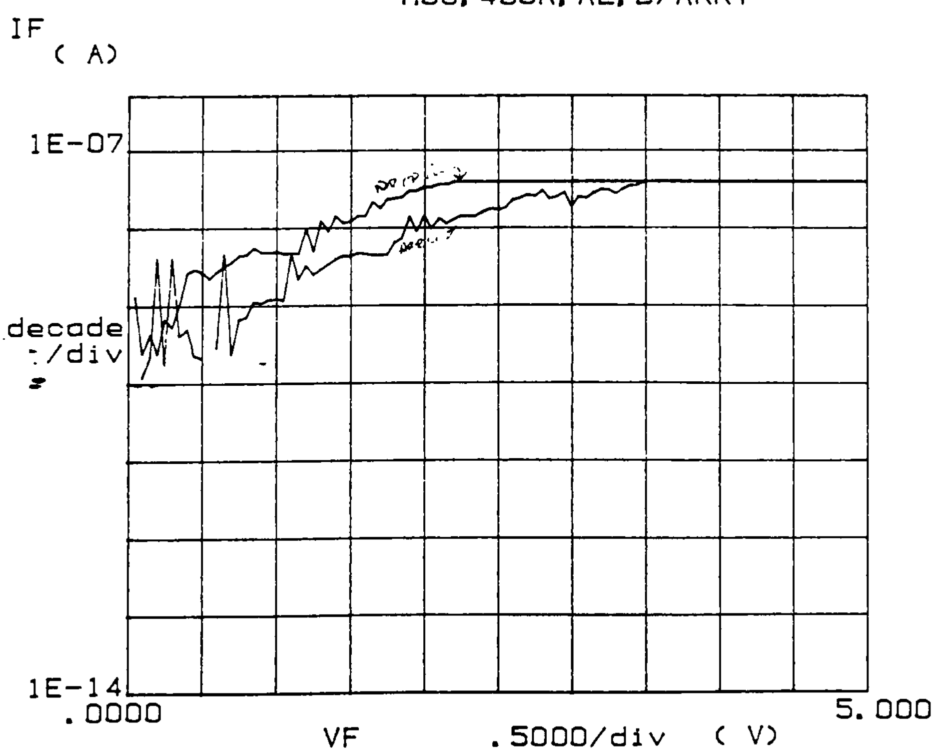


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 6.0000V
Step .0600V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

H06, 400K, AL, D/ARRY

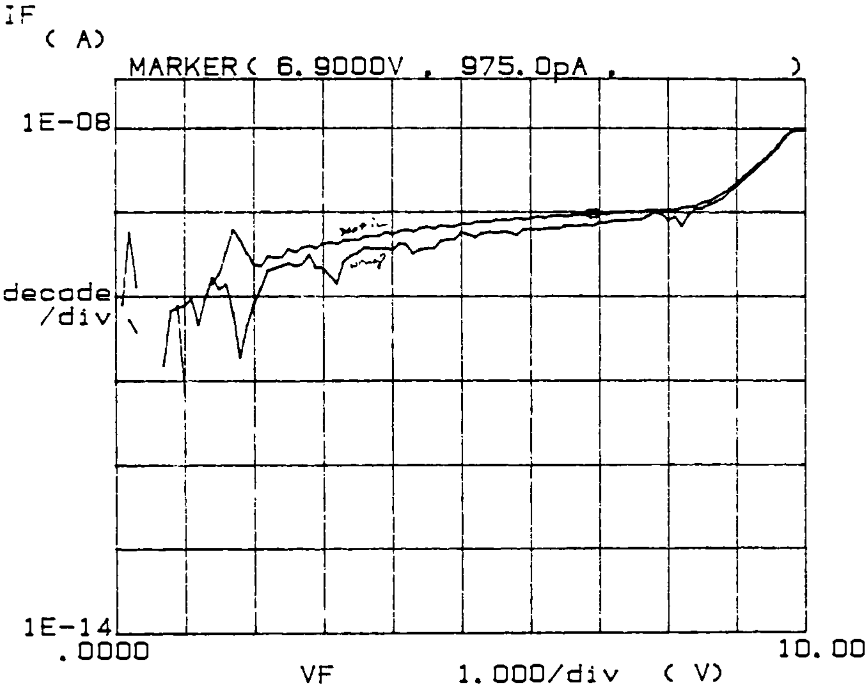


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 5.0000V
Step .050.V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

H11, 100K, POLY, D/W

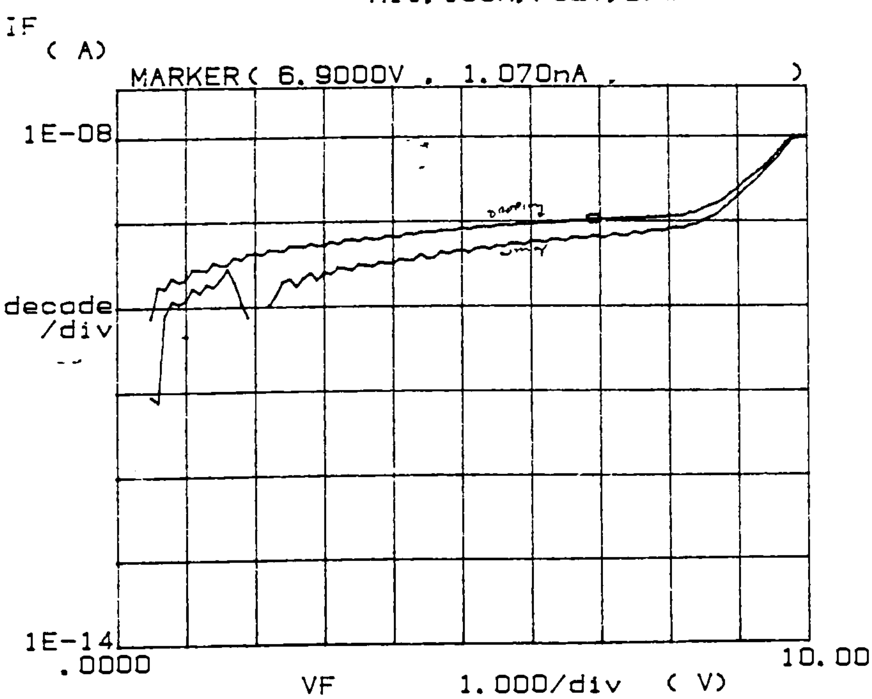


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

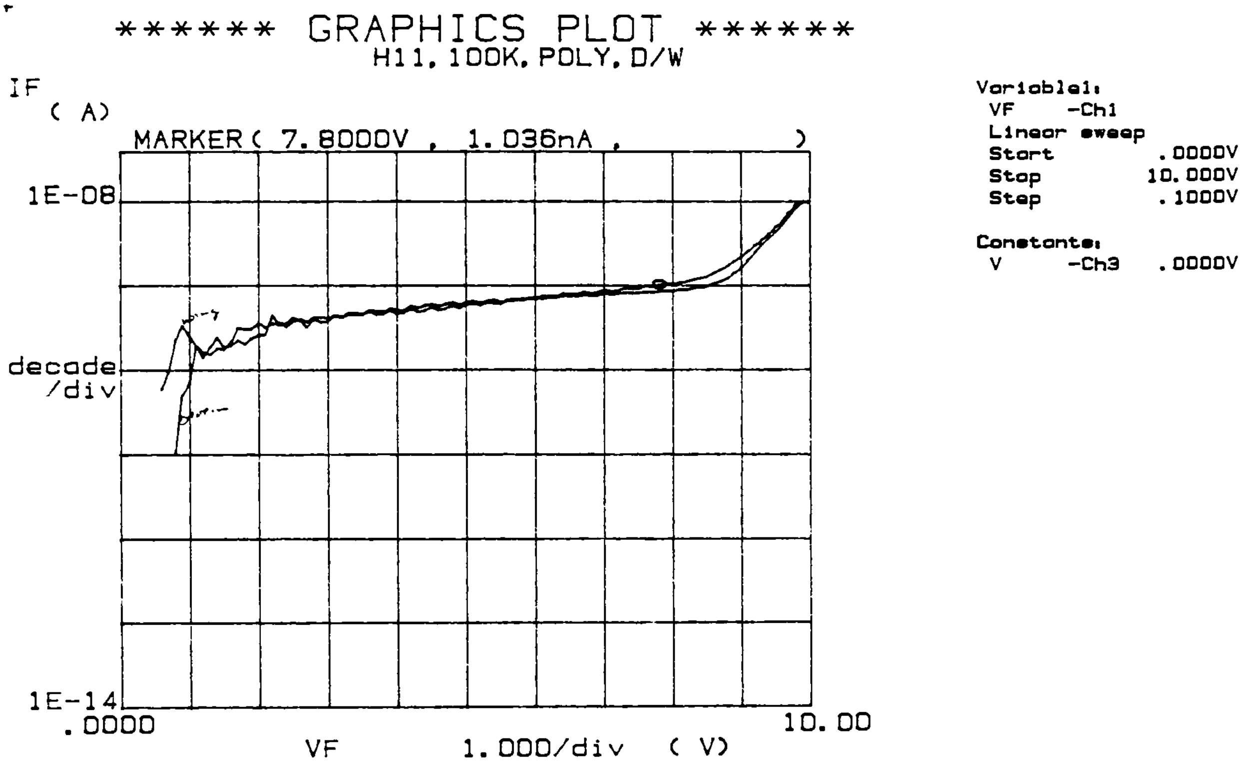
****** GRAPHICS PLOT ******

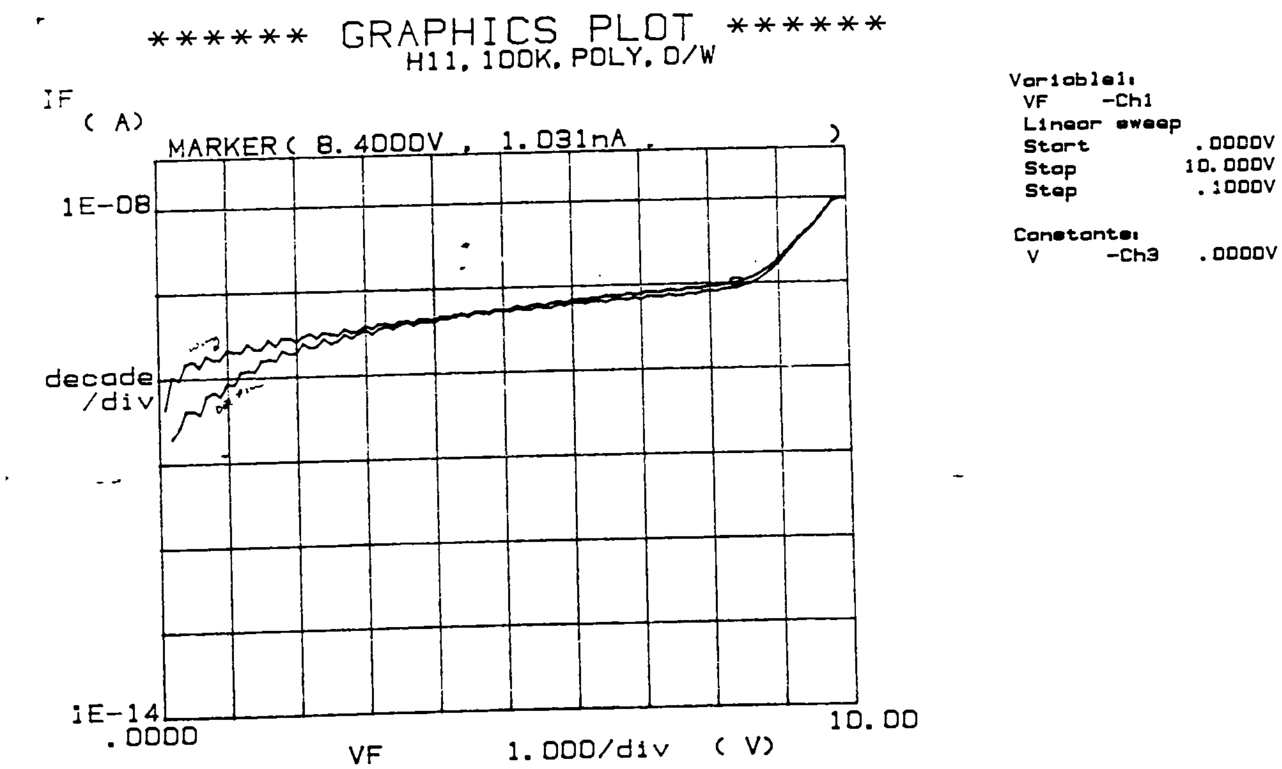
H11, 100K, POLY, D/W



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

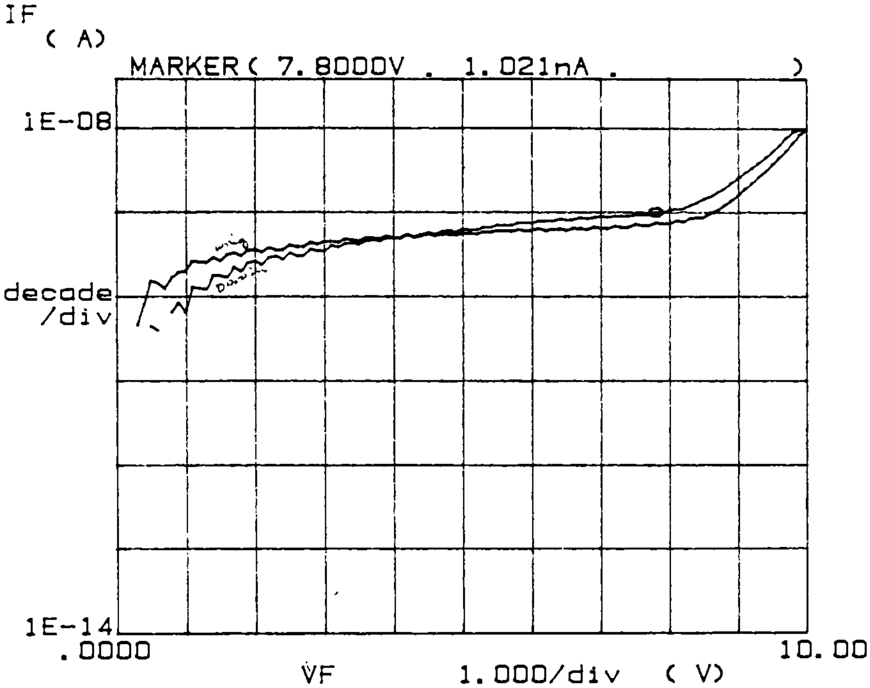
Constants:
V -Ch3 .0000V


****** GRAPHICS PLOT ******
H11, 100K, POLY, D/W
IF (A)
MARKER (7.8000V , 1.036nA ,)
1E-08
decade /div
1E-14
.0000
10.00
VF 1.000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V
Constants:
V -Ch3 .0000V


****** GRAPHICS PLOT ******
H11, 100K, POLY, D/W
IF (A)
MARKER (8.4000V , 1.031nA ,)
1E-08
decade /div
1E-14
.0000
10.00
VF 1.000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V
Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

H11, 100K, POLY, D/W

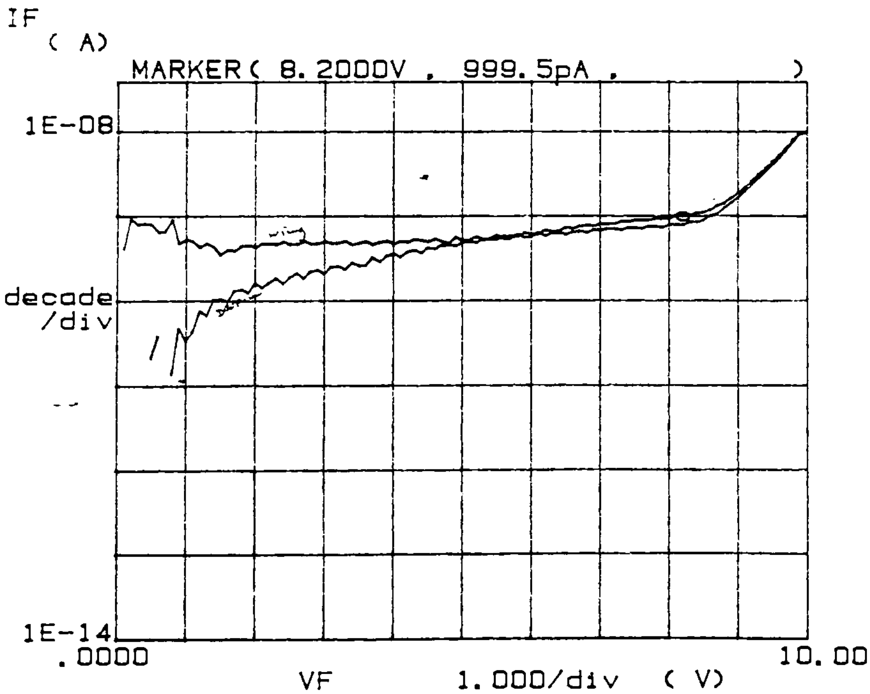


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

H11, 100K, POLY, D/W

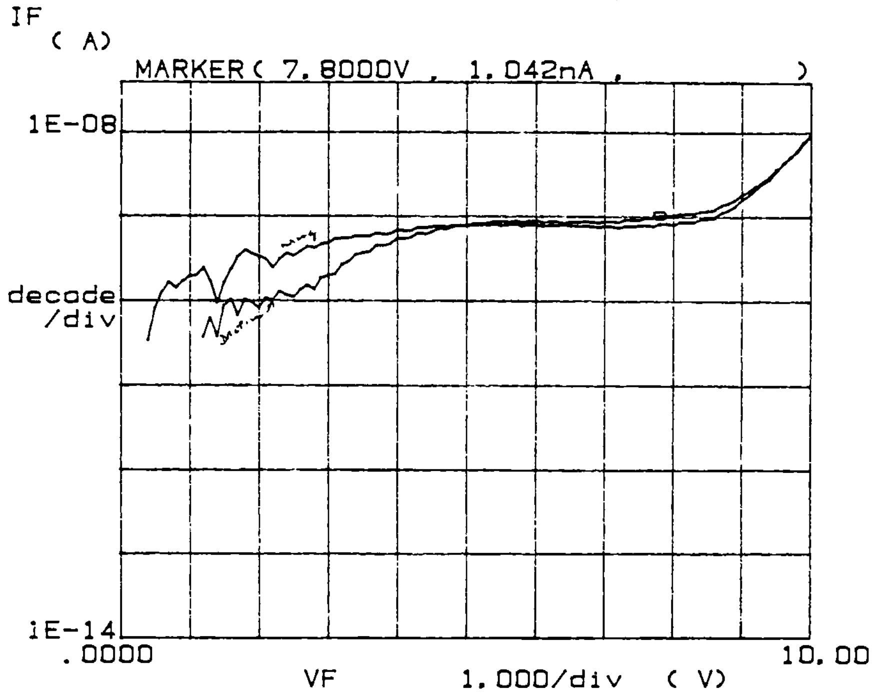


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

H11, 100K, POLY, D/W

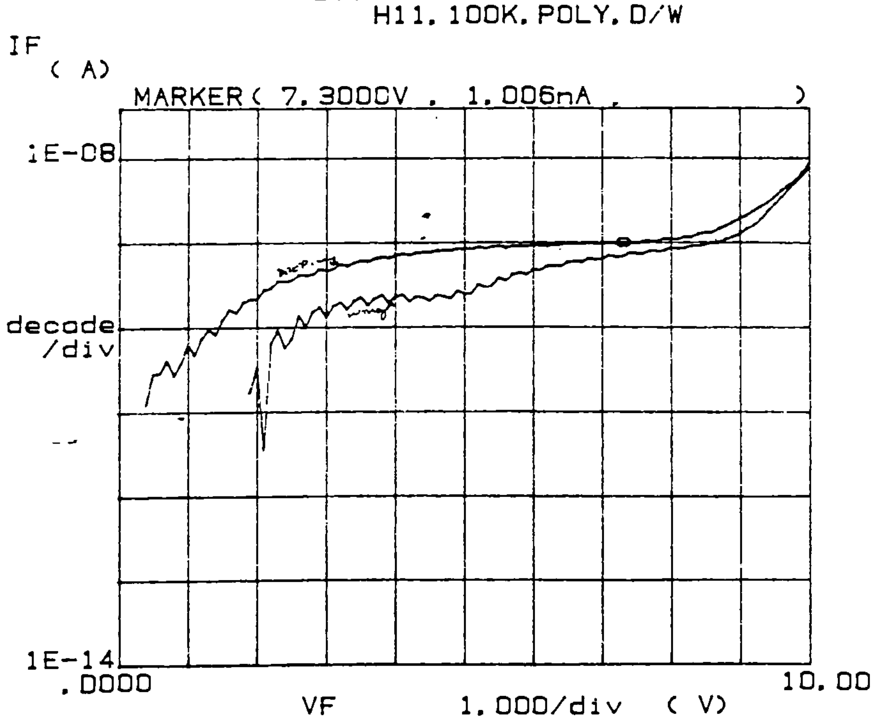


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

H11, 100K, POLY, D/W

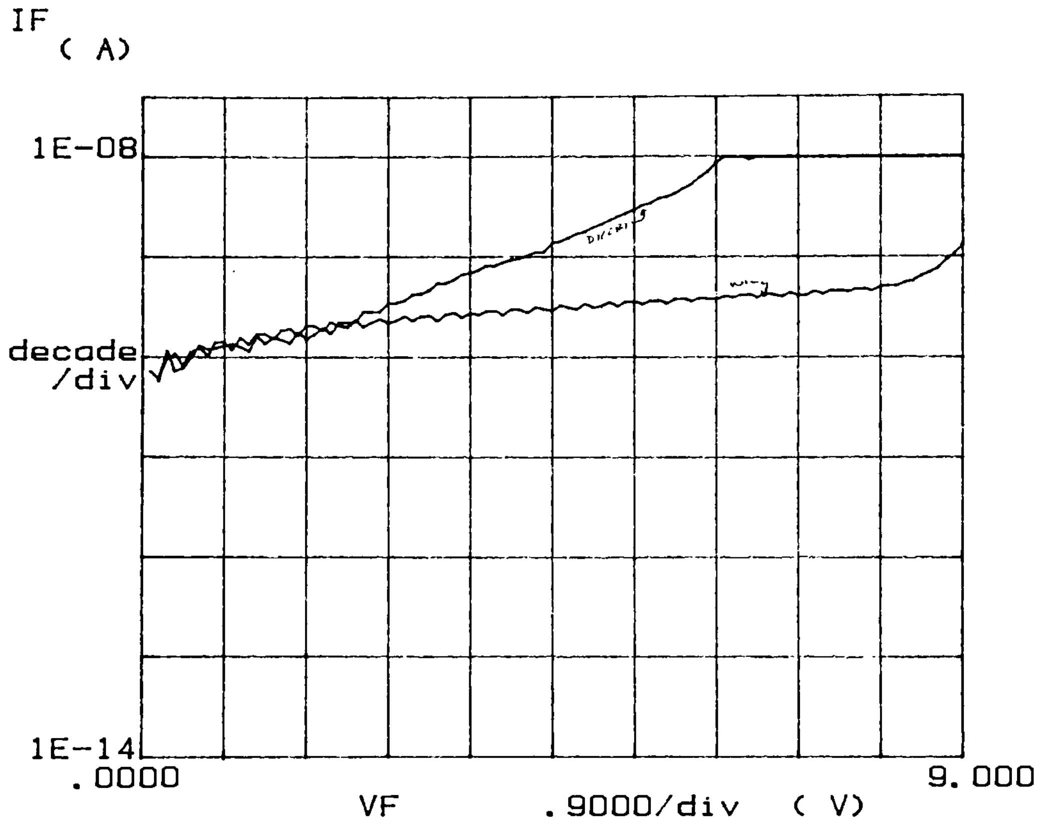


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

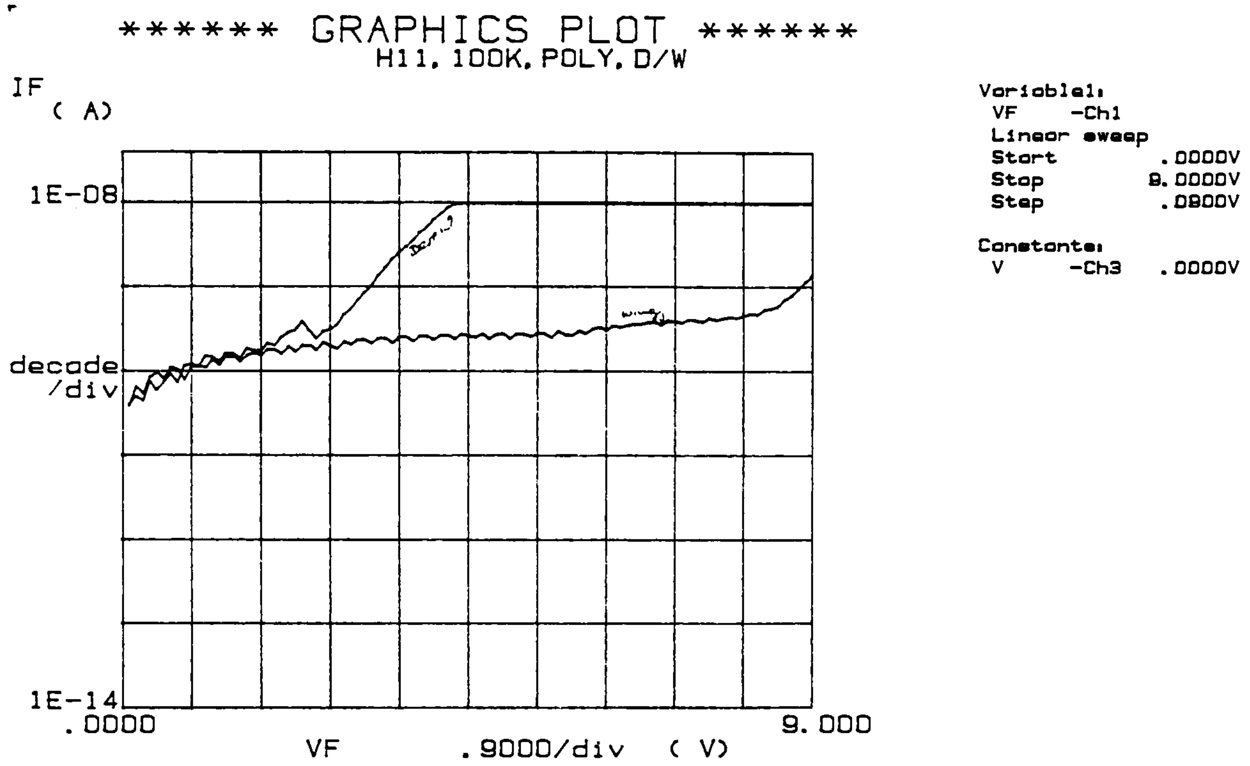
****** GRAPHICS PLOT ******

H11, 100K, POLY, D/W

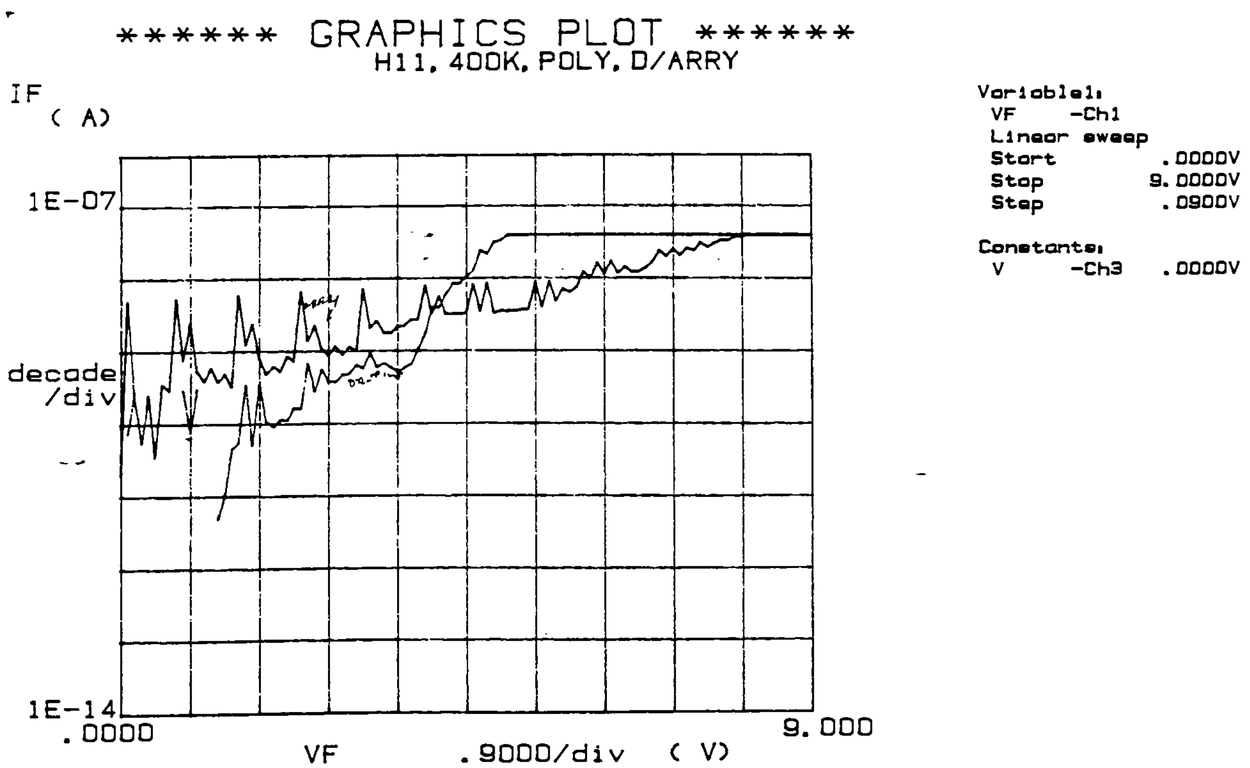


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 9.0000V
Step .0900V

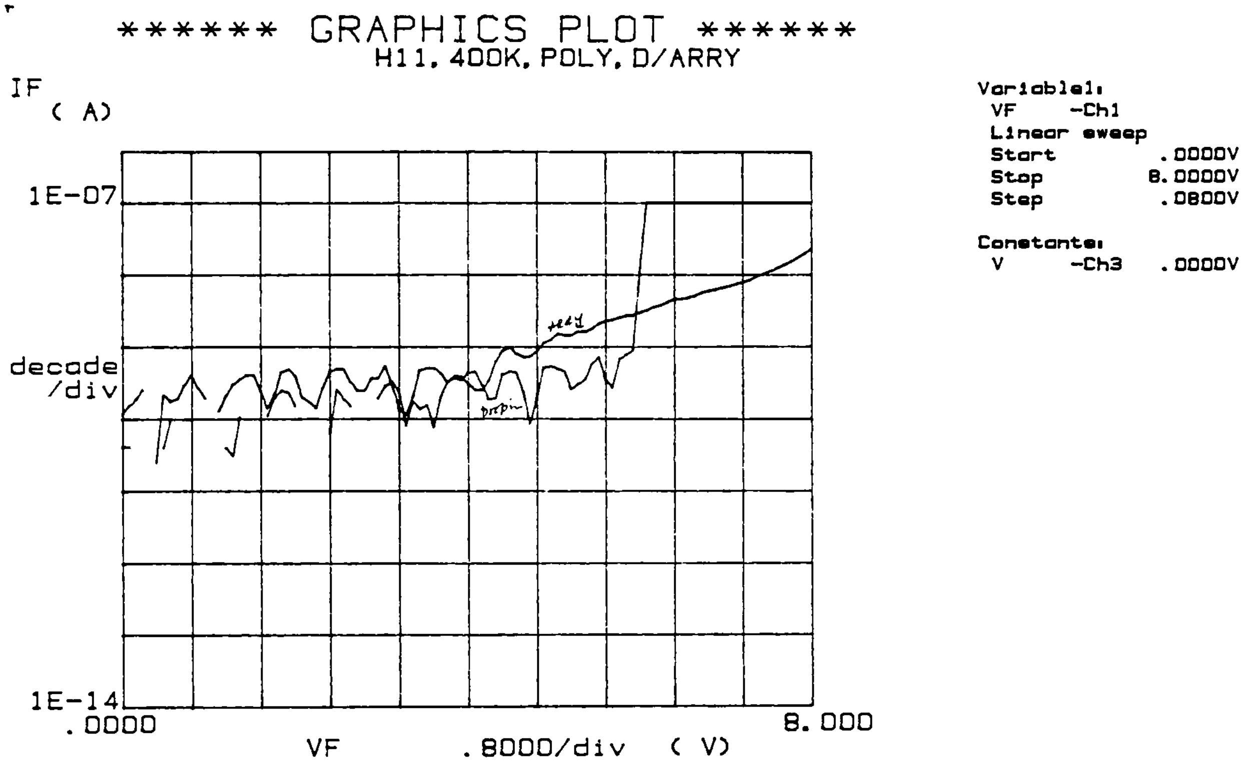
Constants:
V -Ch3 .0000V



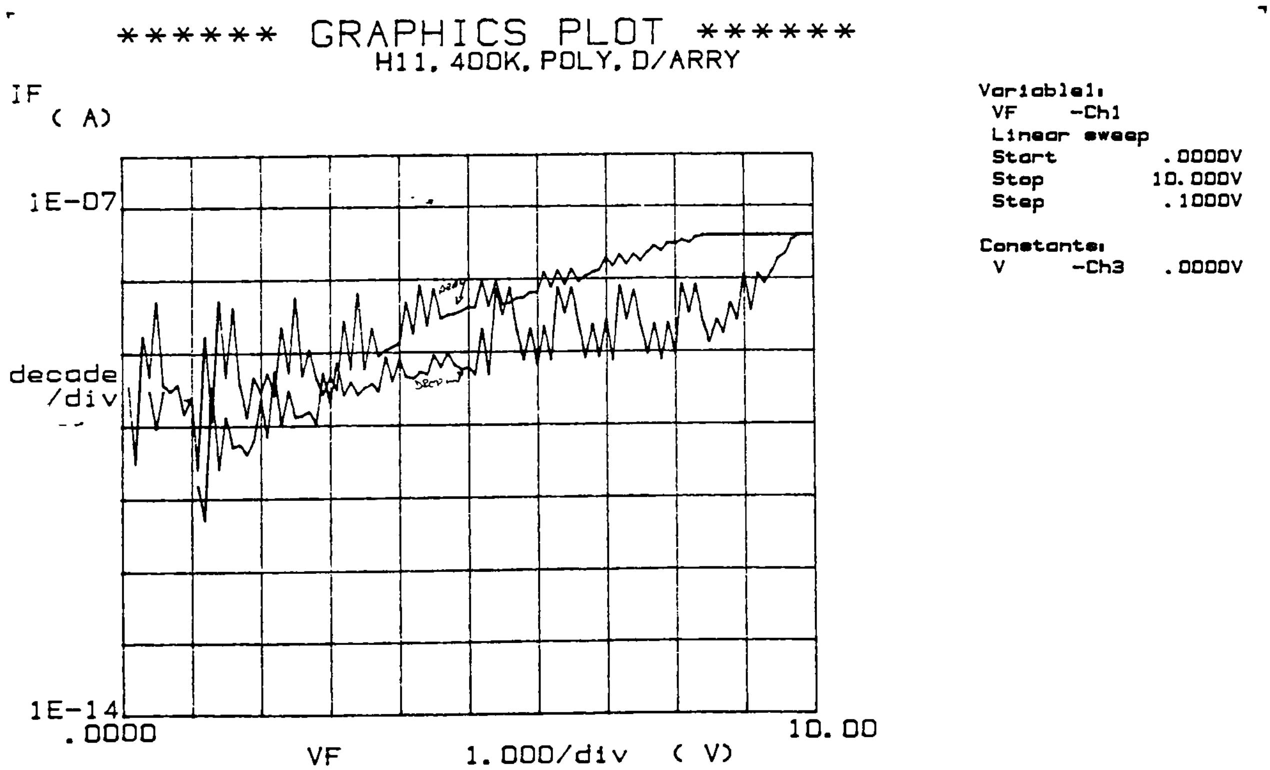
****** GRAPHICS PLOT ******
H11, 100K, POLY, D/W
IF (A)
1E-08
decade /div
1E-14
.0000
9.000
VF .9000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 9.0000V
Step .0900V
Constants:
V -Ch3 .0000V



****** GRAPHICS PLOT ******
H11, 400K, POLY, D/ARRY
IF (A)
1E-07
decade /div
1E-14
.0000
9.000
VF .9000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 9.0000V
Step .0900V
Constants:
V -Ch3 .0000V



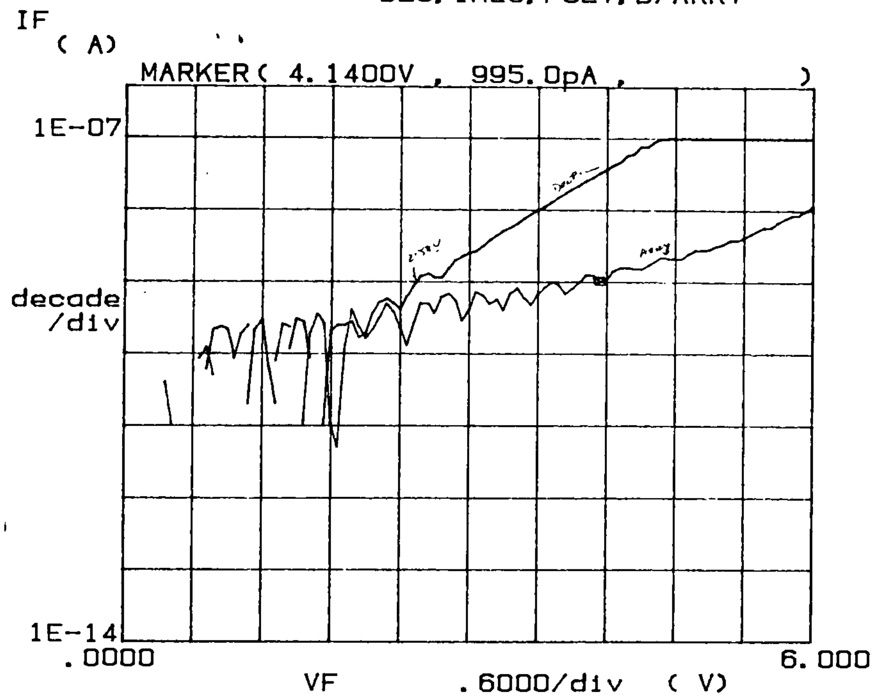
****** GRAPHICS PLOT ******
H11, 400K, POLY, D/ARRY
IF
(A)
1E-07
decade
/div
1E-14
.0000
8.000
VF .8000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 8.0000V
Step .0800V
Constants:
V -Ch3 .0000V



****** GRAPHICS PLOT ******
H11, 400K, POLY, D/ARRY
IF
(A)
1E-07
decade
/div
1E-14
.0000
10.00
VF 1.000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V
Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B20, 1MEG, POLY, D/ARRY

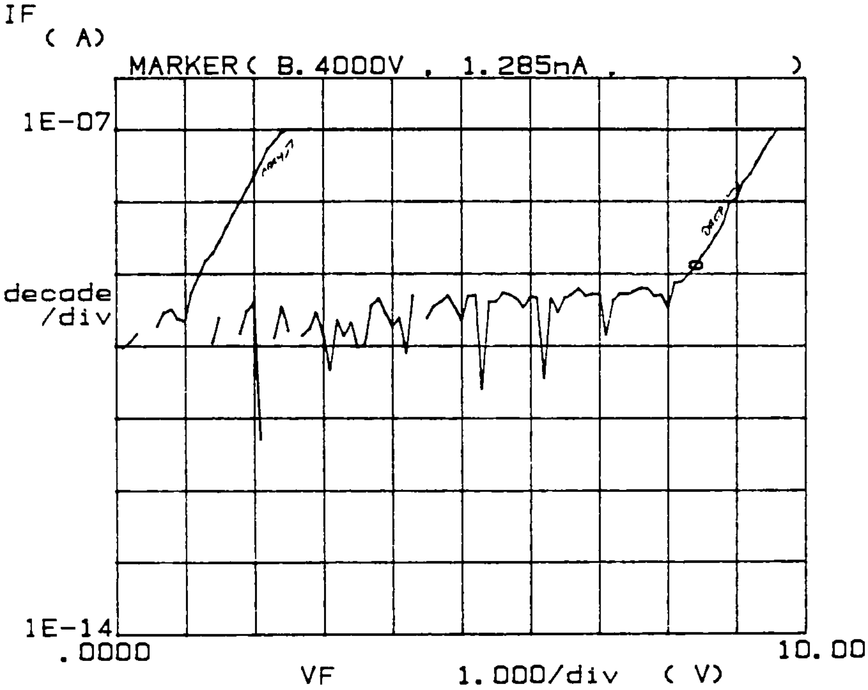


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 6.0000V
Step .0600V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B20, 1MEG, POLY, D/ARRY

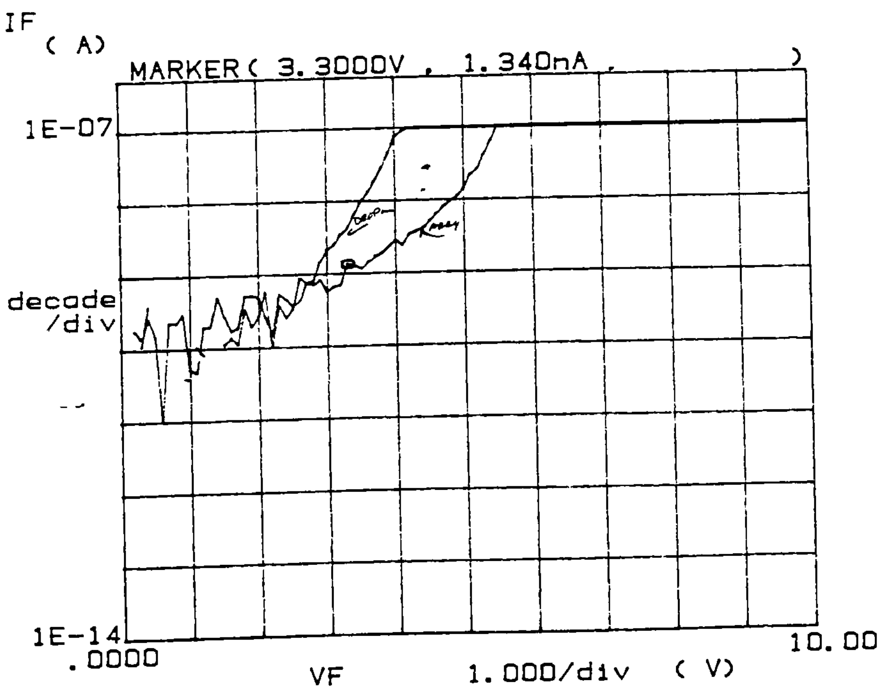


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B20, 1MEG, POLY, D/ARRY

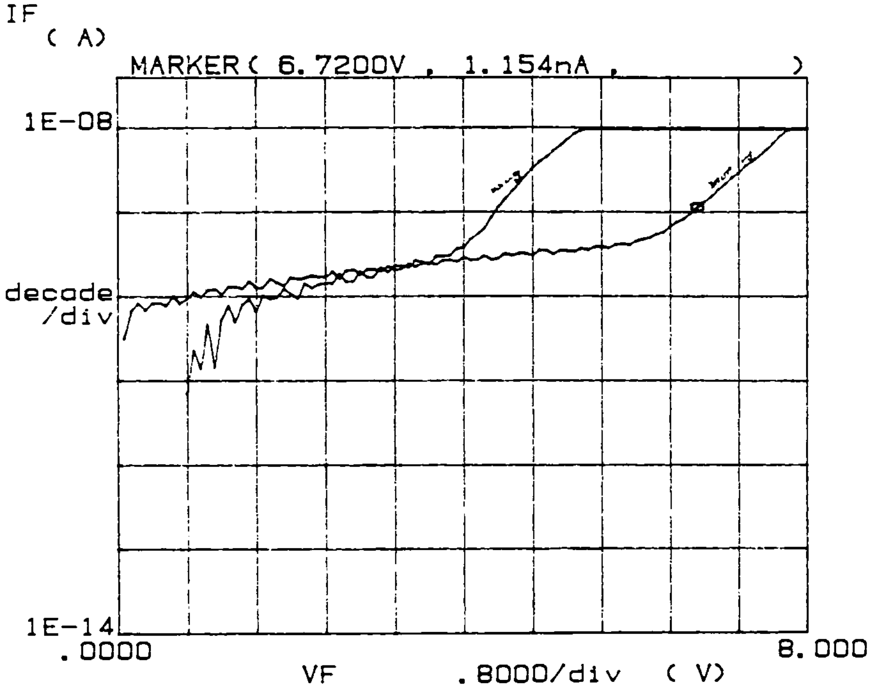


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B20, 100K, POLY, D/W

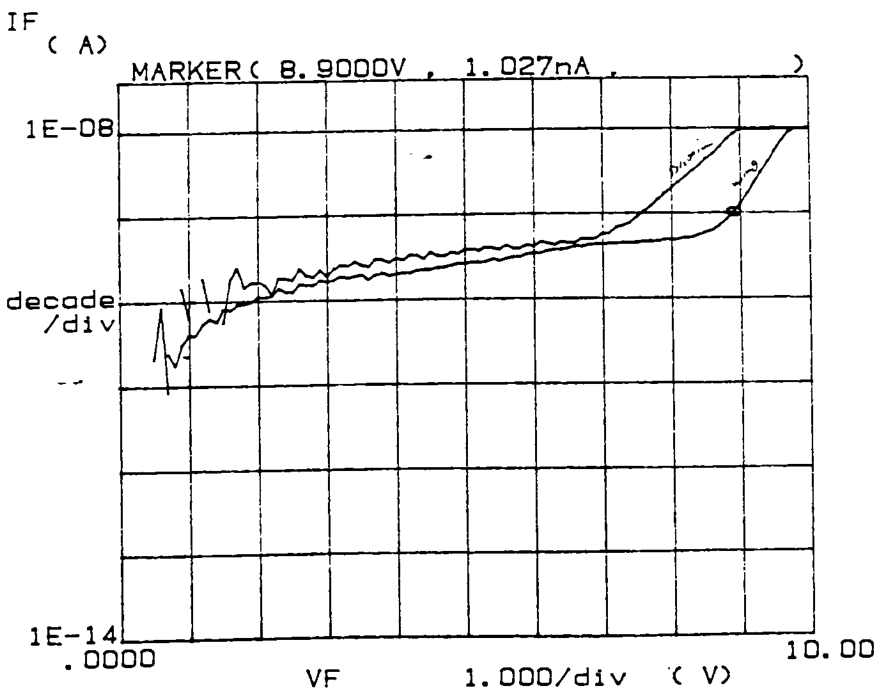


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 8.0000V
Step .0800V

Constants:
V -Ch3 .0000V

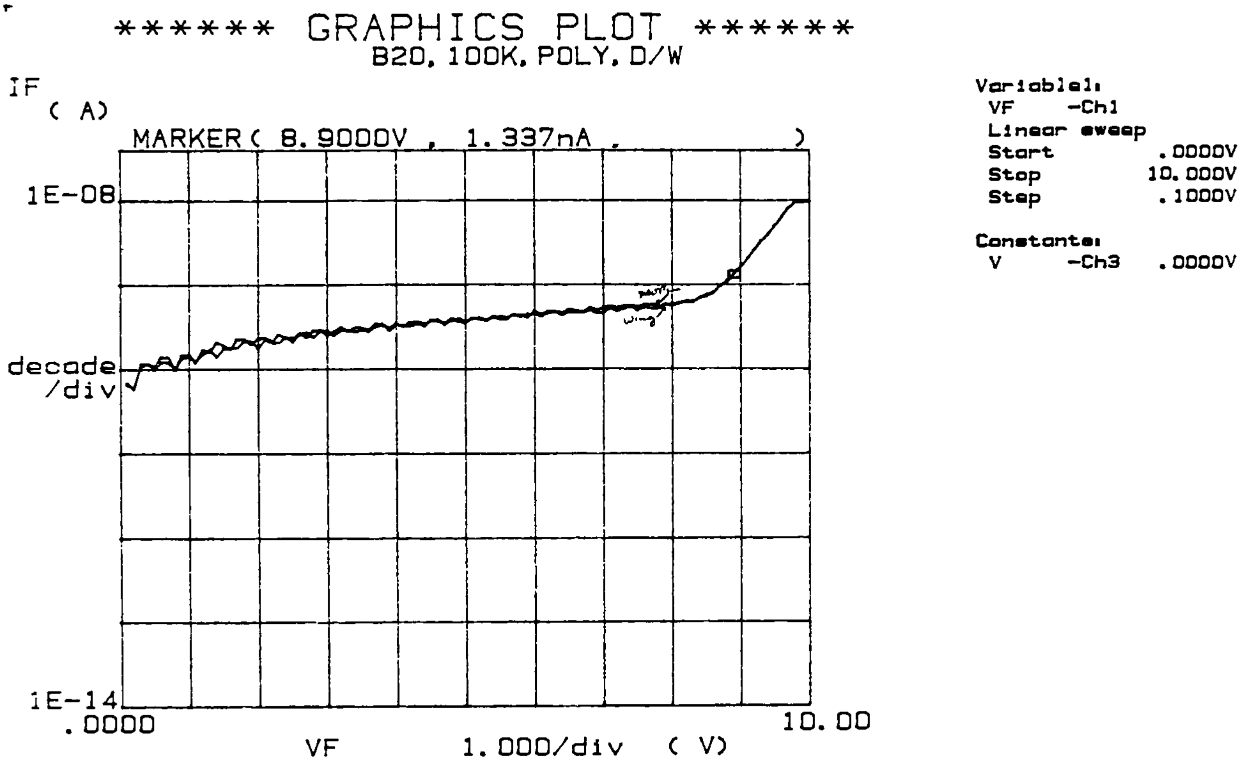
****** GRAPHICS PLOT ******

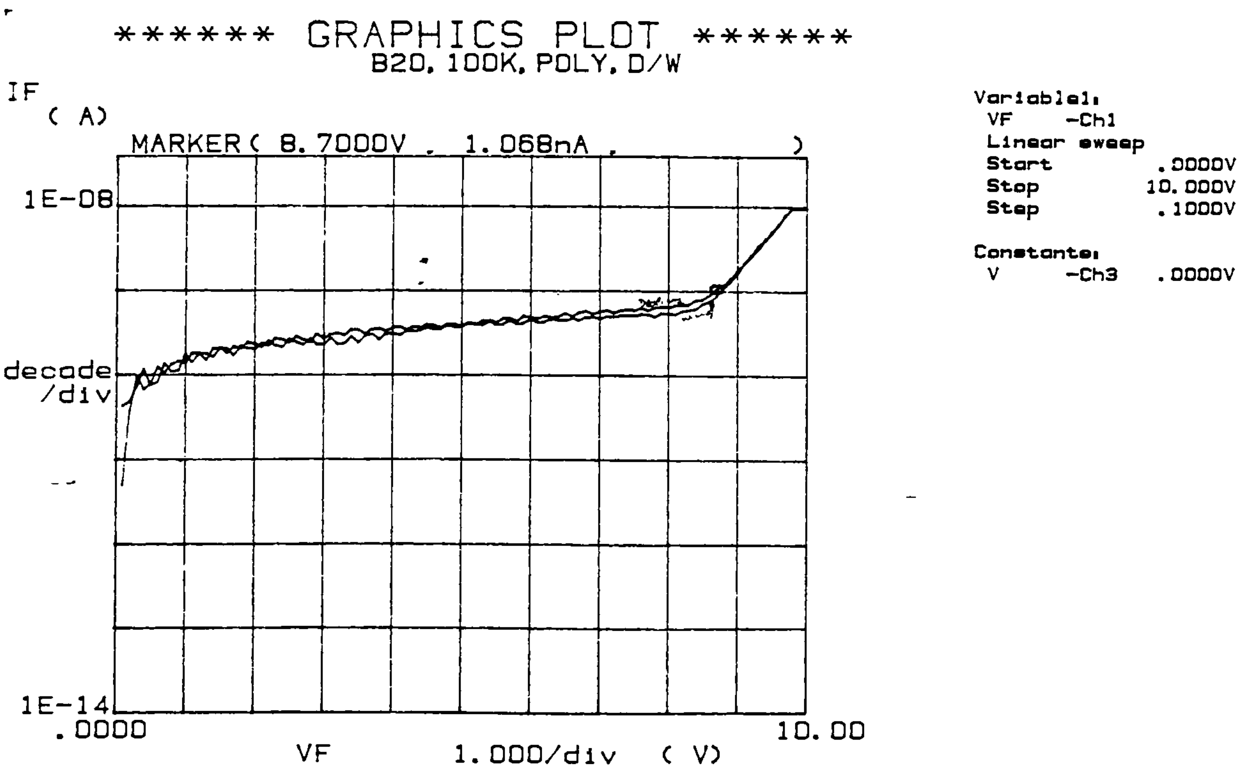
B20, 100K, POLY, D/W



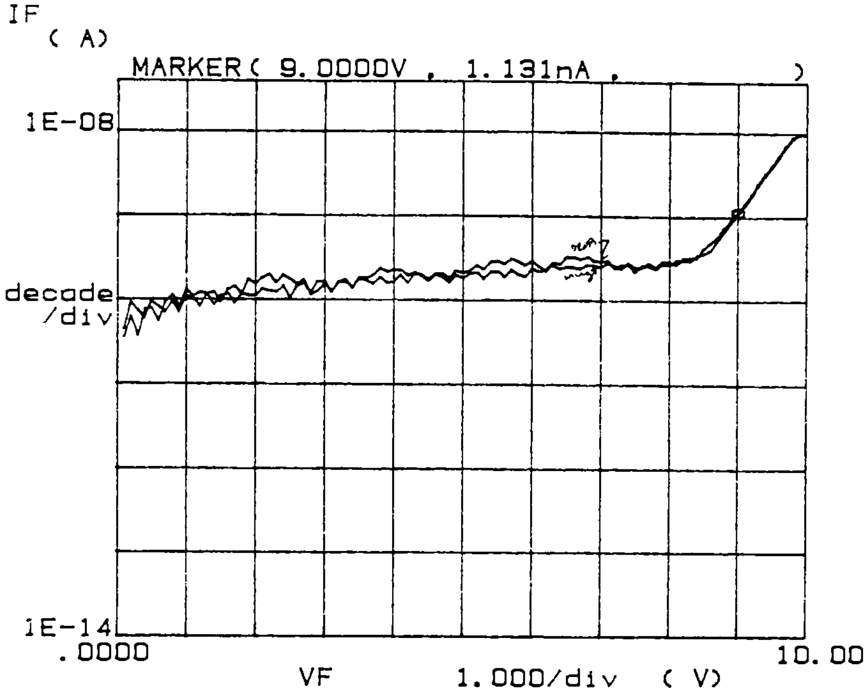
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V


****** GRAPHICS PLOT ******
B20, 100K, POLY, D/W
IF (A)
MARKER (8.9000V , 1.337nA ,)
1E-08
decade /div
1E-14
.0000
10.00
VF 1.000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V
Constants:
V -Ch3 .0000V


****** GRAPHICS PLOT ******
B20, 100K, POLY, D/W
IF (A)
MARKER (8.7000V , 1.068nA ,)
1E-08
decade /div
1E-14
.0000
10.00
VF 1.000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V
Constants:
V -Ch3 .0000V

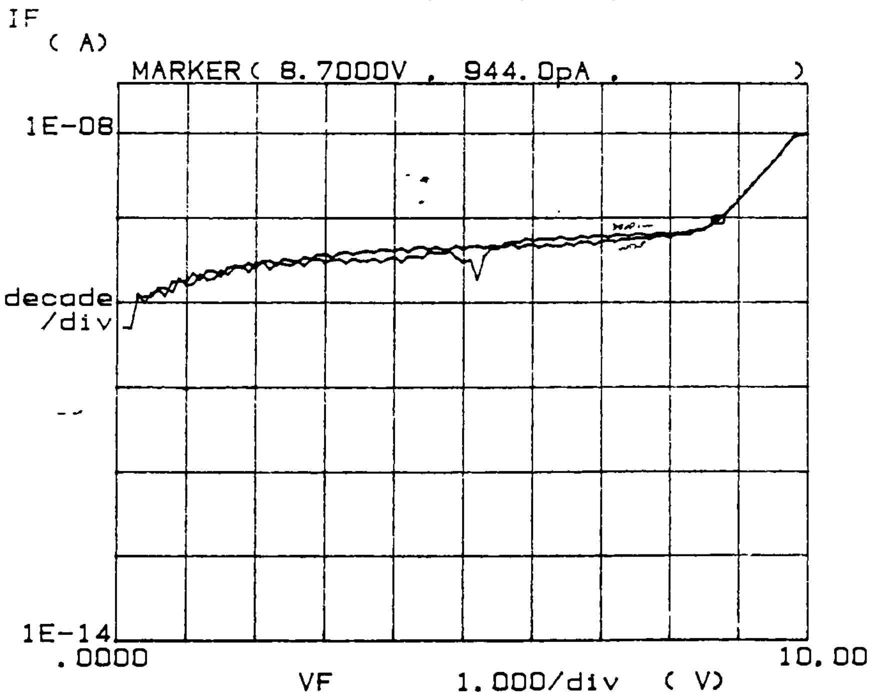
****** GRAPHICS PLOT ******
B20. 100K. POLY. D/W



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******
B20. 100K. POLY. D/W

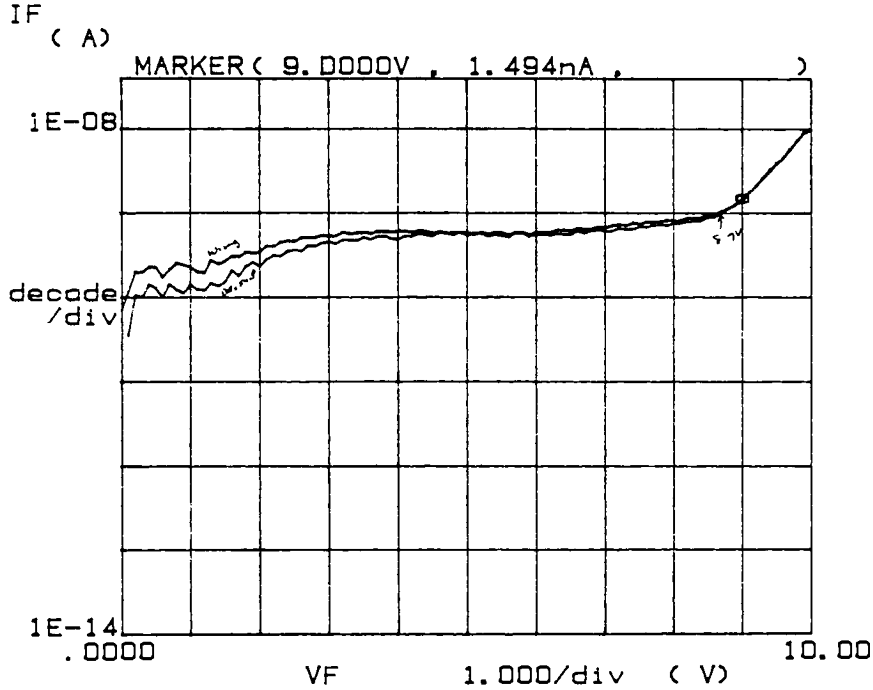


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B20, 100K, POLY, D/W

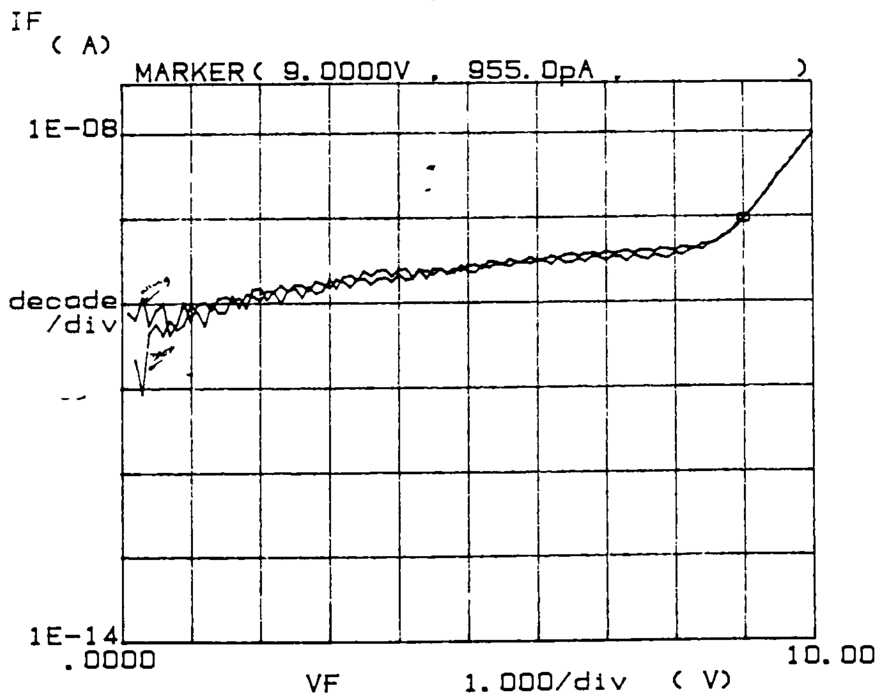


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

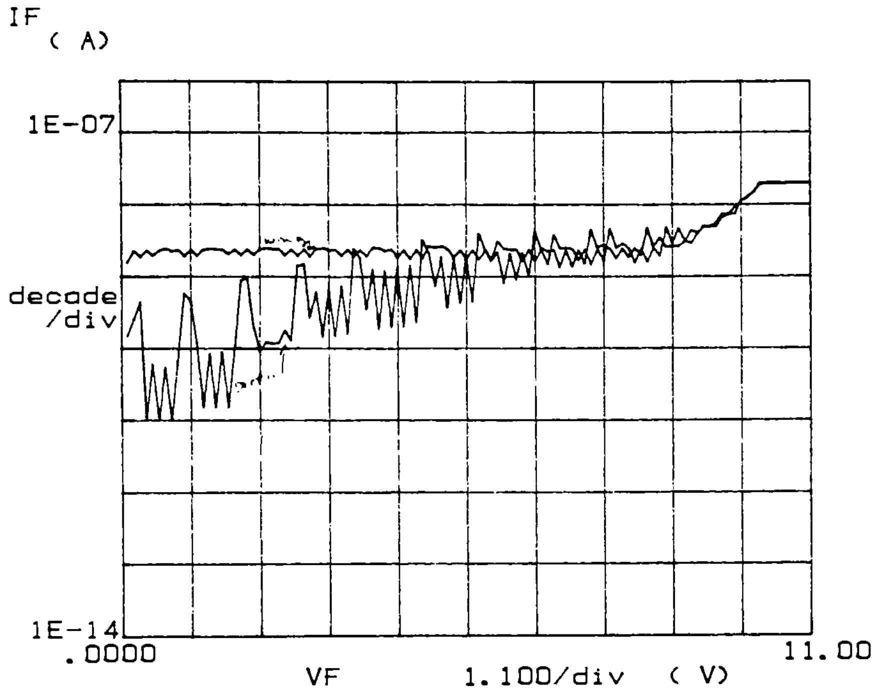
B20, 100K, POLY, D/W



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

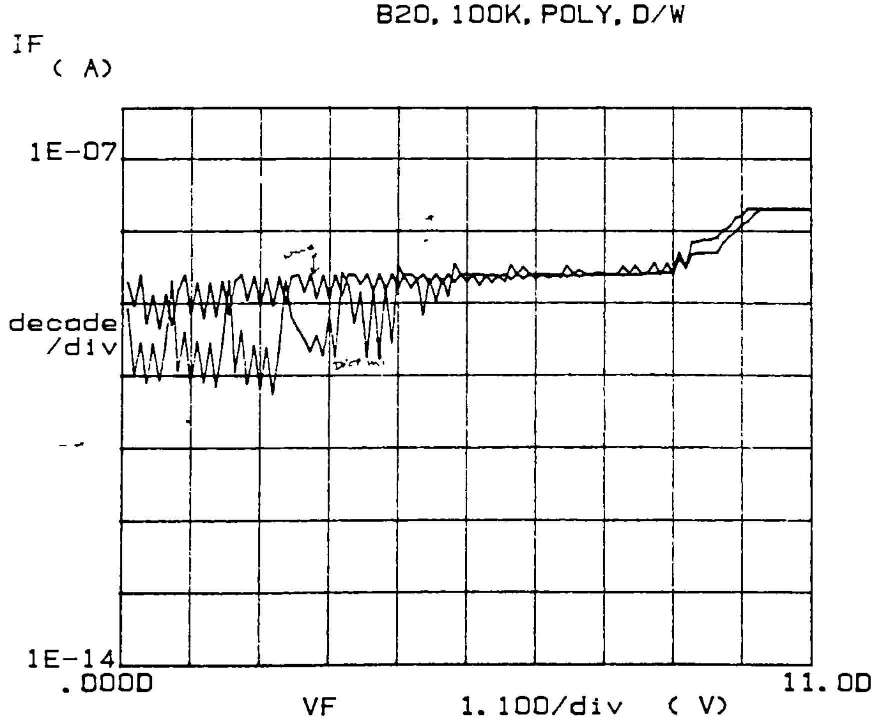
****** GRAPHICS PLOT ******
B20, 100K, POLY, D/W



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 11.000V
Step .1000V

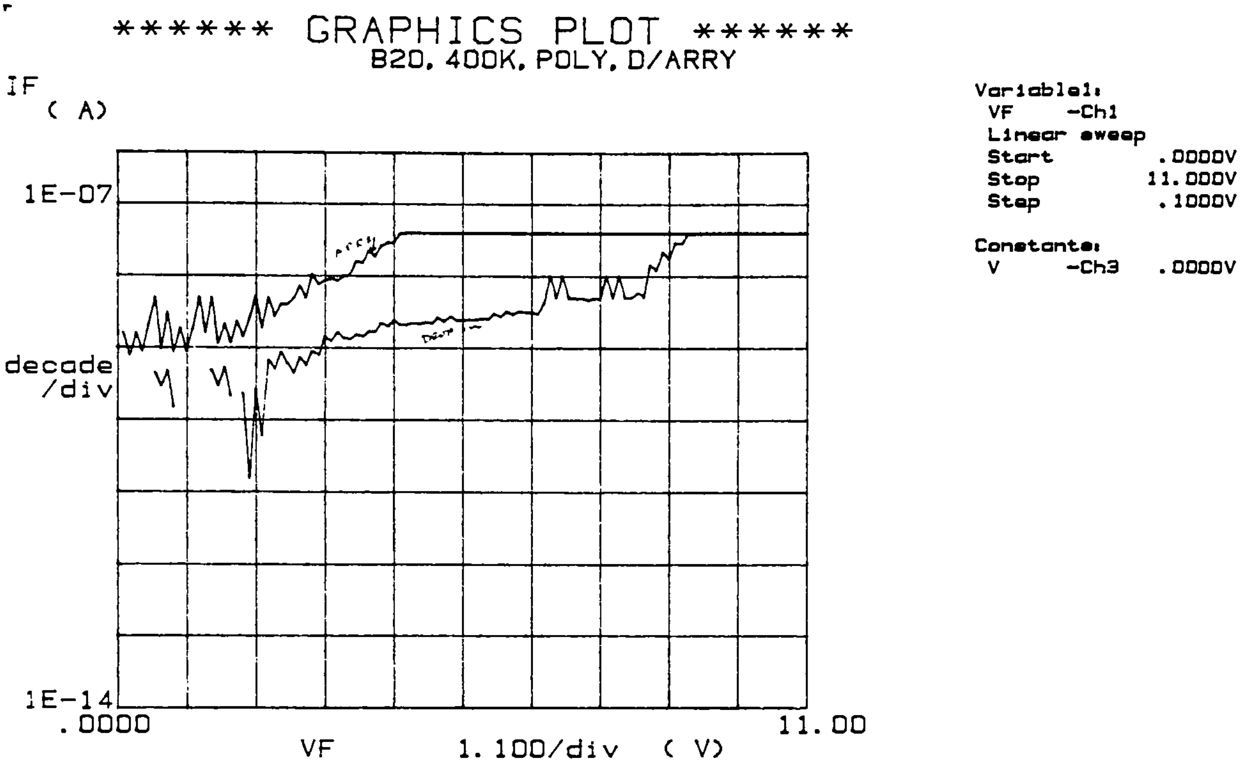
Constants:
V -Ch3 .0000V

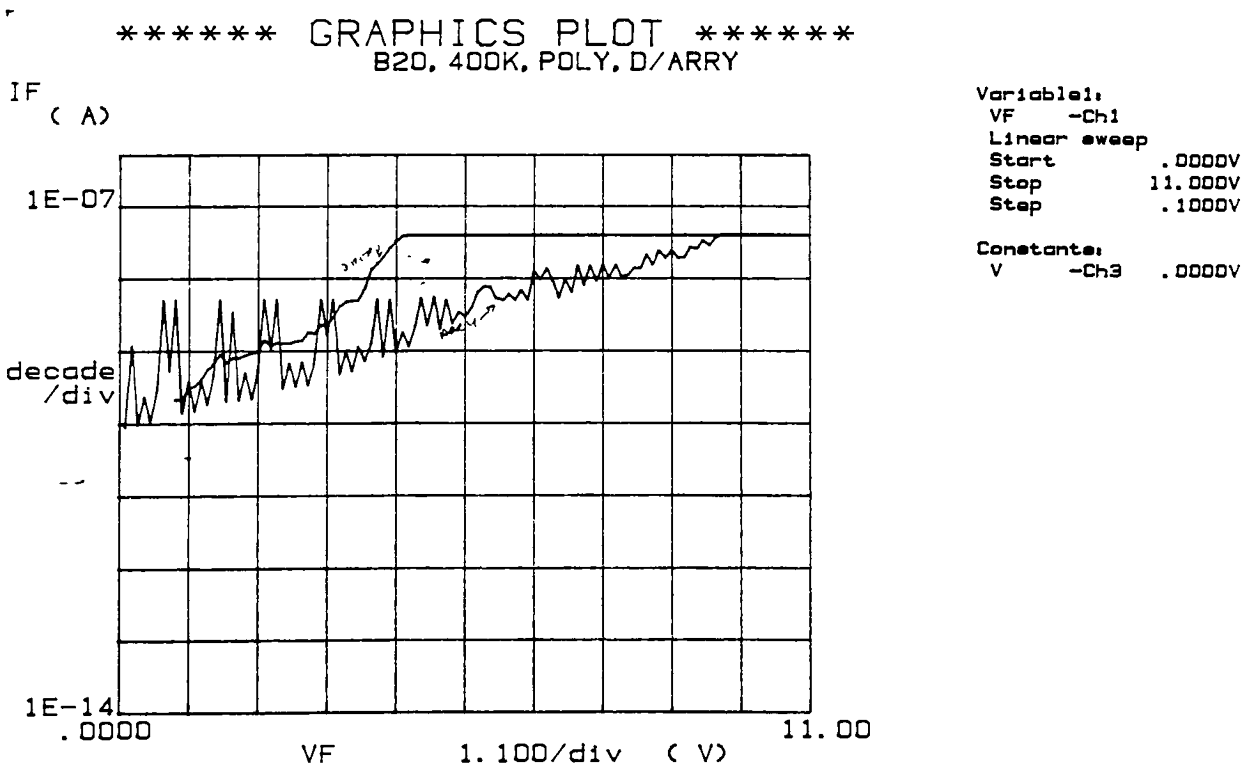
****** GRAPHICS PLOT ******
B20, 100K, POLY, D/W

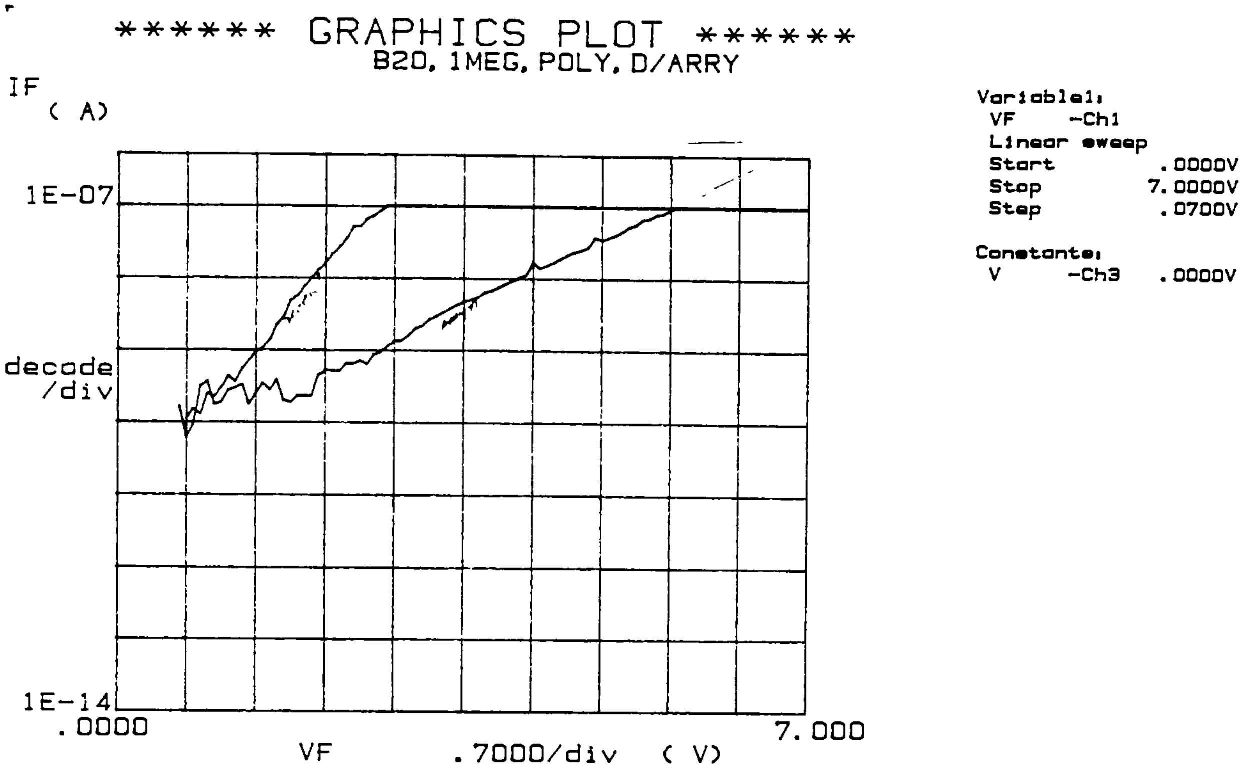


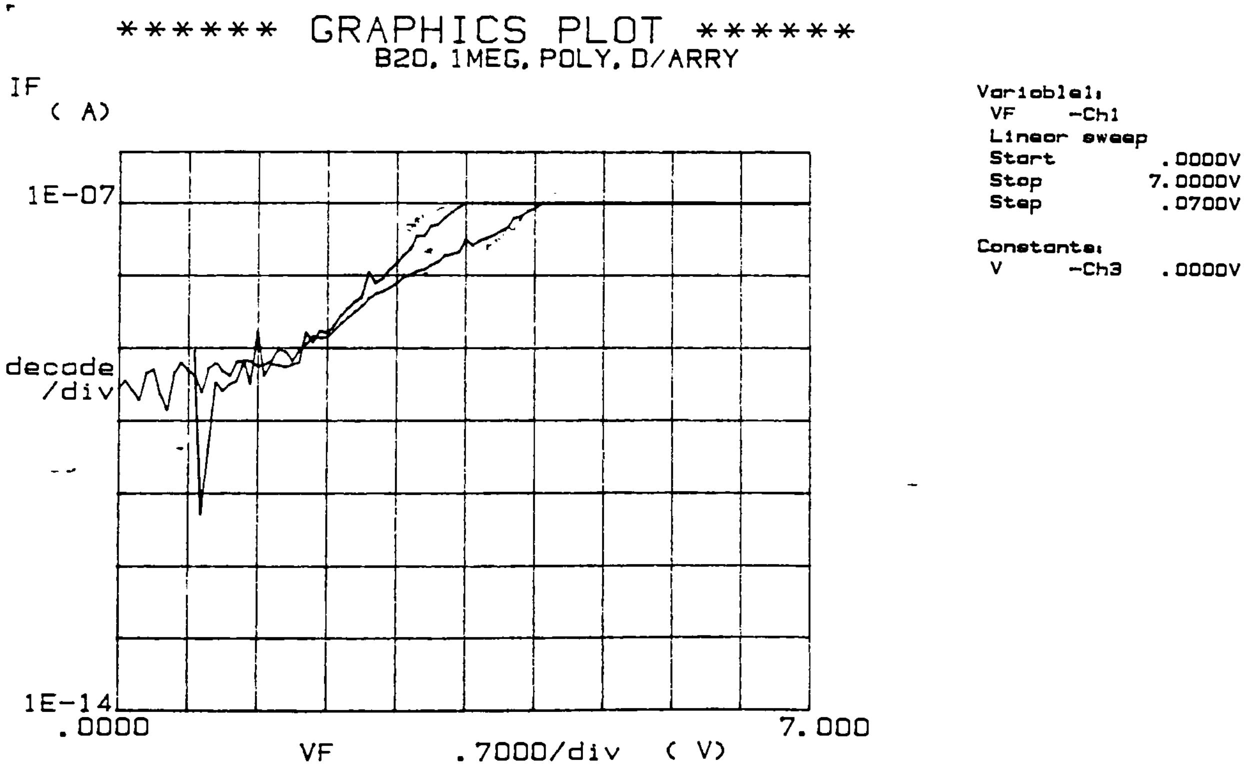
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 11.000V
Step .1000V

Constants:
V -Ch3 .0000V


****** GRAPHICS PLOT ******
B20, 400K, POLY, D/ARRY
IF (A)
1E-07
decade /div
1E-14
.0000
11.00
VF 1.100/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 11.000V
Step .1000V
Constants:
V -Ch3 .0000V


****** GRAPHICS PLOT ******
B20, 400K, POLY, D/ARRY
IF (A)
1E-07
decade /div
1E-14
.0000
11.00
VF 1.100/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 11.000V
Step .1000V
Constants:
V -Ch3 .0000V

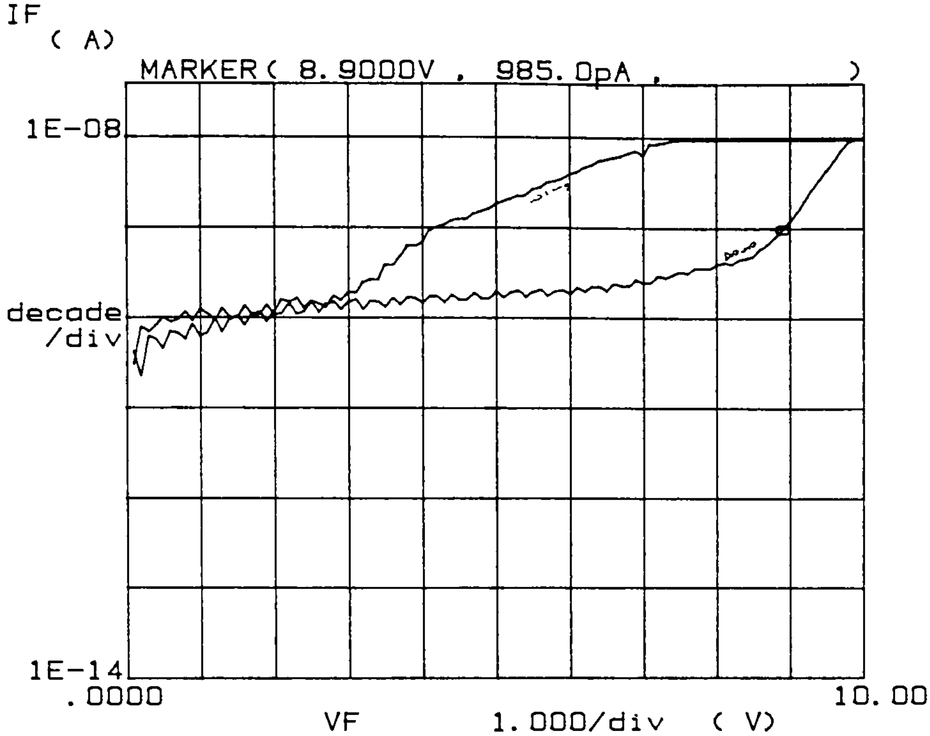

****** GRAPHICS PLOT ******
B20, 1MEG, POLY, D/ARRY
IF
(A)
1E-07
decade
/div
1E-14
.0000
7.000
VF
.7000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 7.0000V
Step .0700V
Constants:
V -Ch3 .0000V


****** GRAPHICS PLOT ******
B20, 1MEG, POLY, D/ARRY
IF
(A)
1E-07
decade
/div
1E-14
.0000
7.000
VF
.7000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 7.0000V
Step .0700V
Constants:
V -Ch3 .0000V

4500 Å Etch Back Results

****** GRAPHICS PLOT ******

H07, 100K, POLY, D/W

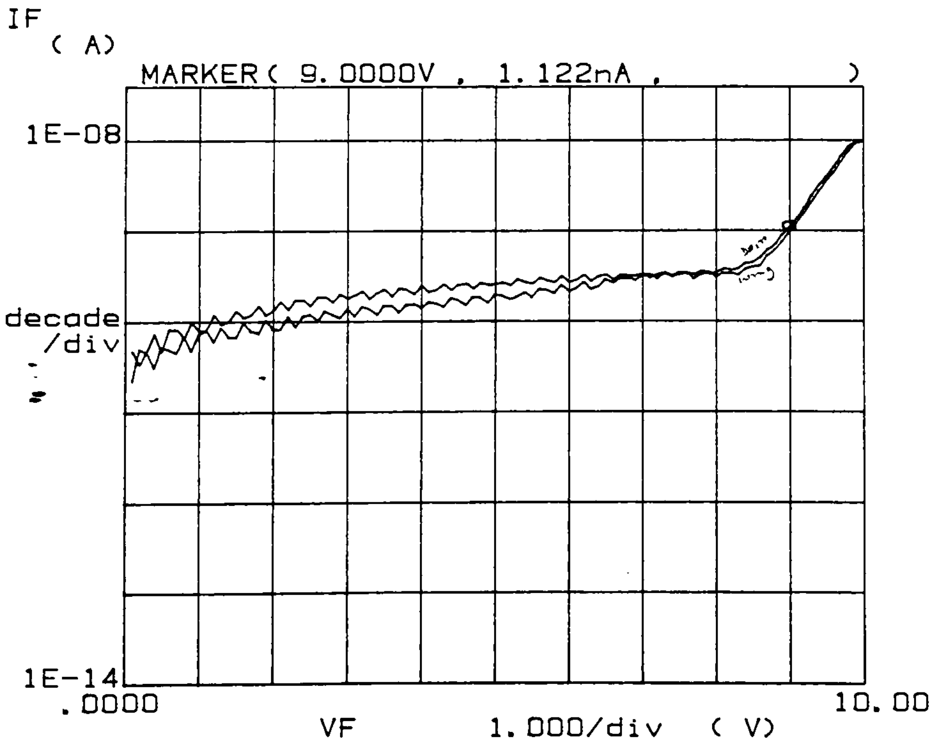


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

H07, 100K, POLY, D/W

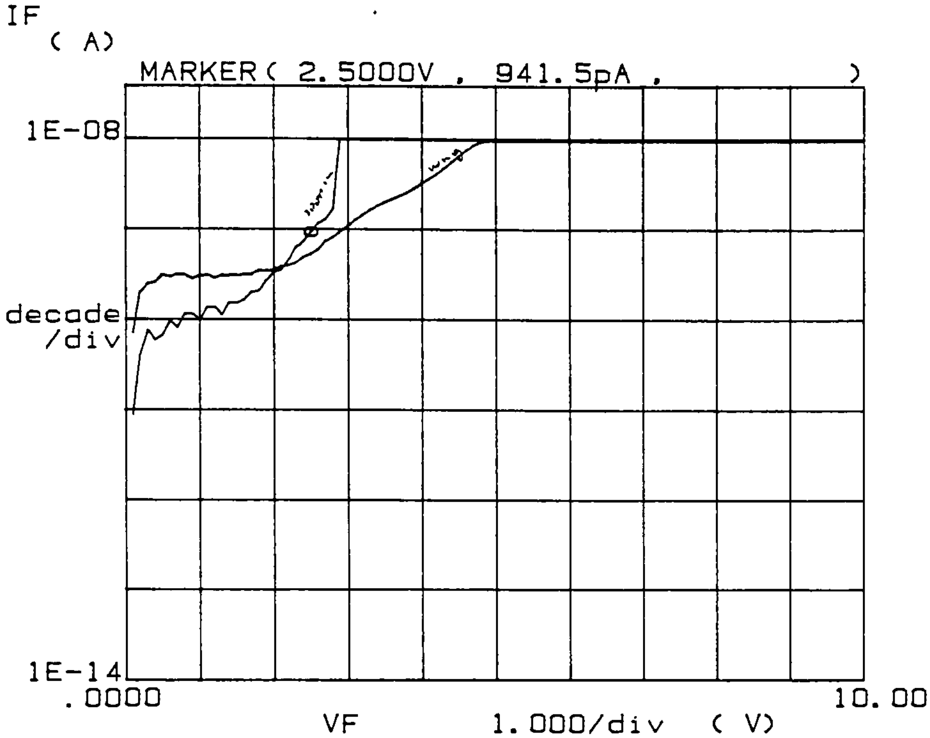


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

H07, 100K, POLY, D/W

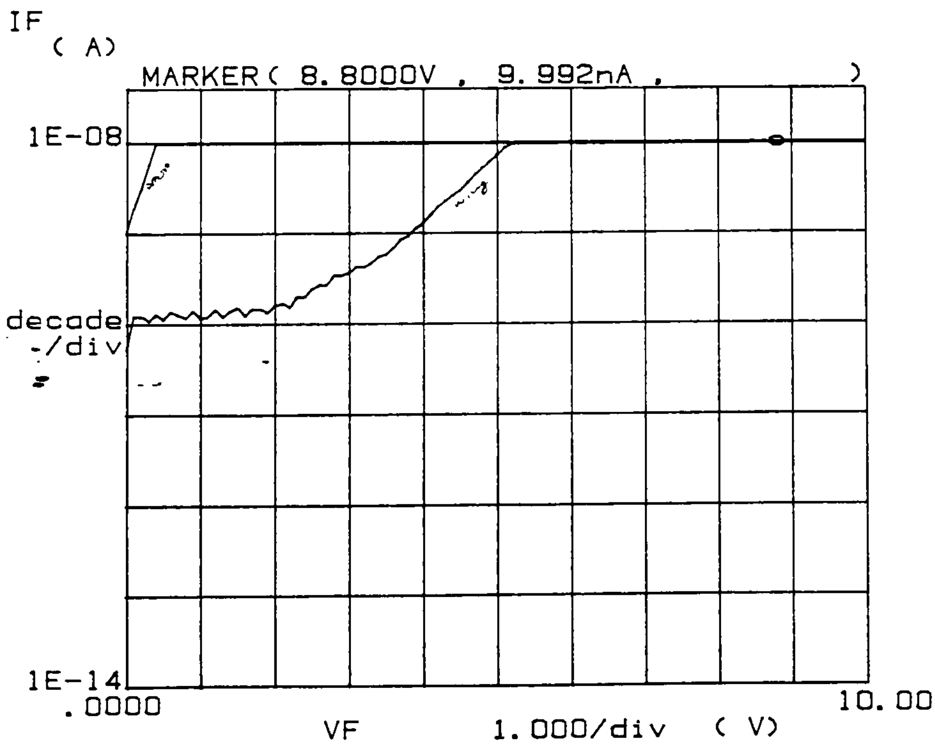


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

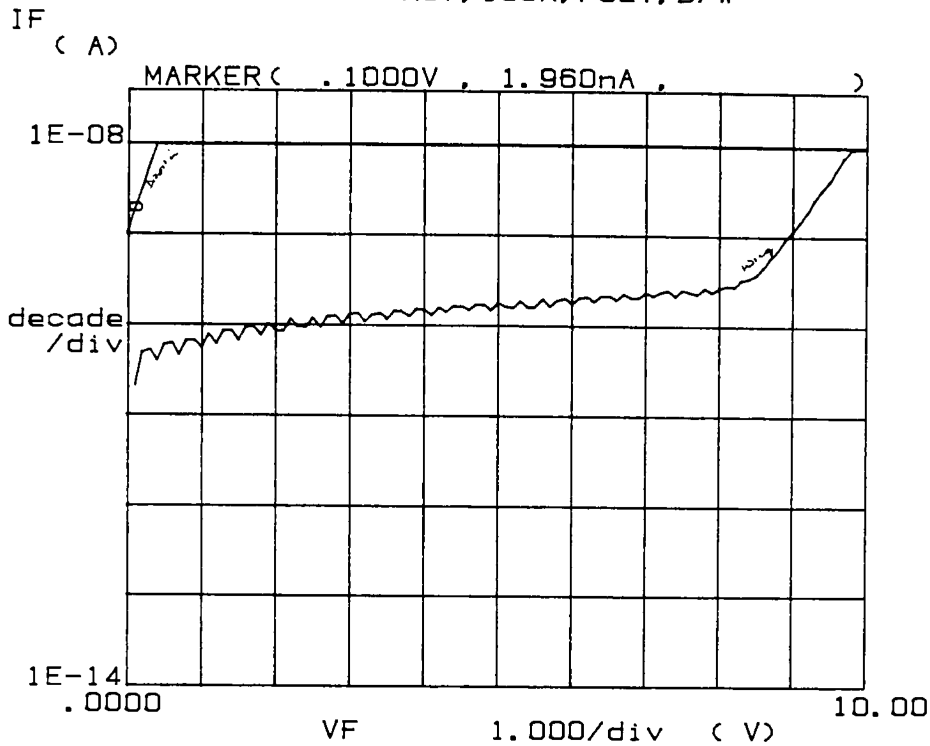
H07, 100K, POLY, D/W



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

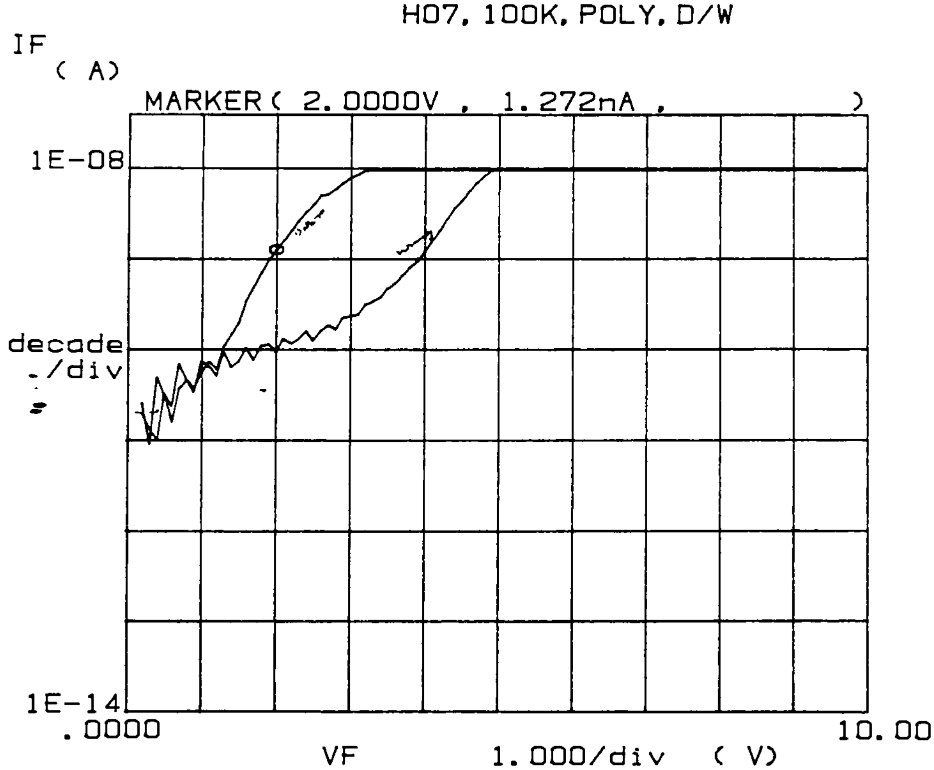
****** GRAPHICS PLOT ******
H07, 100K, POLY, D/W



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

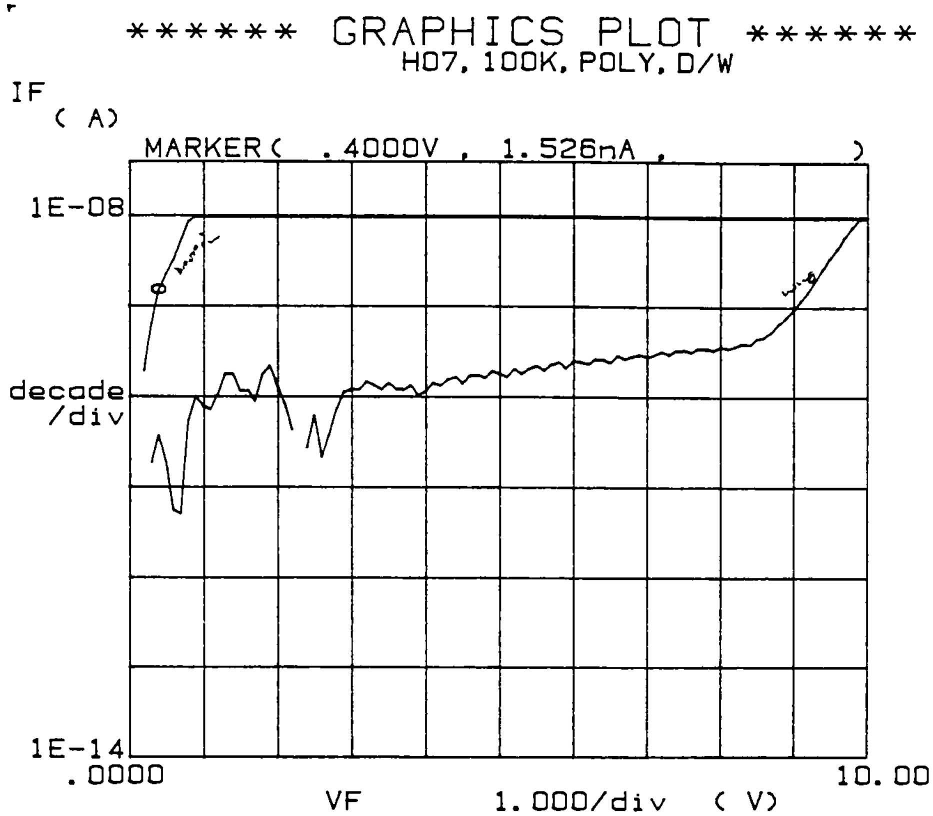
Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******
H07, 100K, POLY, D/W



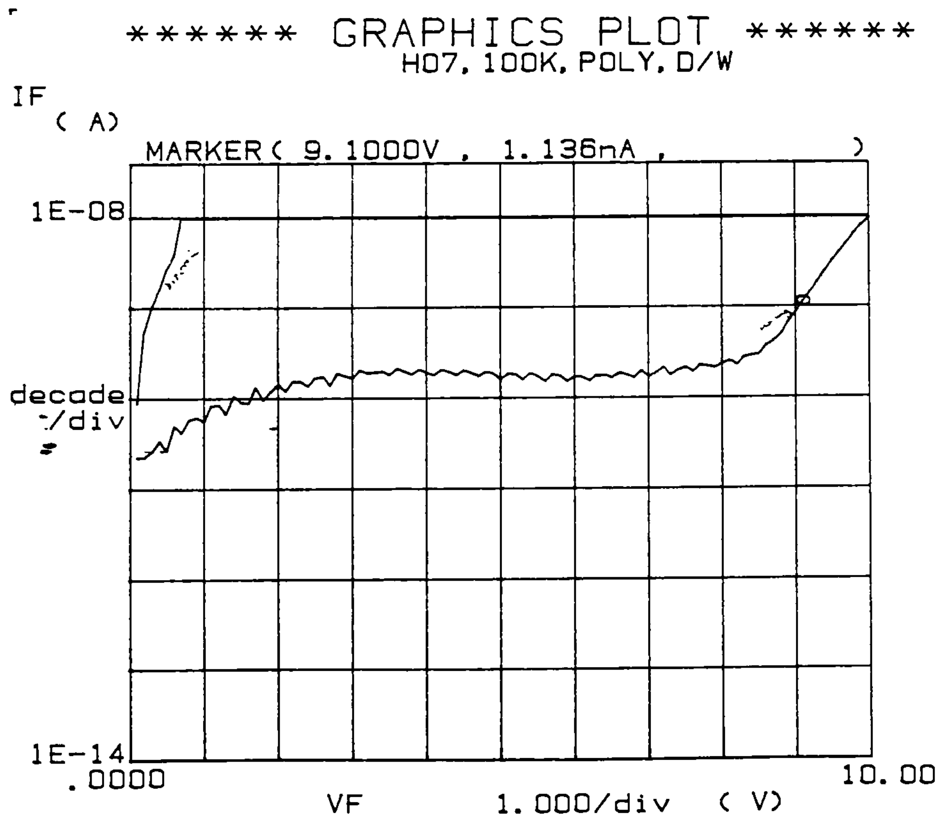
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

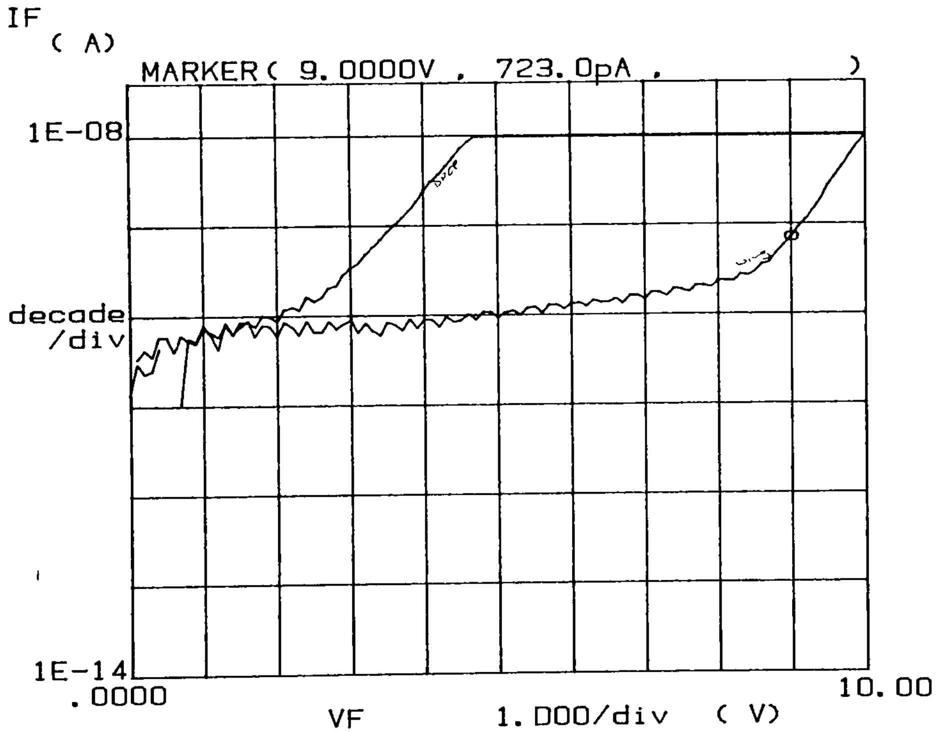


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

H08, 100K, POLY, D/W

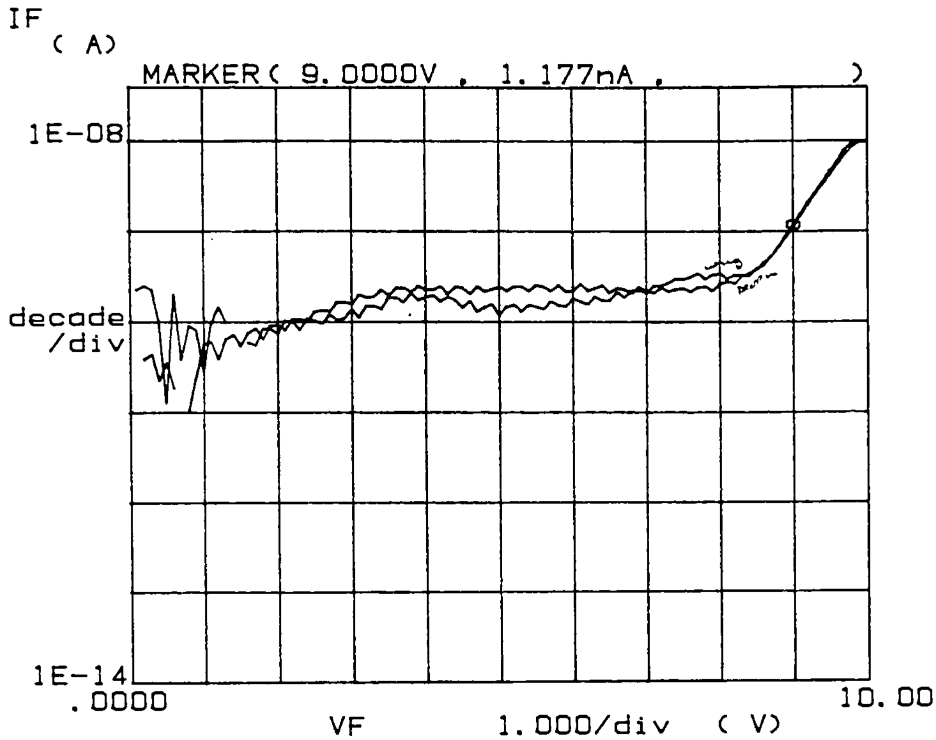


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

H08, 100K, POLY, D/W

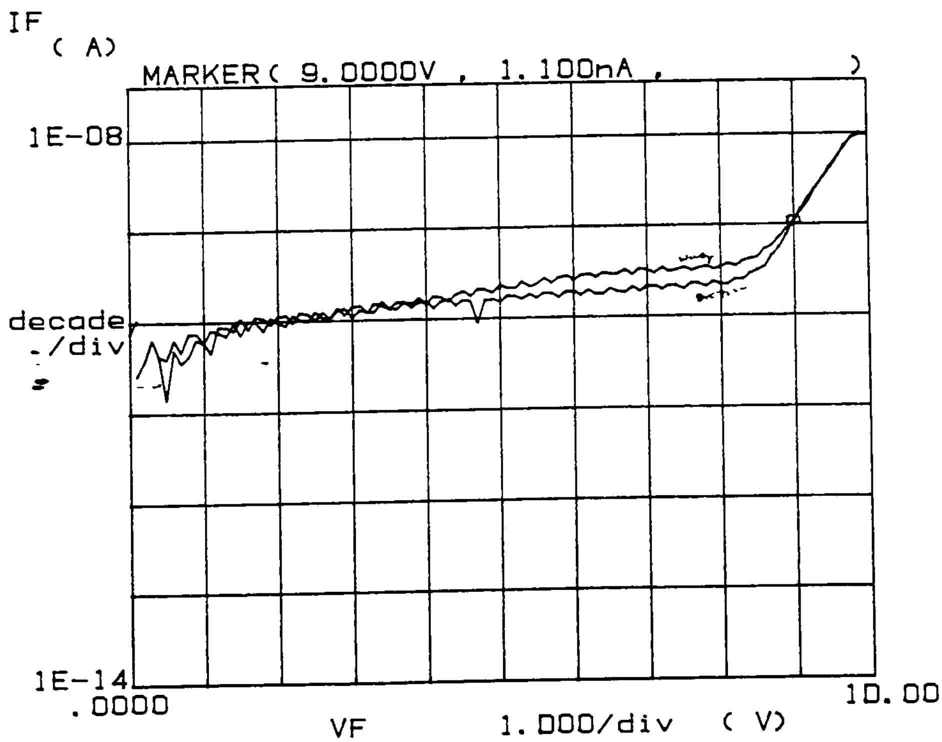


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

H08, 100K, POLY, D/W

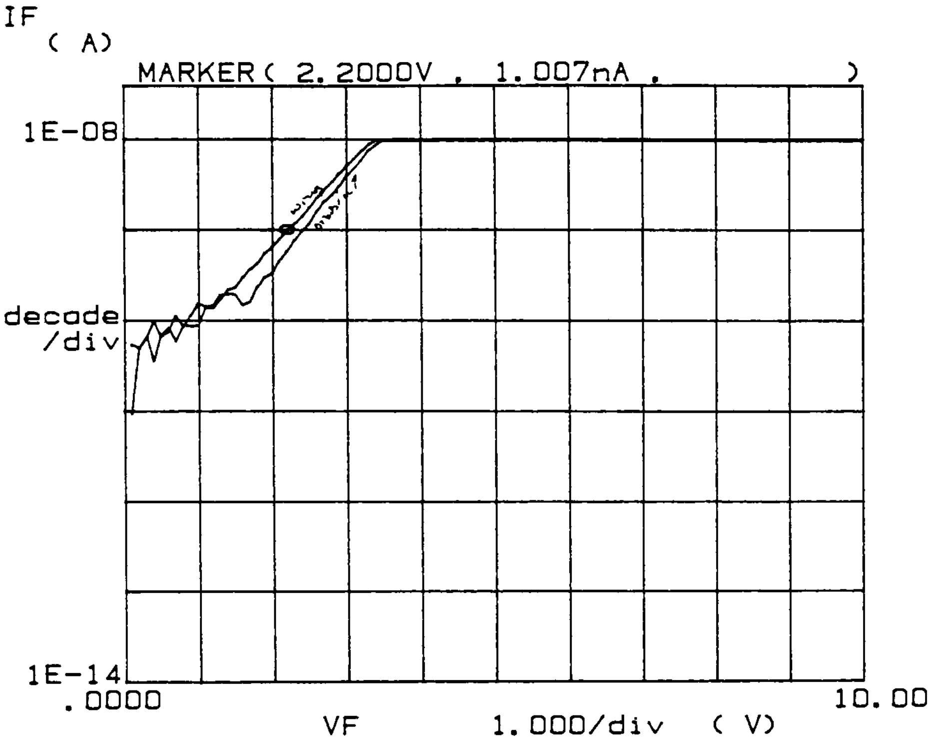


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

HO8, 100K, POLY, D/W

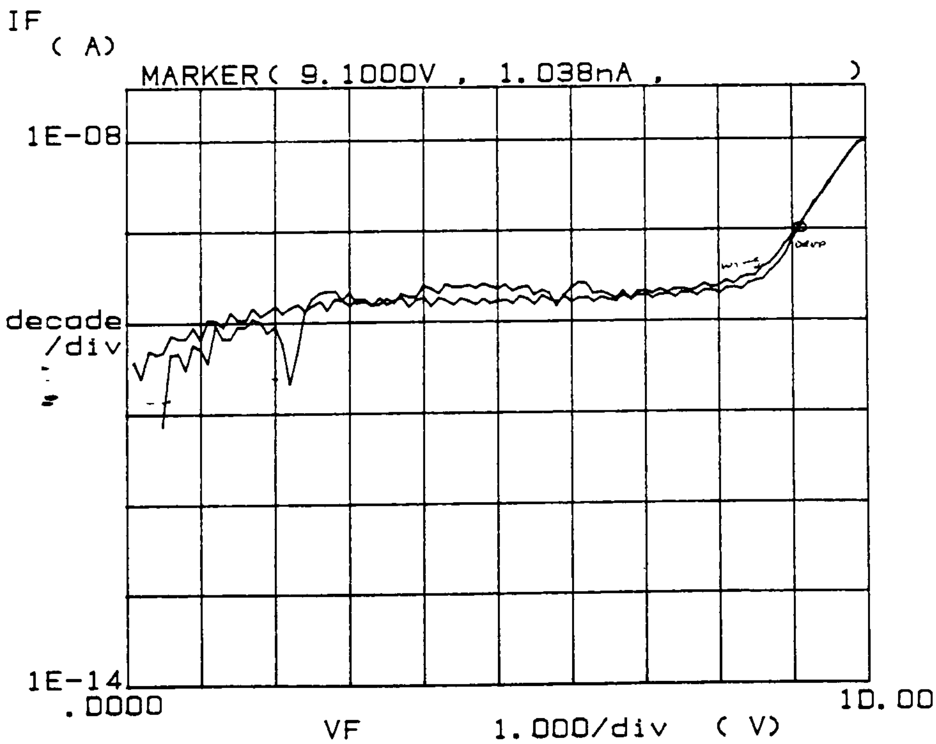


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

HO8, 100K, POLY, D/W

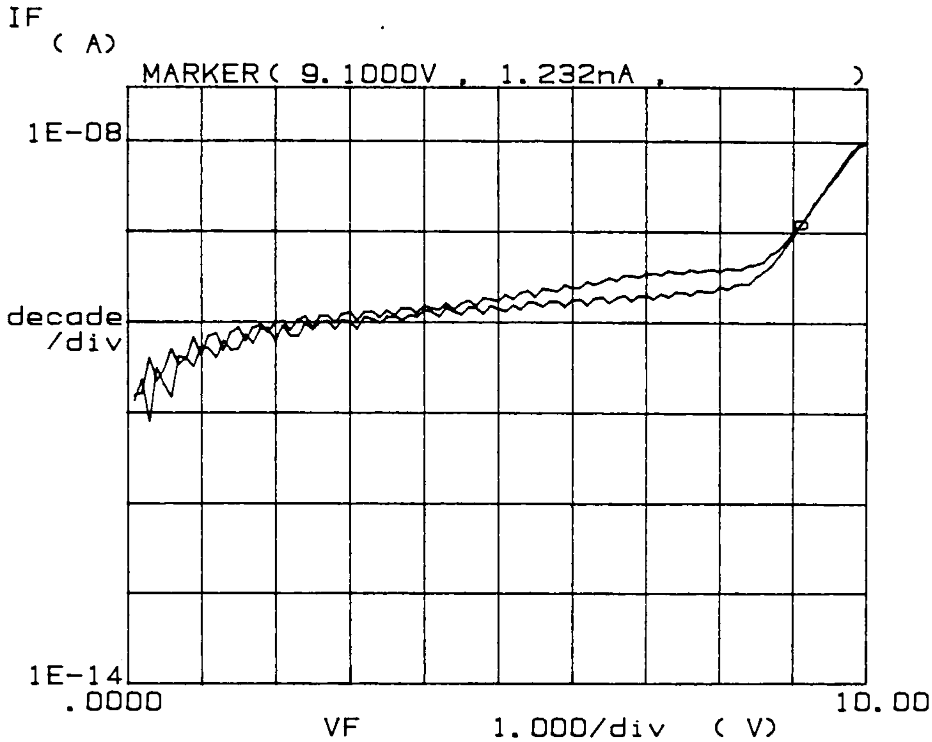


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

HO8, 100K, POLY, D/W

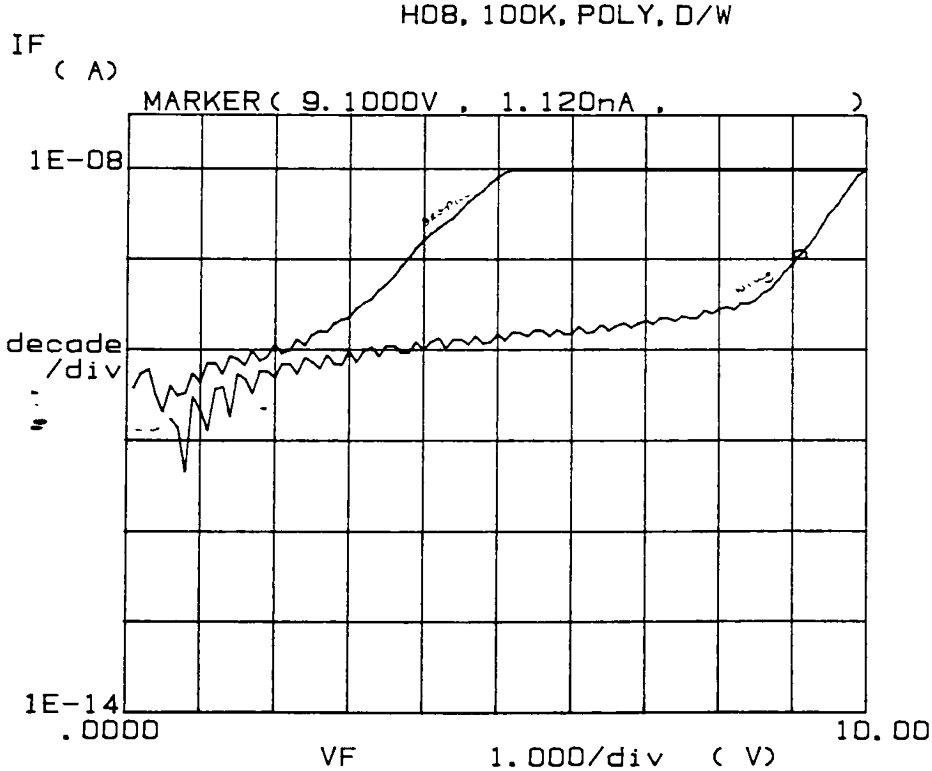


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

HO8, 100K, POLY, D/W

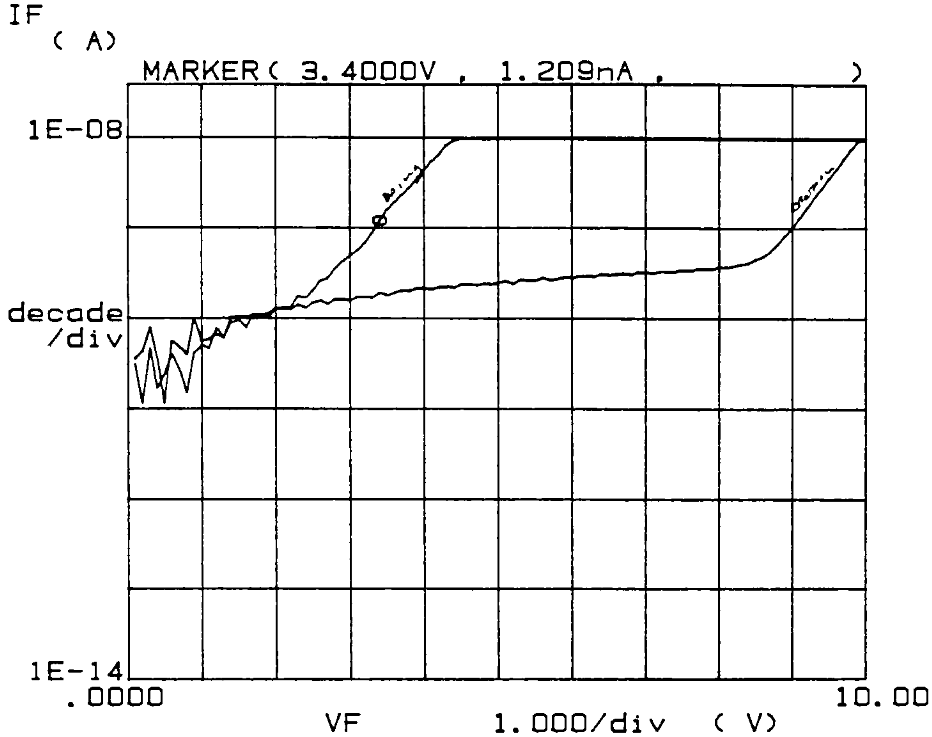


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

H08, 100K, POLY, D/W

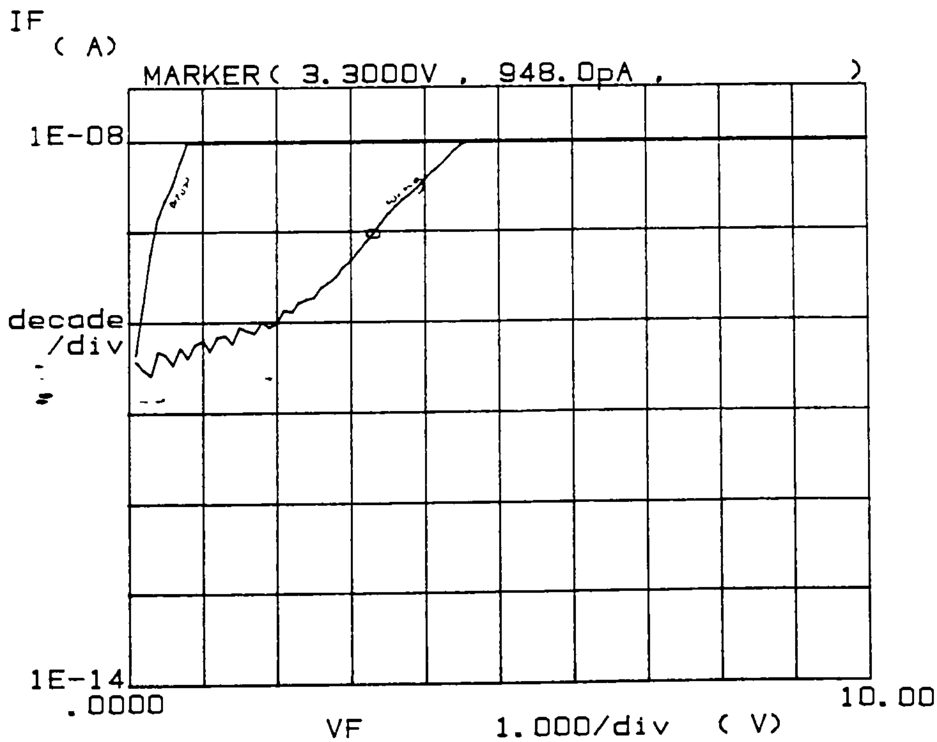


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

H08, 100K, POLY, D/W

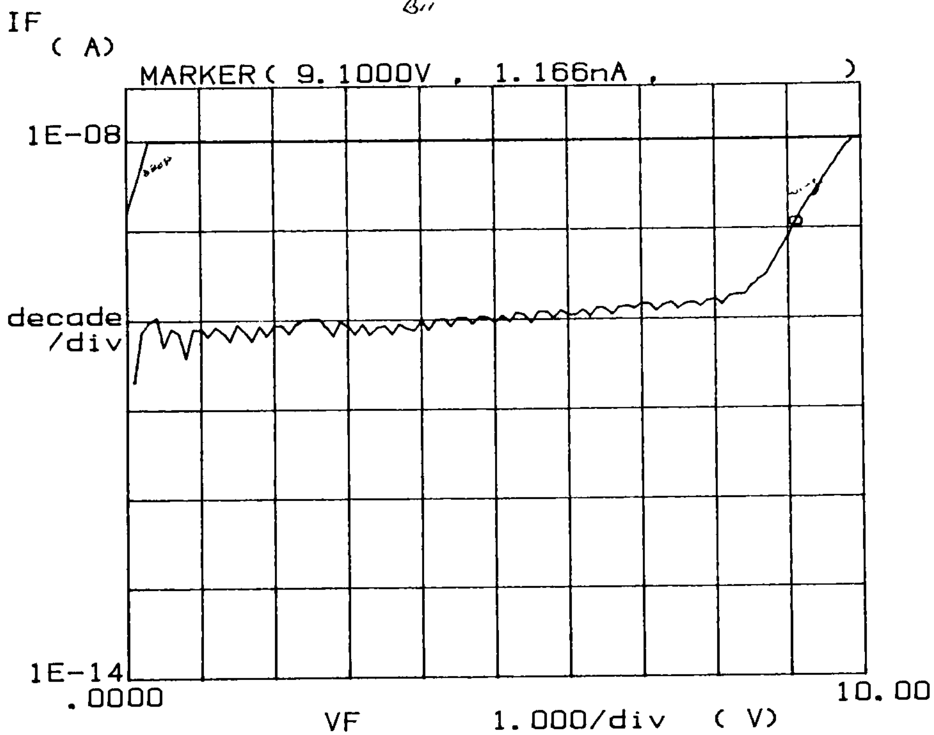


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

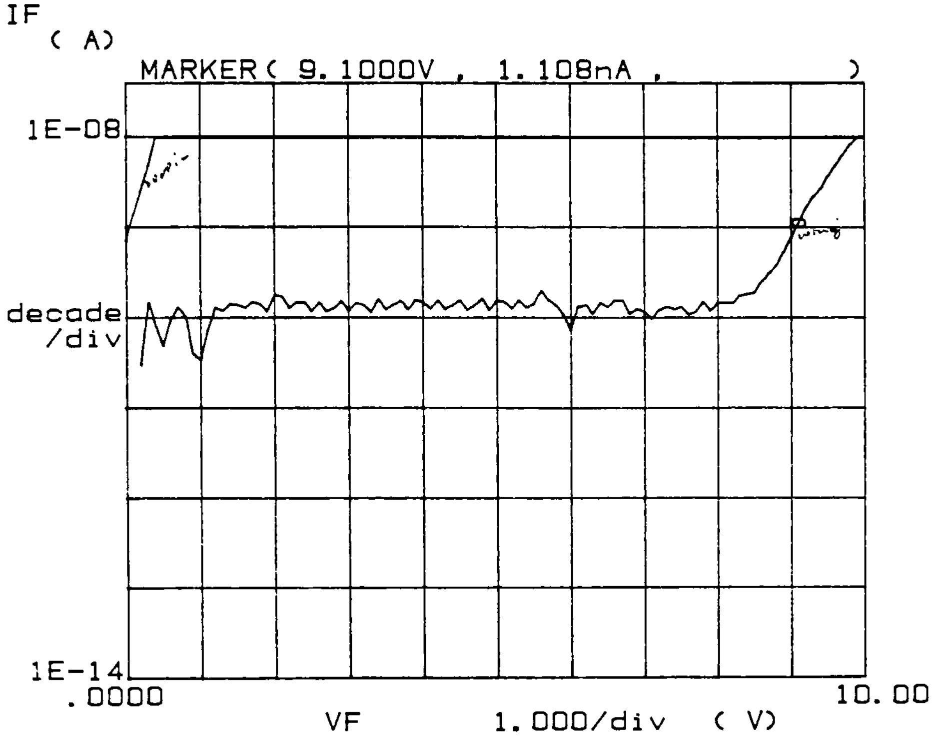
~~H08~~ B11, 100K, POLY, D/W



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

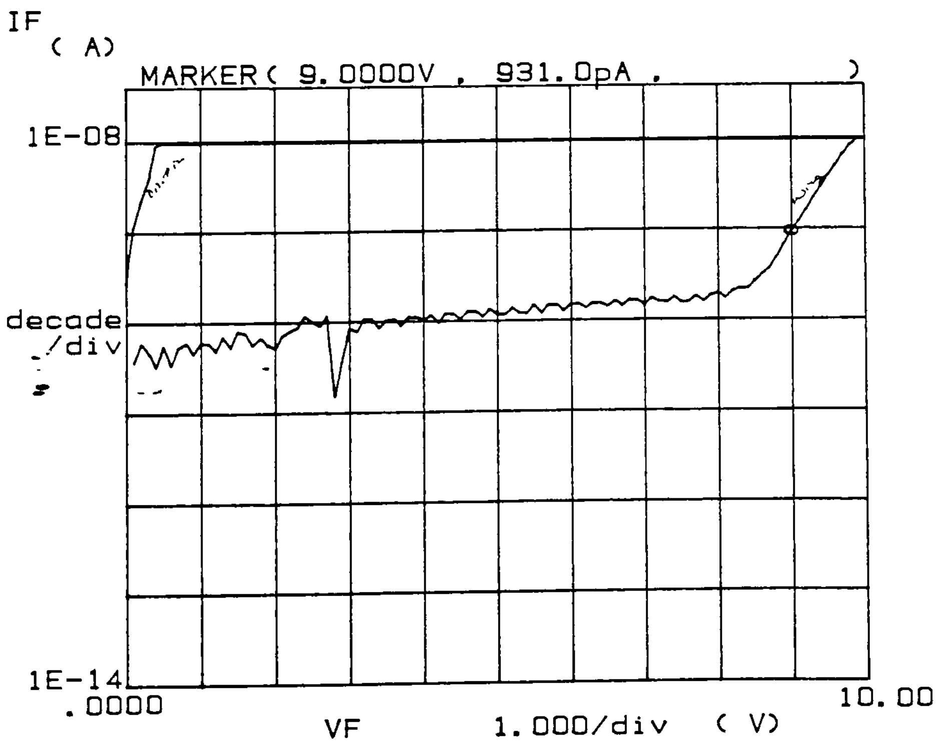
****** GRAPHICS PLOT ******
B11. 100K. POLY. D/W



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

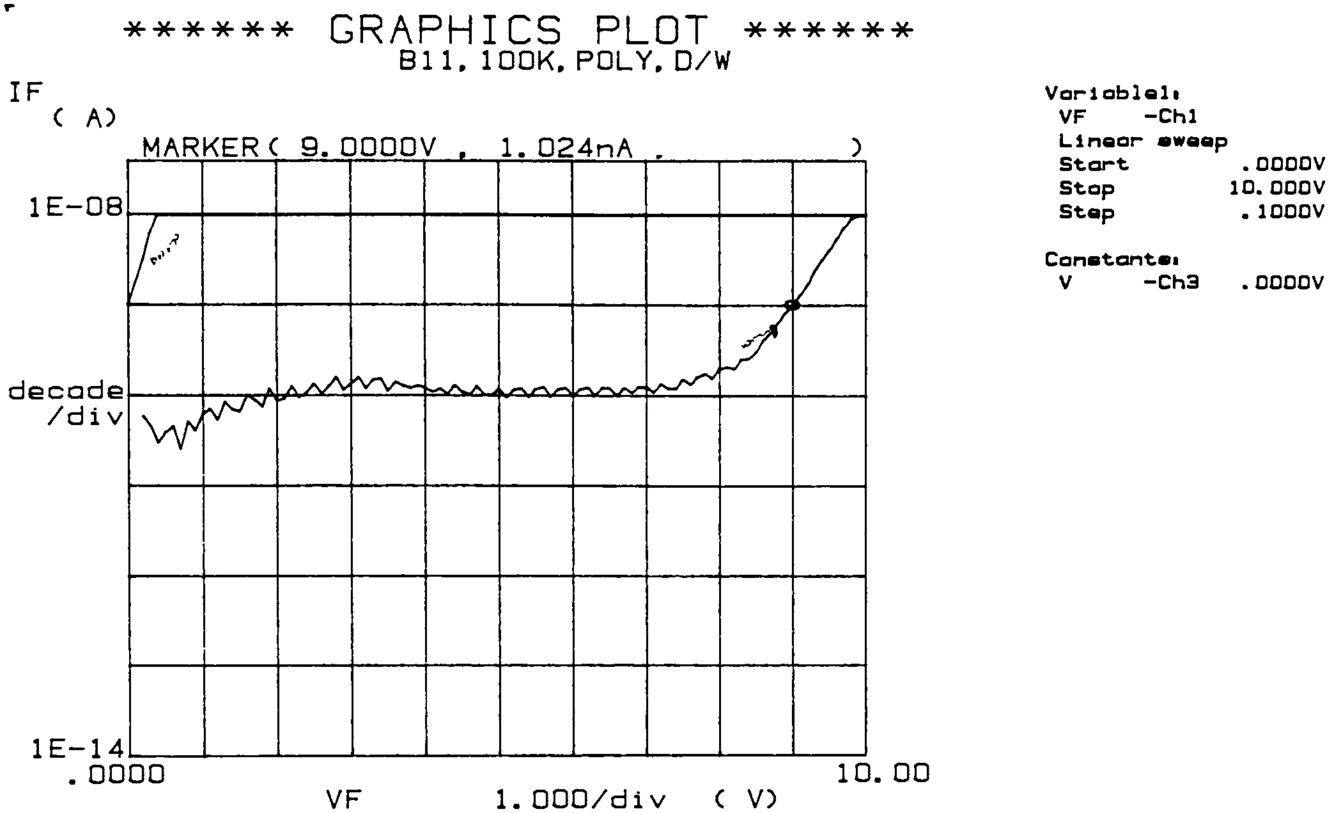
Constants:
V -Ch3 .0000V

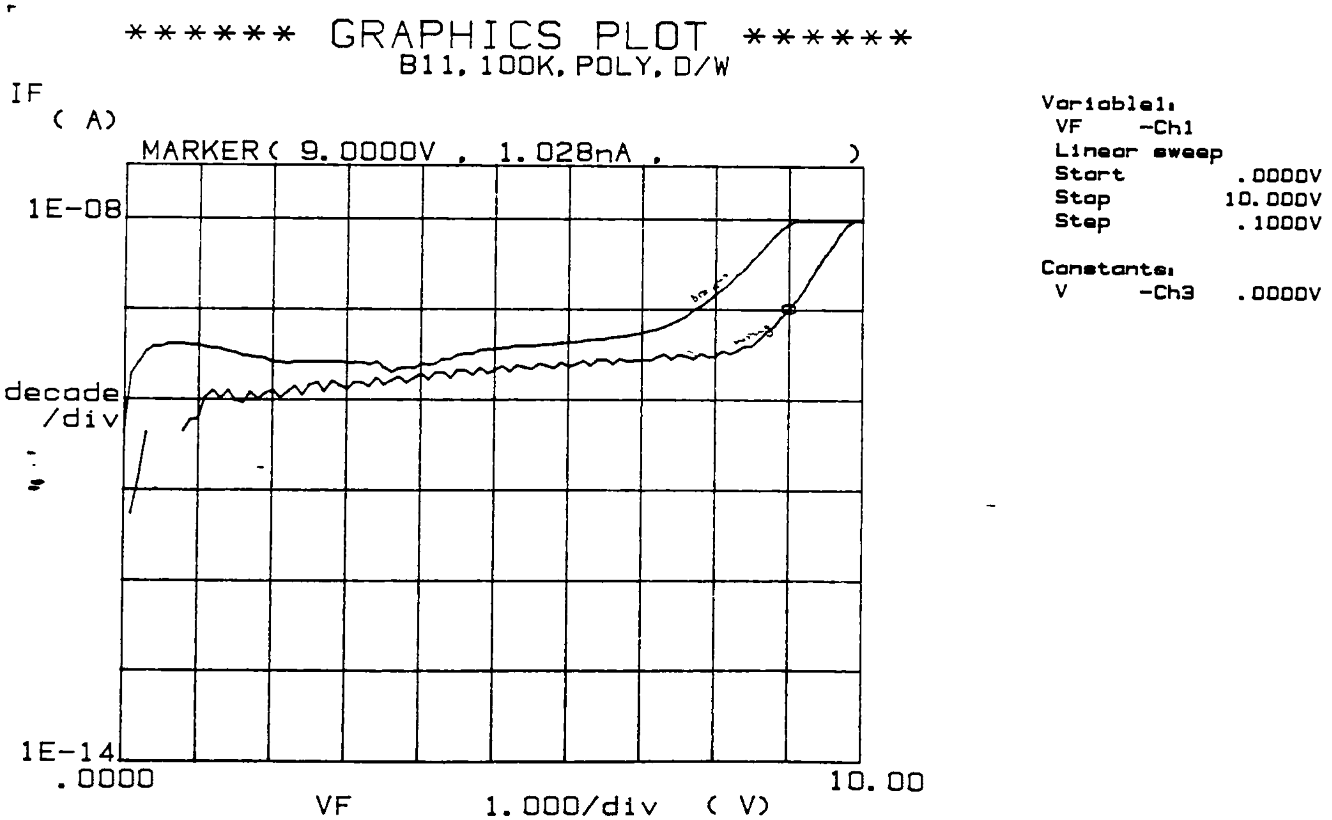
****** GRAPHICS PLOT ******
B11. 100K. POLY. D/W

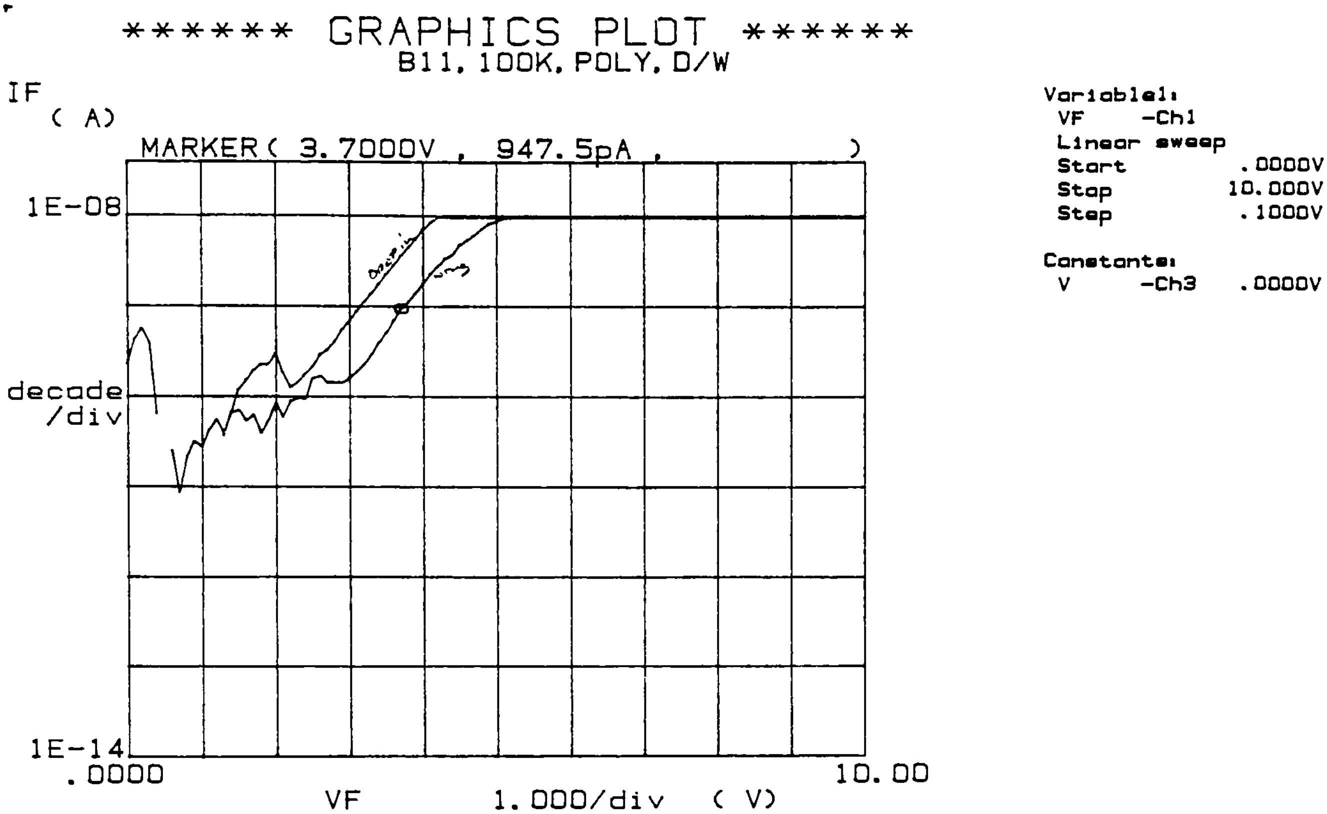


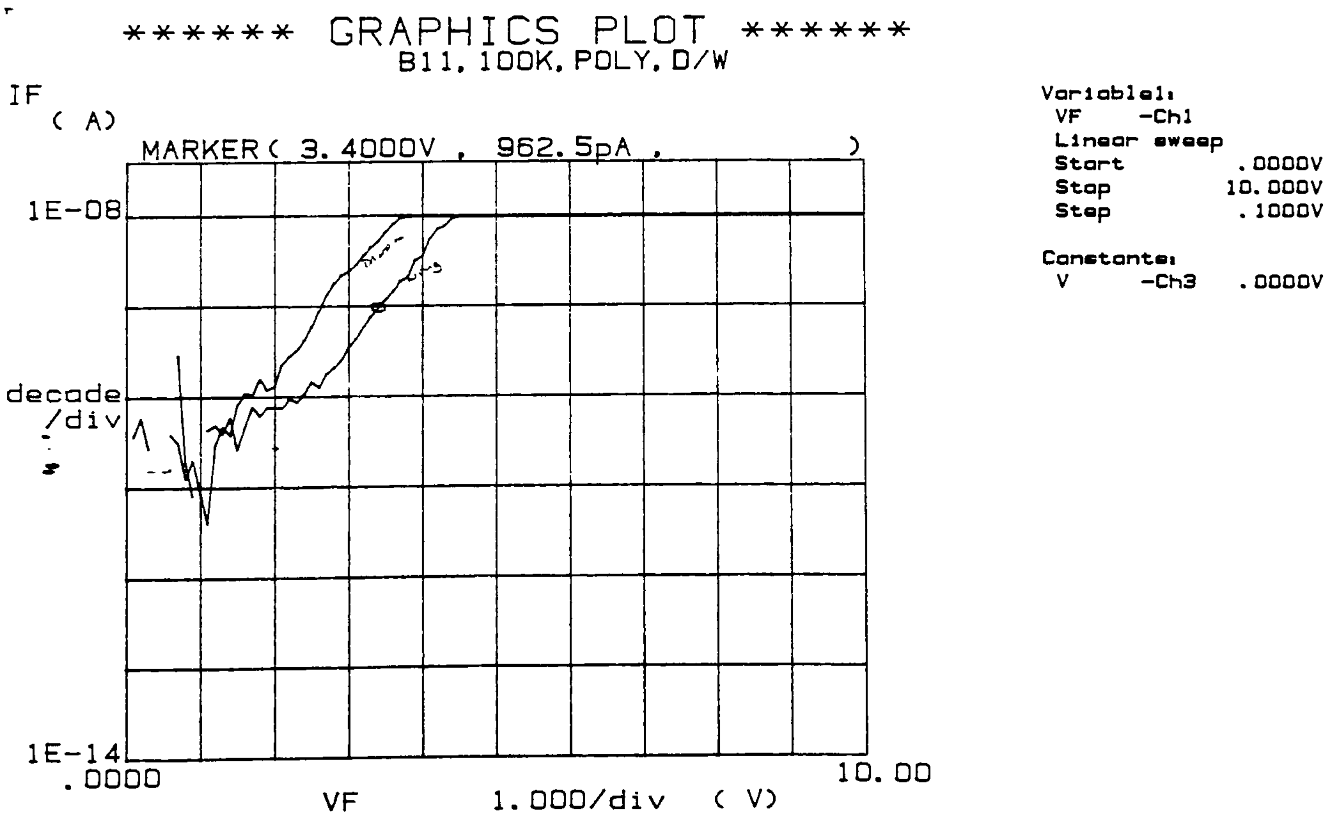
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V


****** GRAPHICS PLOT ******
B11, 100K, POLY, D/W
IF (A)
MARKER (9.0000V , 1.024nA ,)
1E-08
decade /div
1E-14
.0000
10.00
VF 1.000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V
Constants:
V -Ch3 .0000V


****** GRAPHICS PLOT ******
B11, 100K, POLY, D/W
IF (A)
MARKER (9.0000V , 1.028nA ,)
1E-08
decade /div
1E-14
.0000
10.00
VF 1.000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V
Constants:
V -Ch3 .0000V

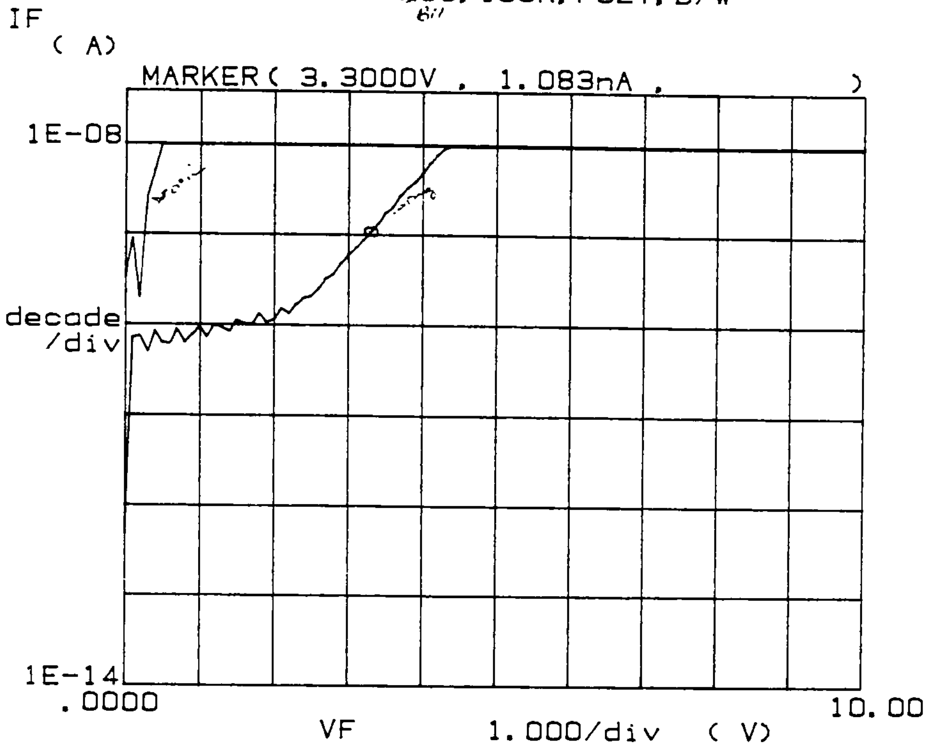

****** GRAPHICS PLOT ******
B11, 100K, POLY, D/W
IF
(A)
MARKER (3.7000V , 947.5pA ,)
1E-08
decade
/div
1E-14
.0000
10.00
VF
1.000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V
Constants:
V -Ch3 .0000V


****** GRAPHICS PLOT ******
B11, 100K, POLY, D/W
IF
(A)
MARKER (3.4000V , 962.5pA ,)
1E-08
decade
/div
1E-14
.0000
10.00
VF
1.000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V
Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

~~H08~~, 100K, POLY, D/W

B11



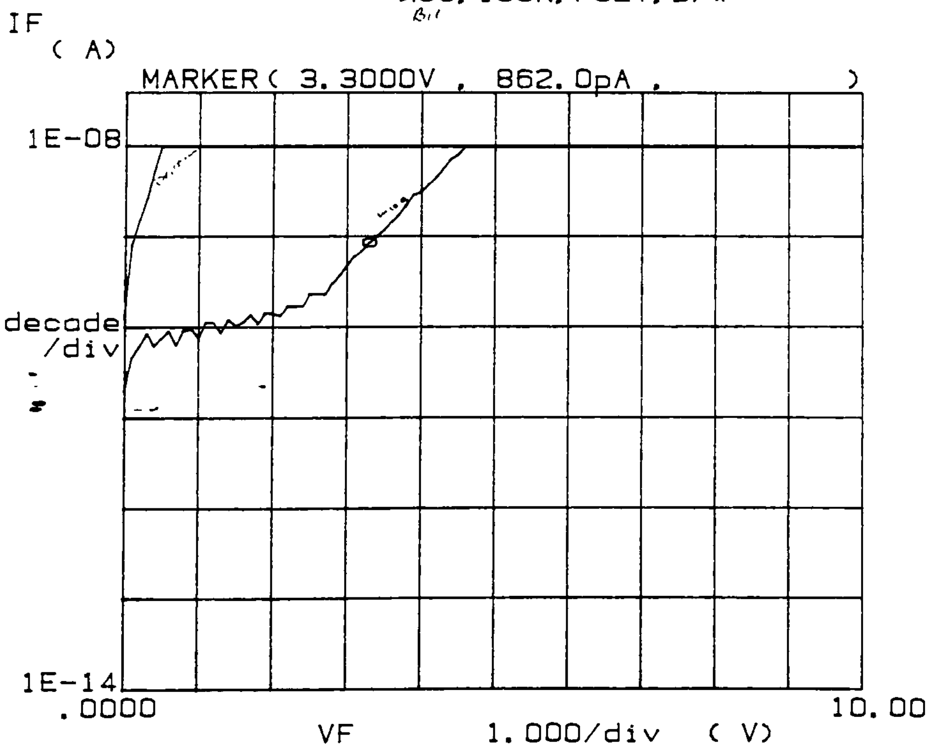
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

~~H08~~, 100K, POLY, D/W

B11

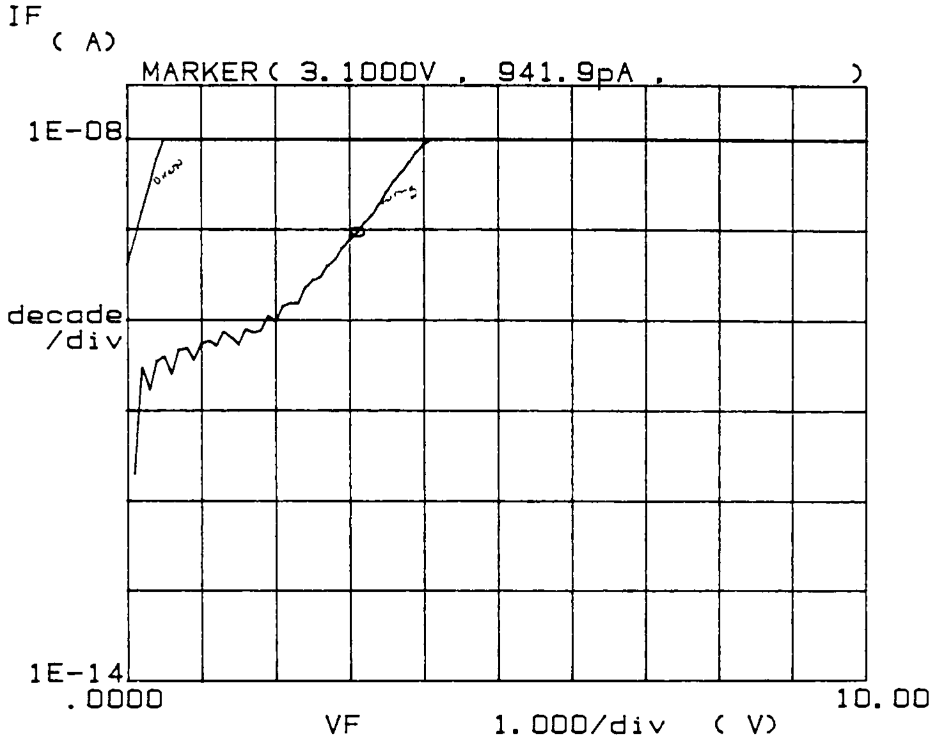


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B11, 100K, POLY, D/W

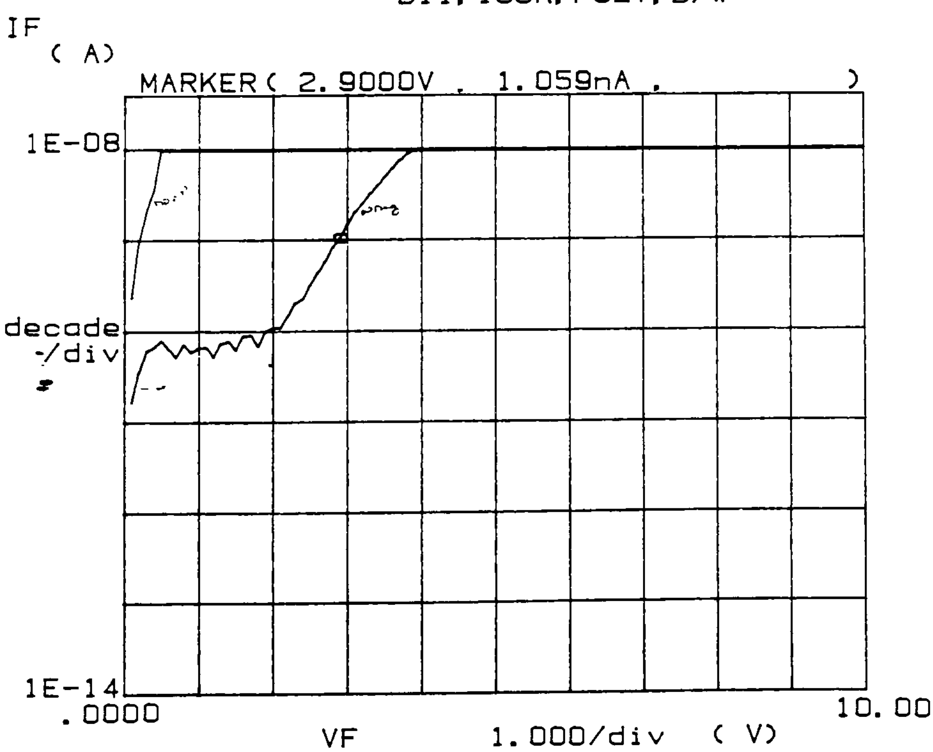


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

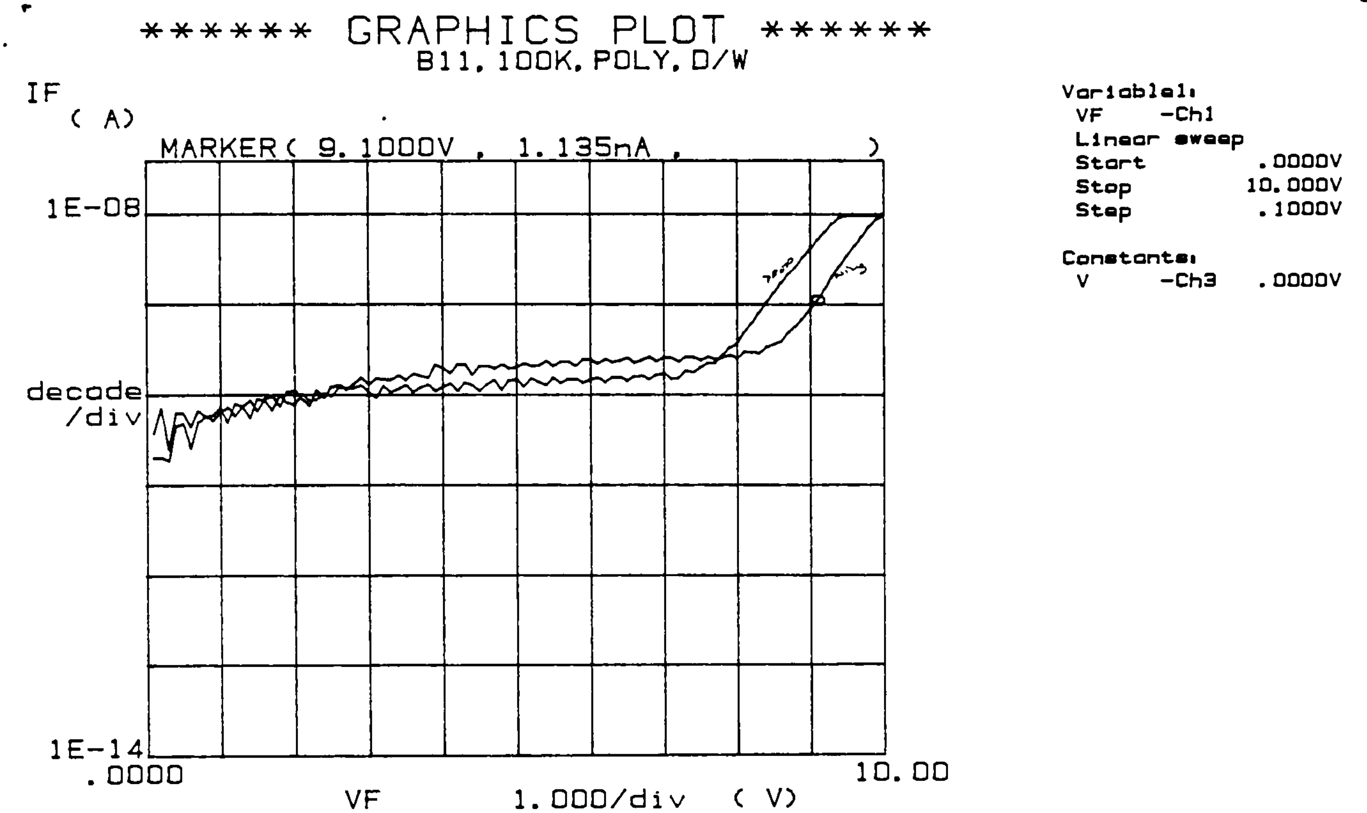
****** GRAPHICS PLOT ******

B11, 100K, POLY, D/W



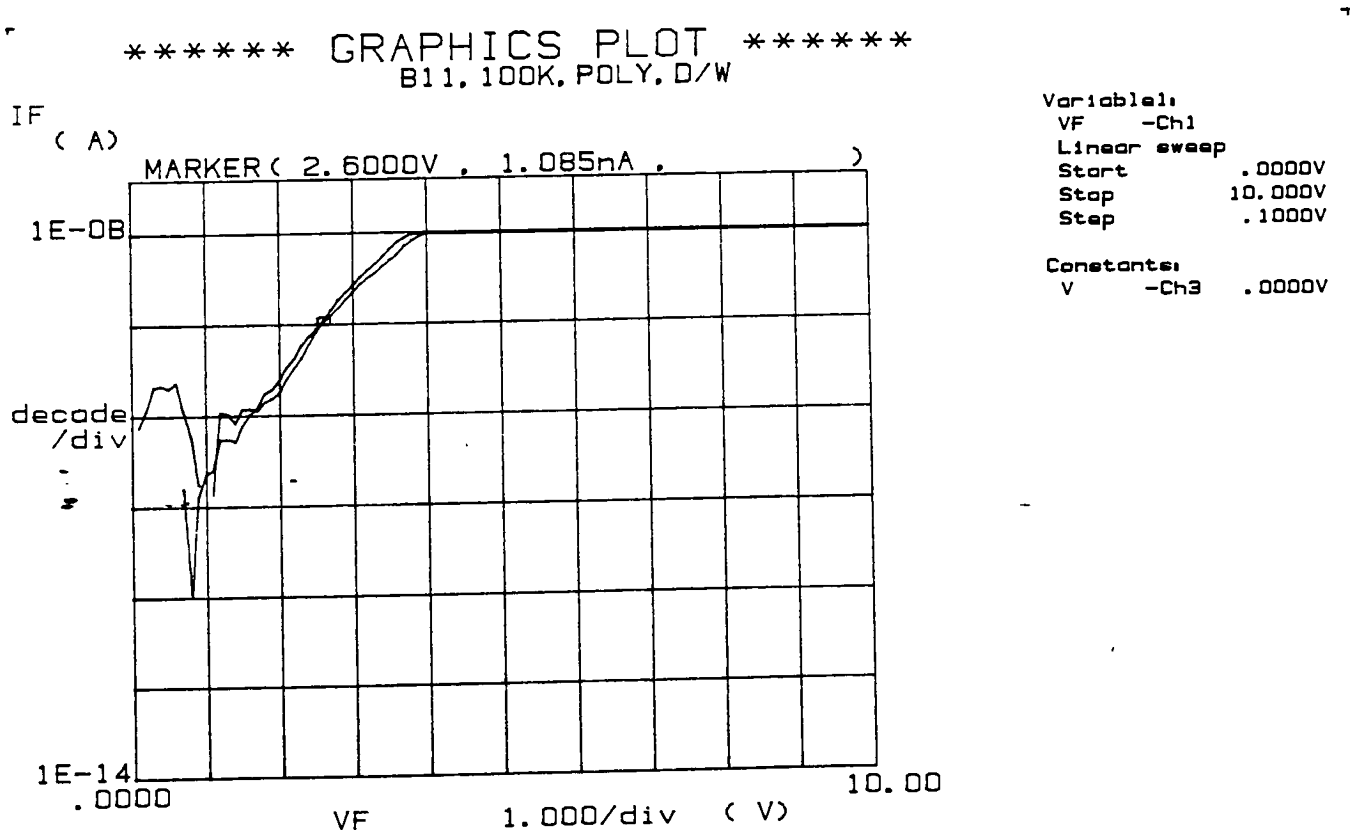
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V



A= 10^{-3} cm^2, NO I^2

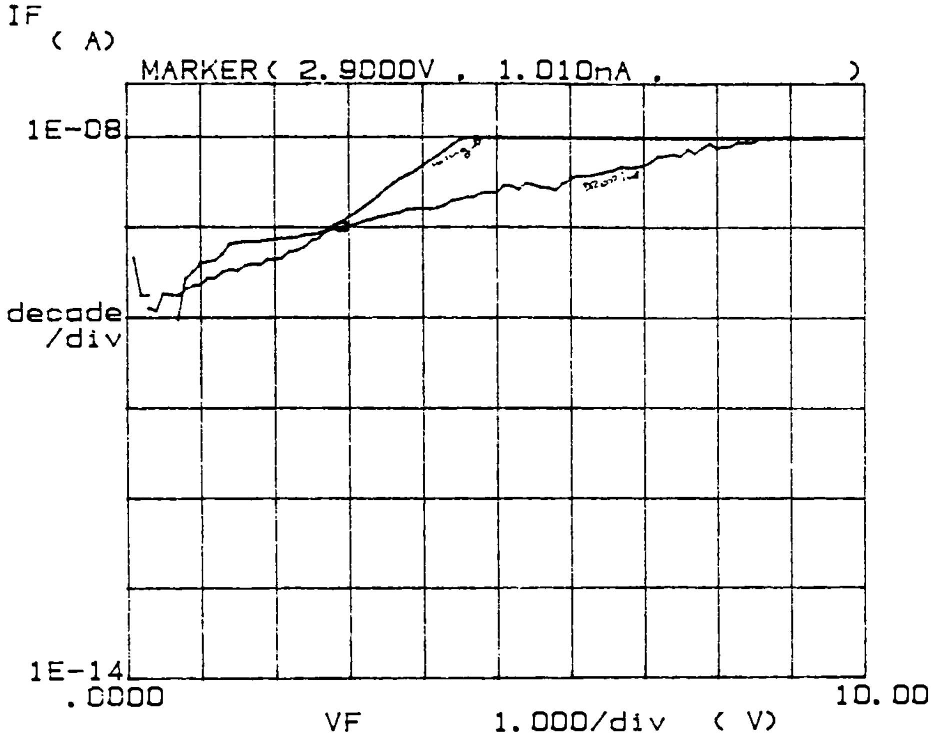
BOE ETCH BACK=4500 A



5500 Å Etch Back Results

****** GRAPHICS PLOT ******

C01, 100K, POLY, D/W

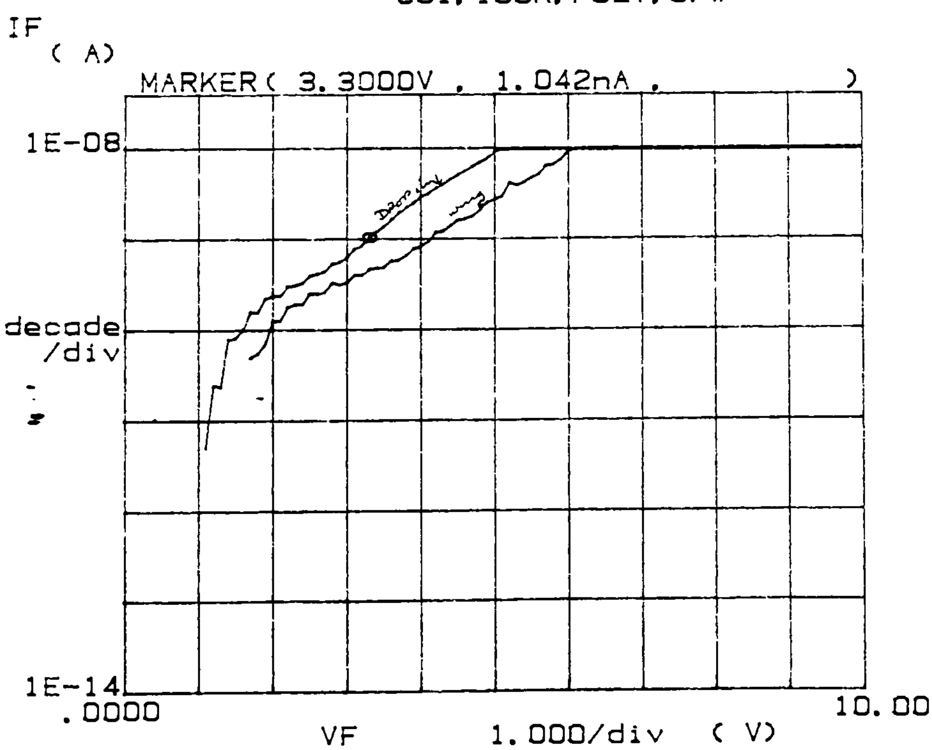


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

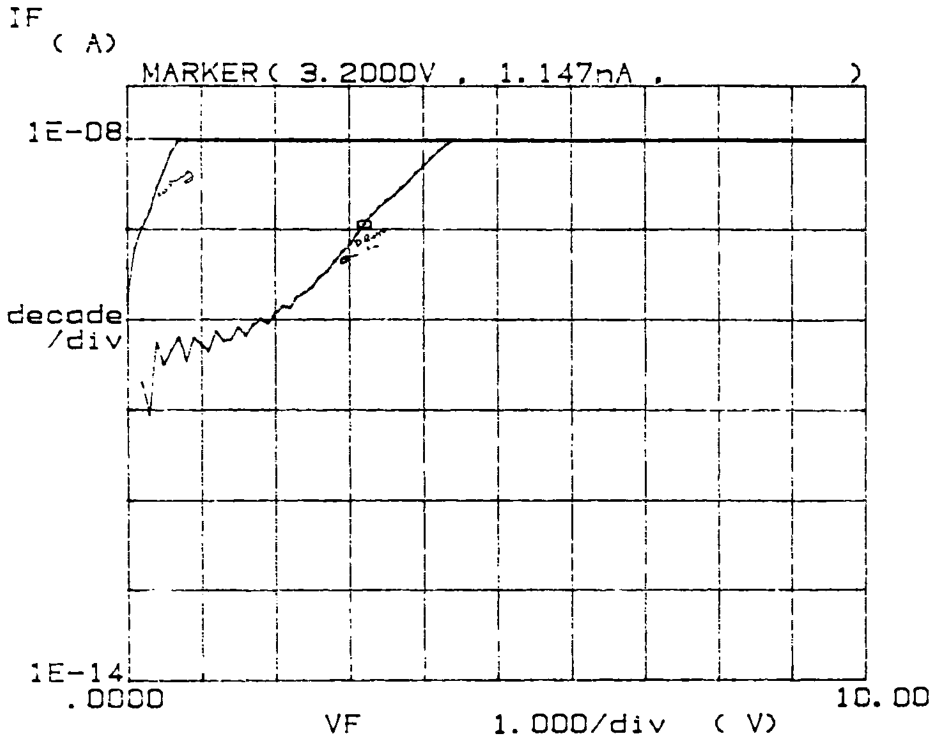
C01, 100K, POLY, D/W



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

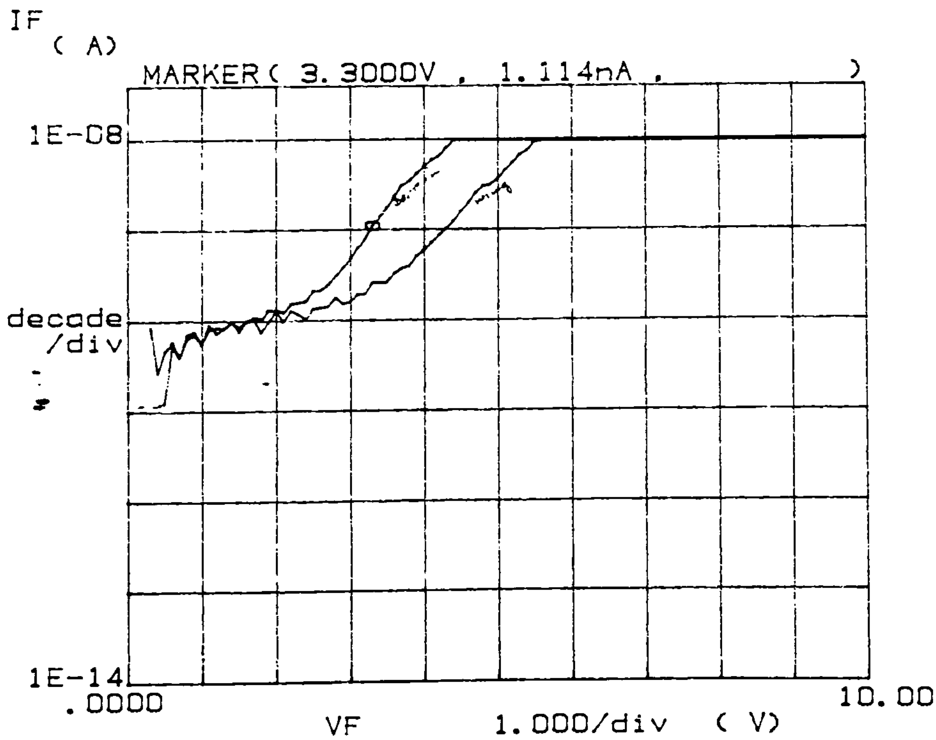
****** GRAPHICS PLOT ******
CD1, 100K, POLY, D/W



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******
CD1, 100K, POLY, D/W

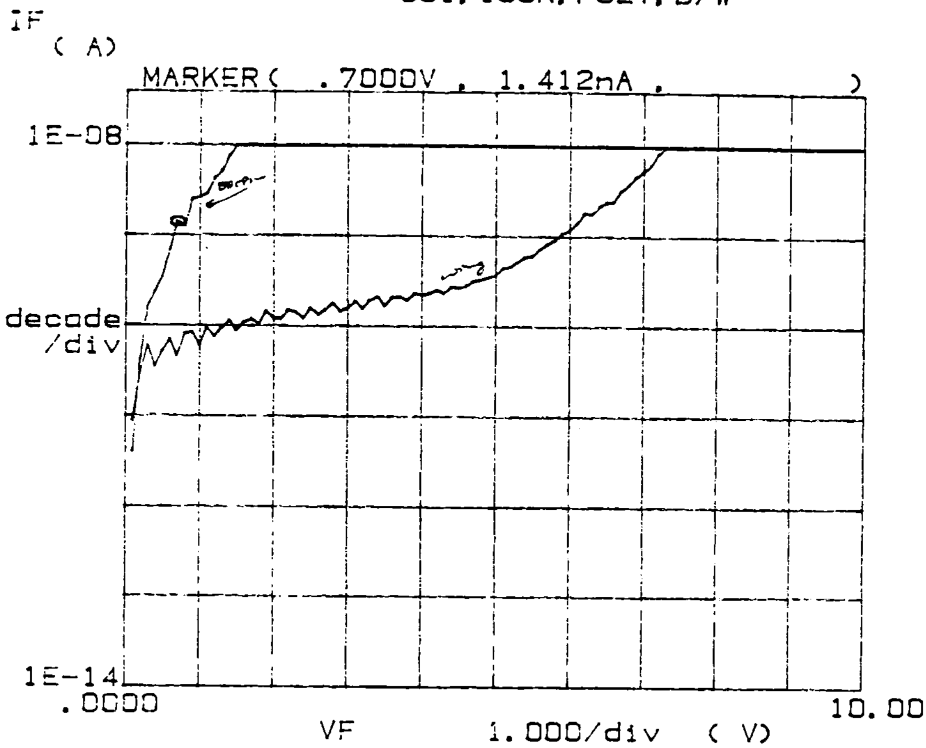


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

C01, 100K, POLY, D/W

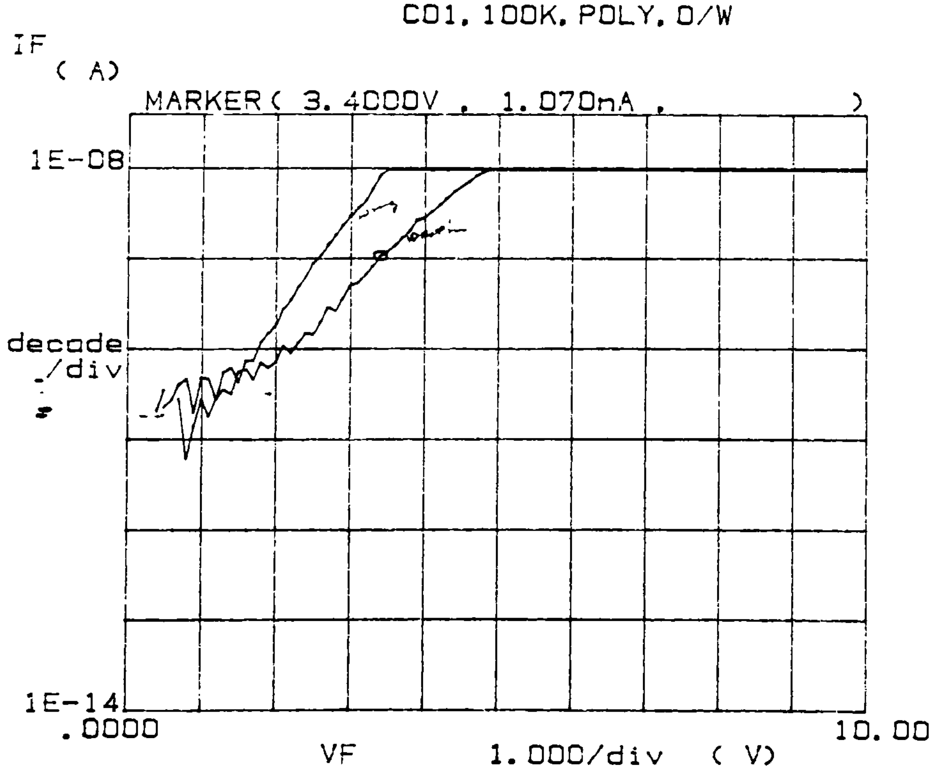


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

C01, 100K, POLY, D/W

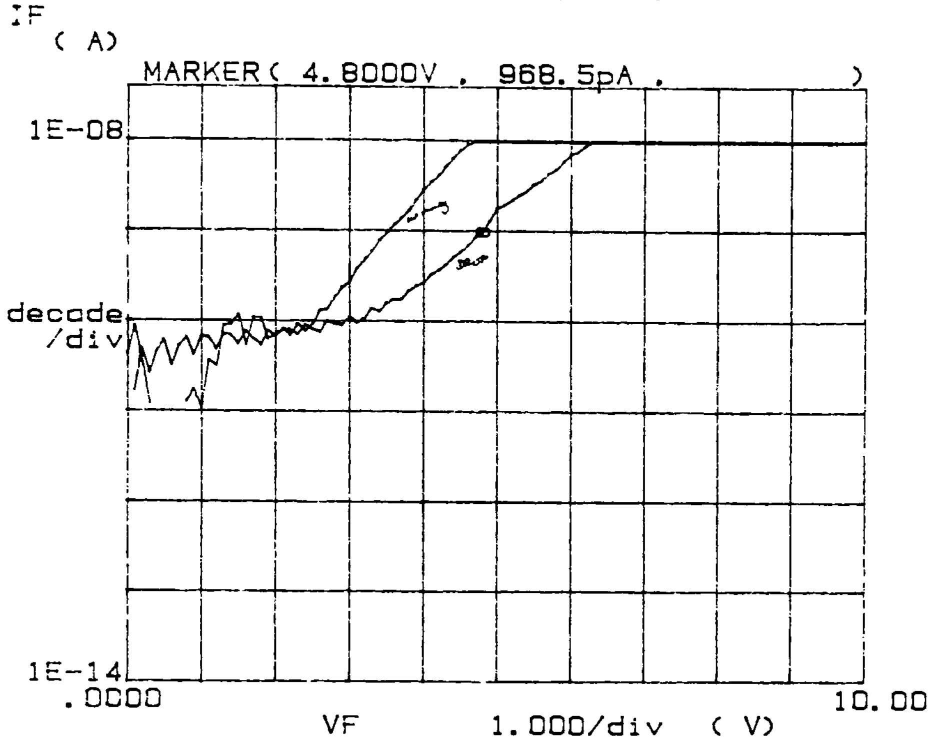


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

C01. 100K. POLY. D/W

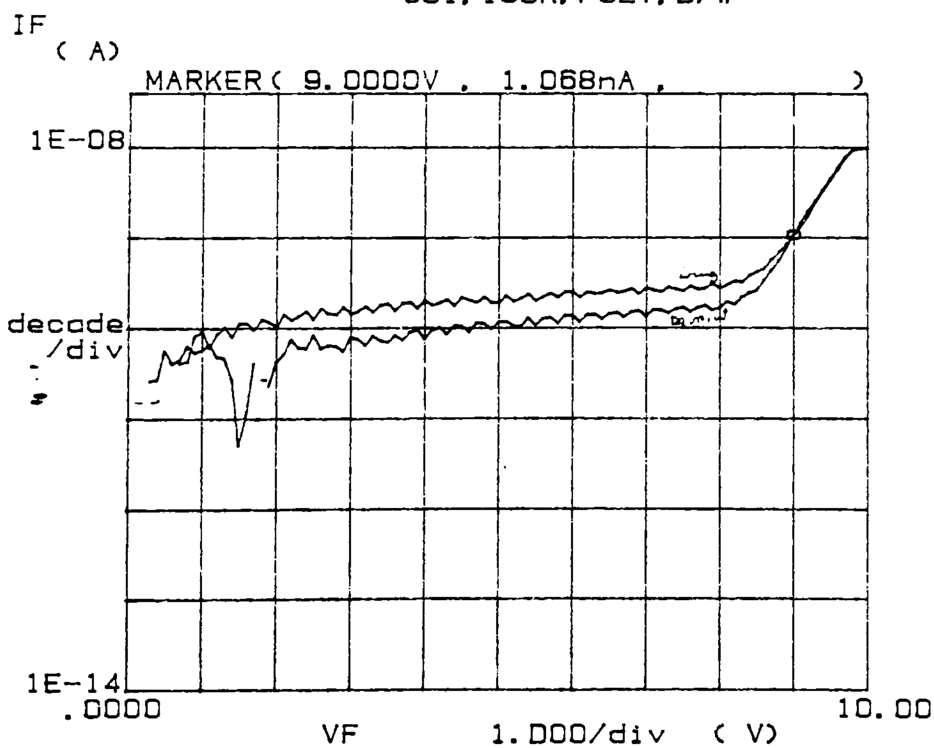


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

C01. 100K. POLY. D/W

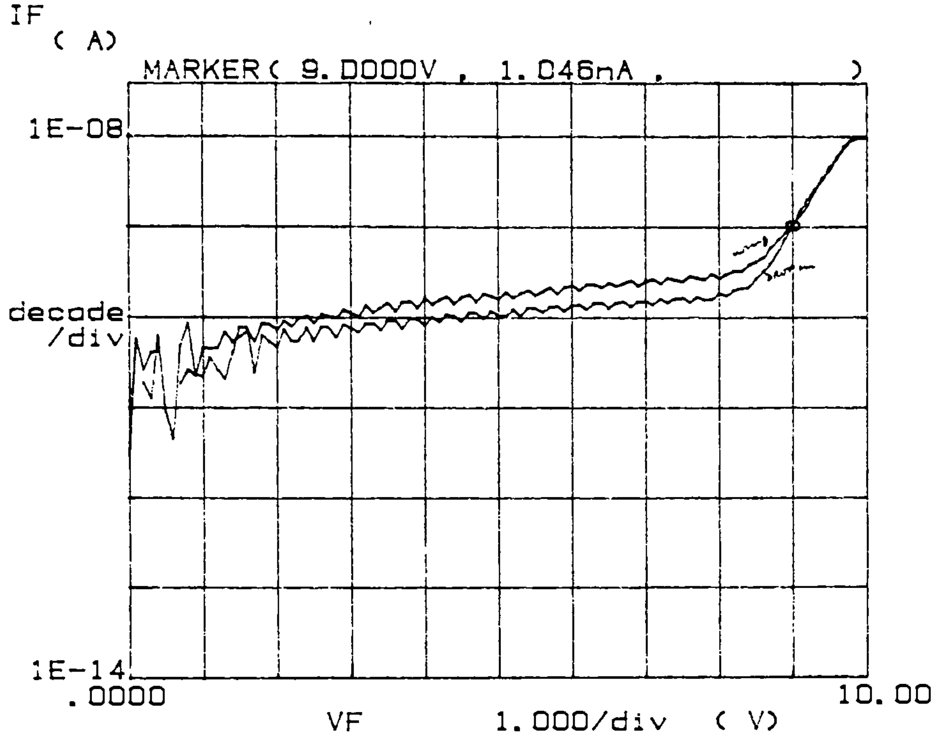


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

C01, 100K, POLY, D/W

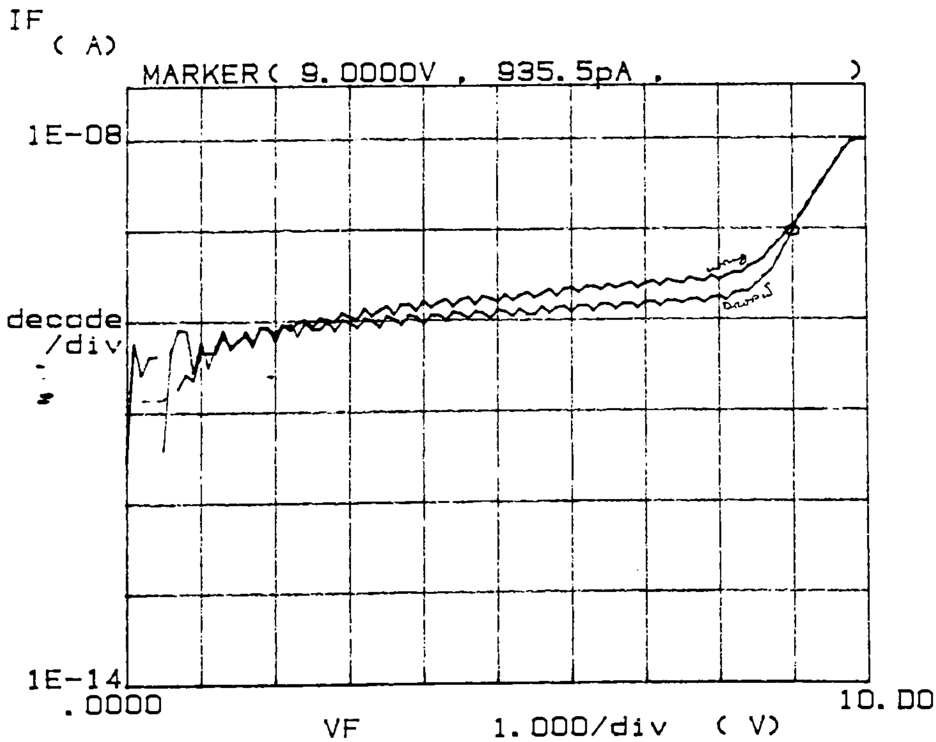


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

C01, 100K, POLY, D/W

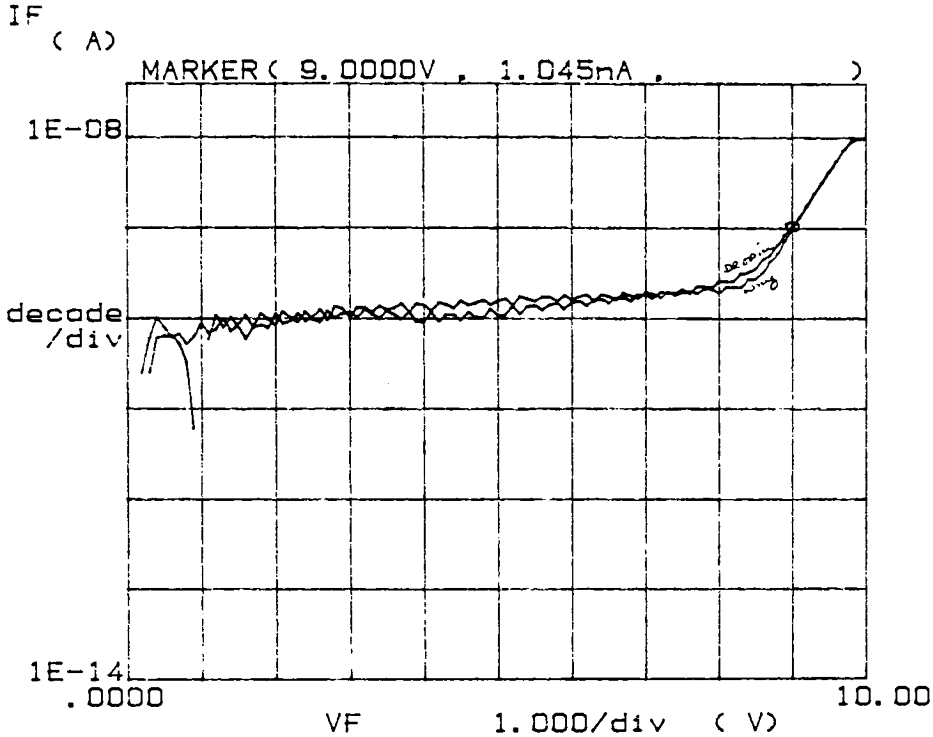


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

C01. 100K. POLY. D/W

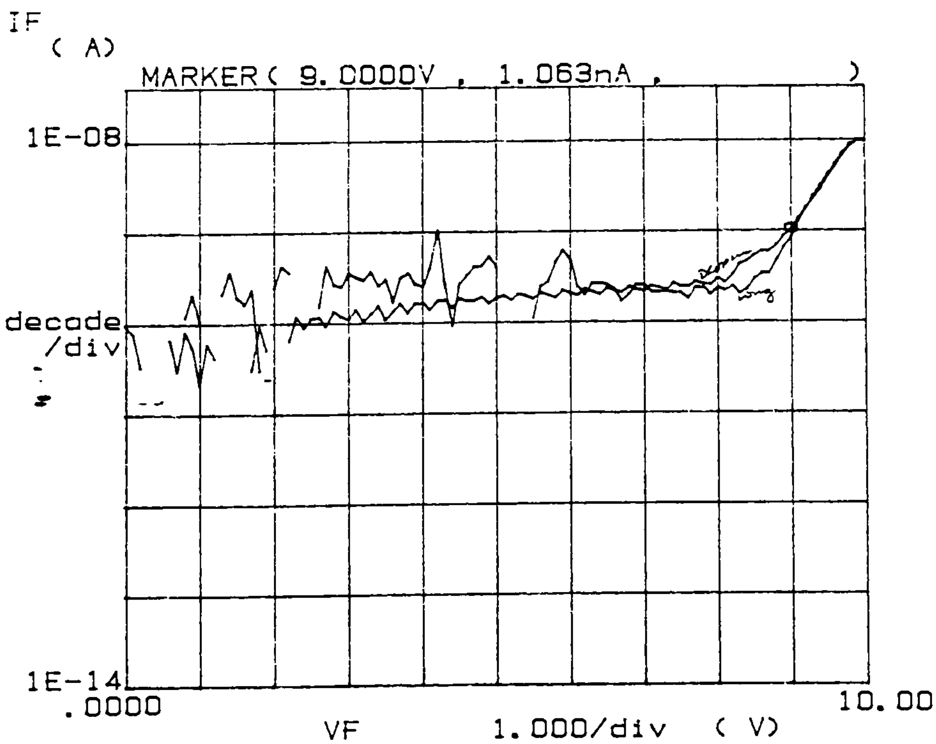


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10. 000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

C01. 100K. POLY. D/W

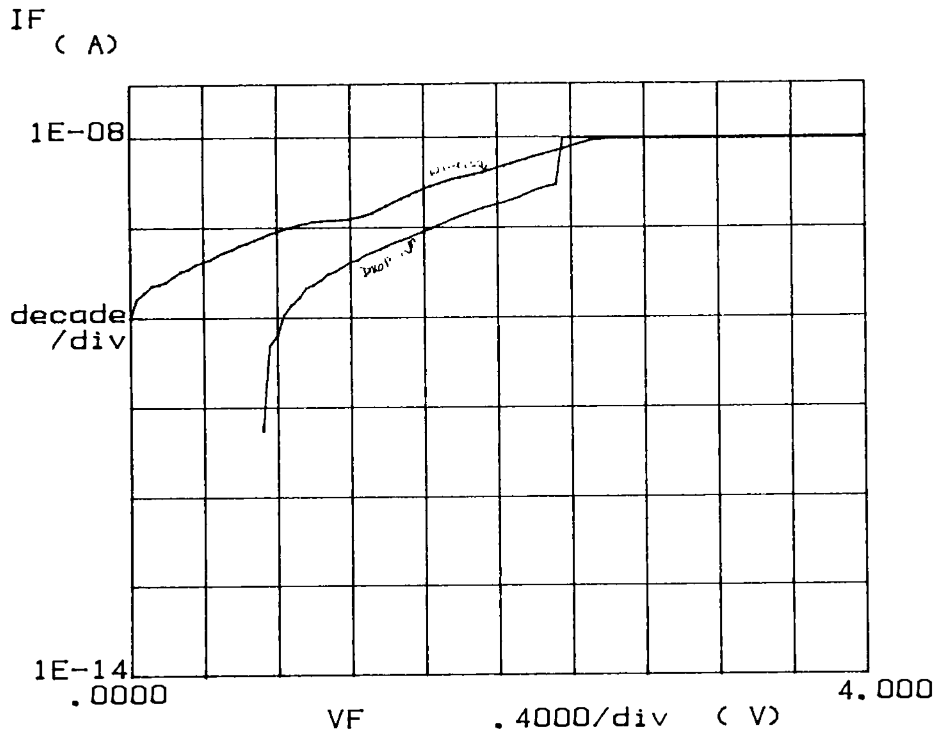


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10. 000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

C02, 100K, AL, D, W

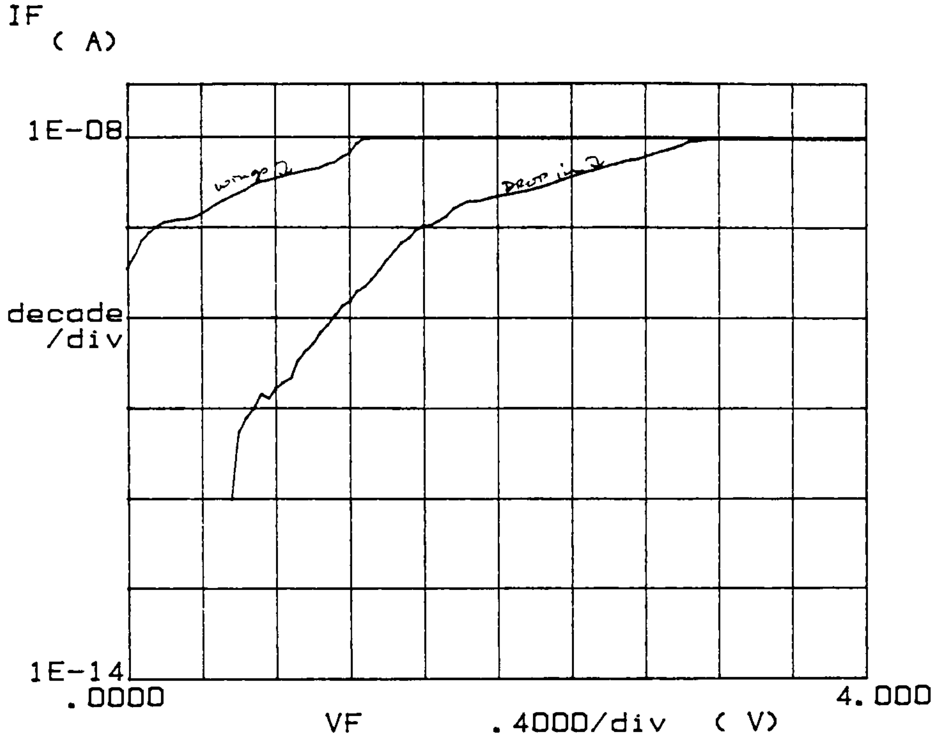


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

CD2, 100K, AL, D, W

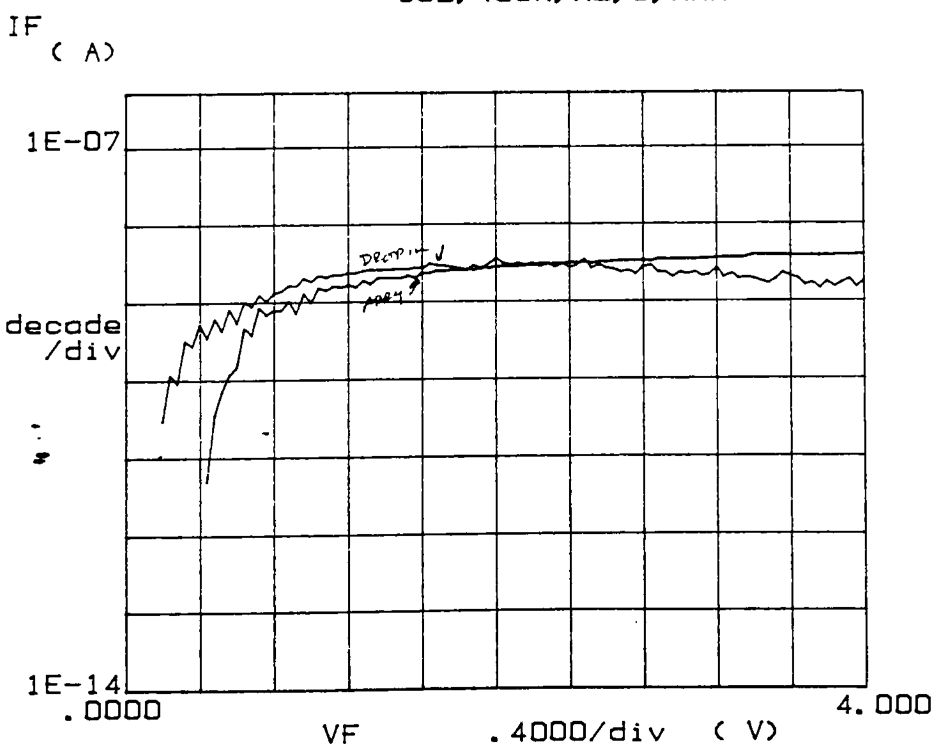


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

CD2, 400K, AL, D, ARRY

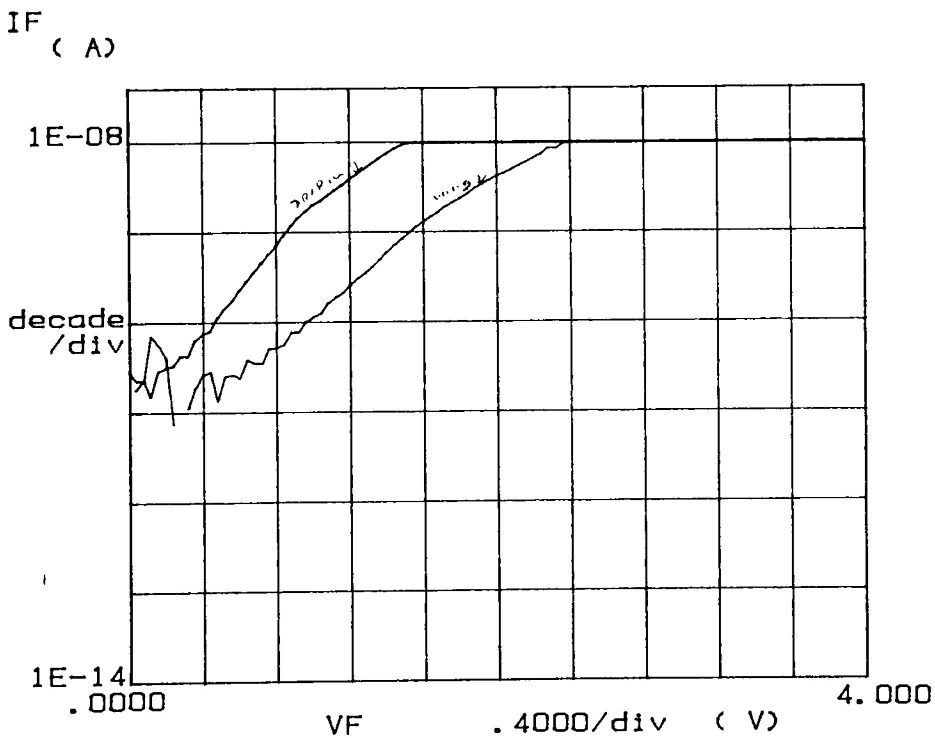


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B17, 100K, AL, D/W

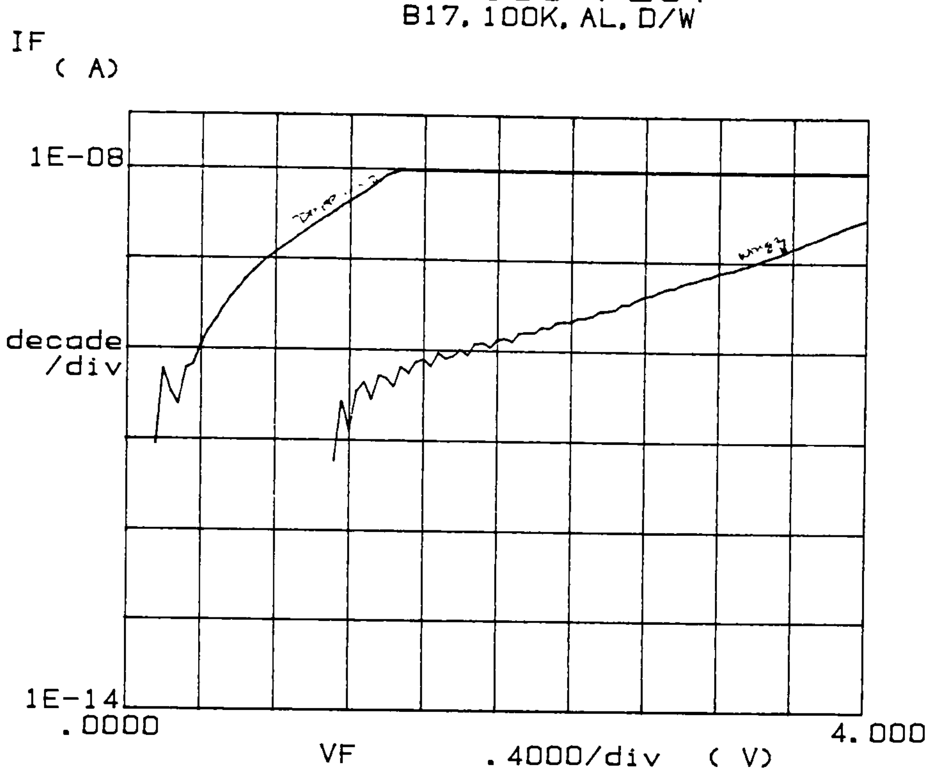


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B17, 100K, AL, D/W

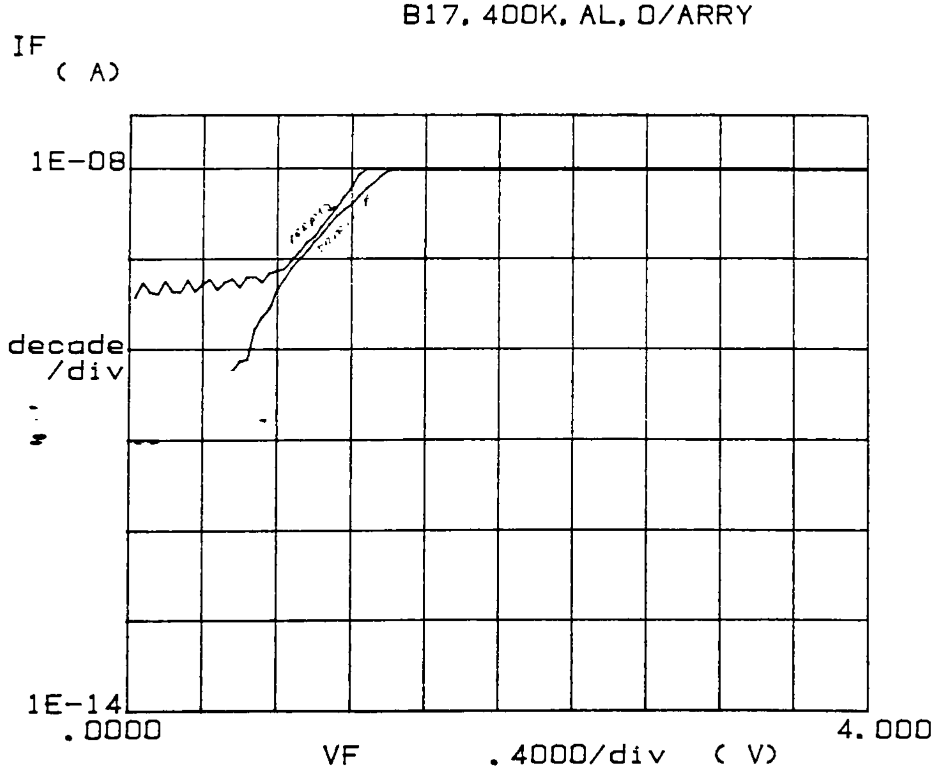


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B17, 400K, AL, D/ARRY

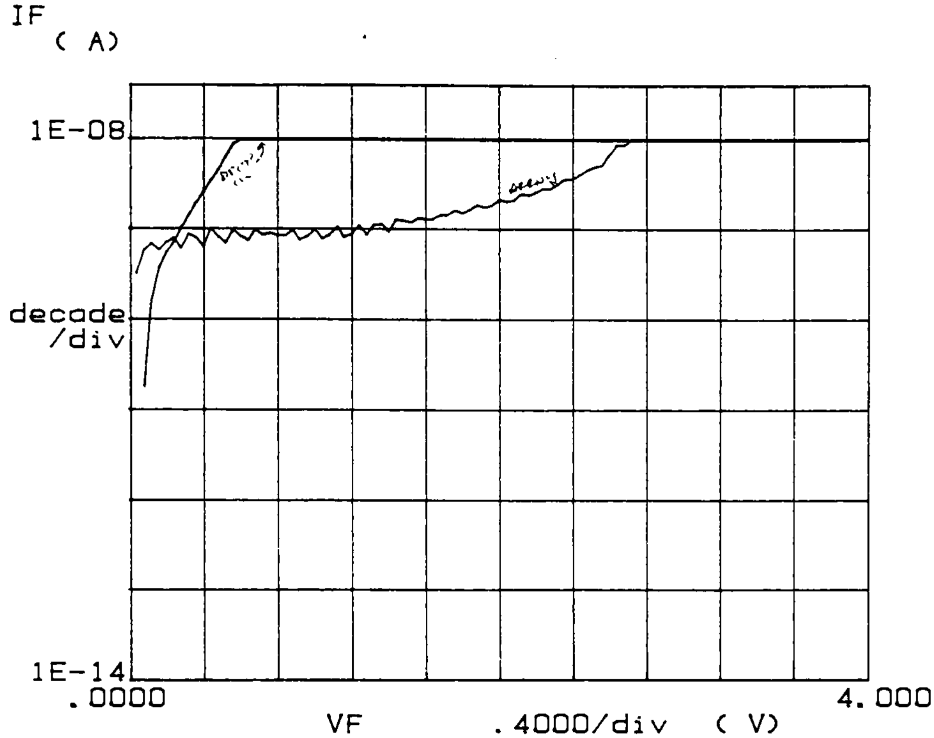


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B17, 400K, AL, D/ARRY

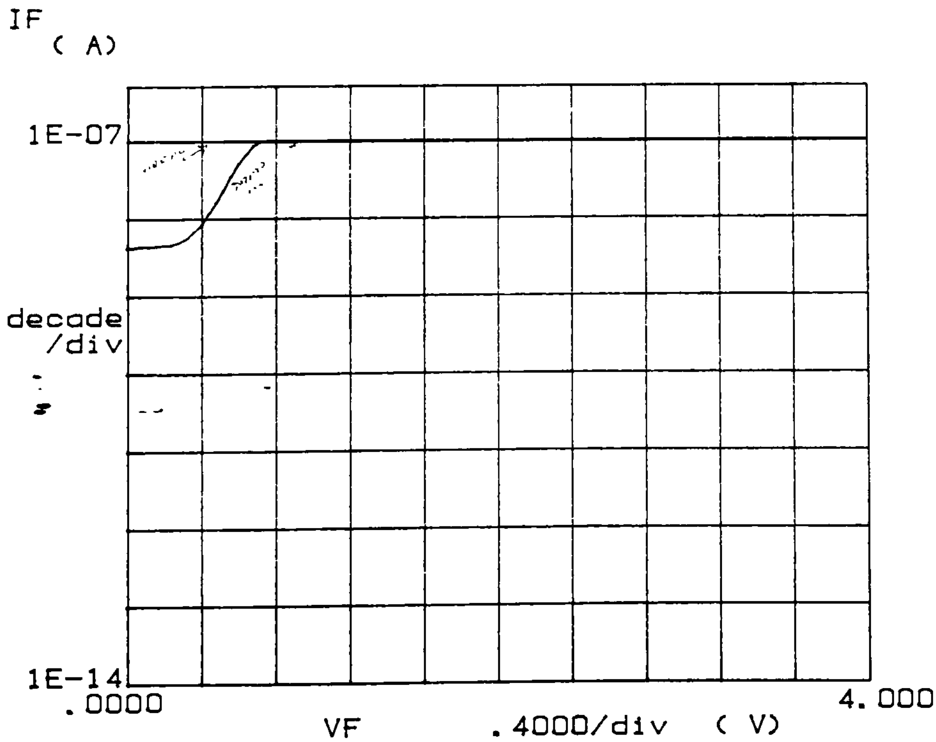


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B17, 1MEG, AL, D/ARRY

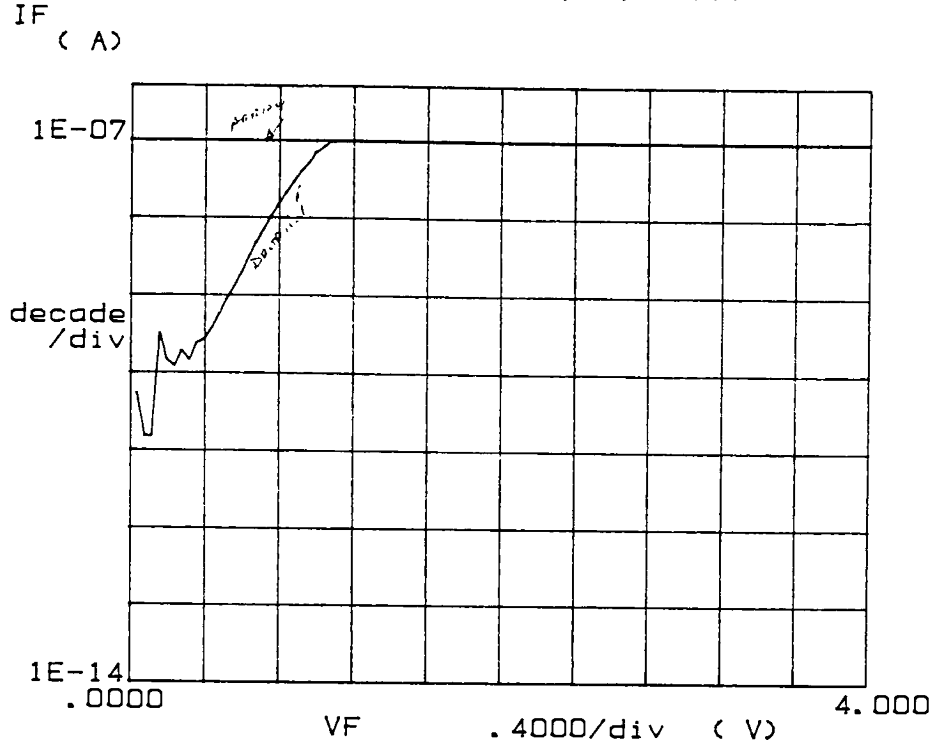


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B17, 1MEG, AL, D/ARRY



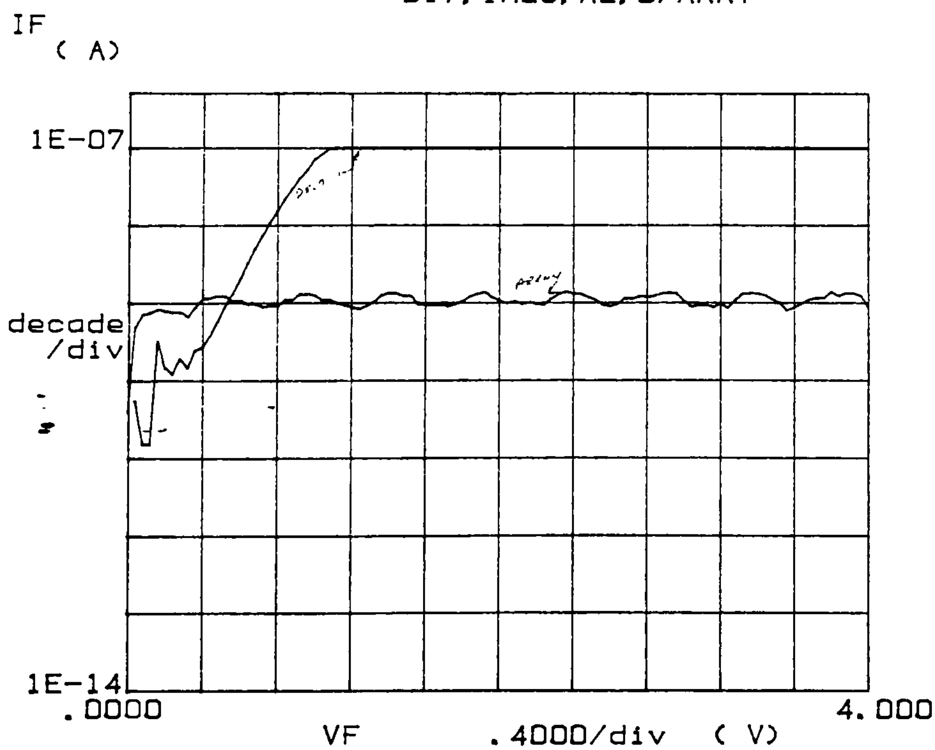
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

Constants:
V -Ch3 .0000V

I^2

****** GRAPHICS PLOT ******

B17, 1MEG, AL, D/ARRY

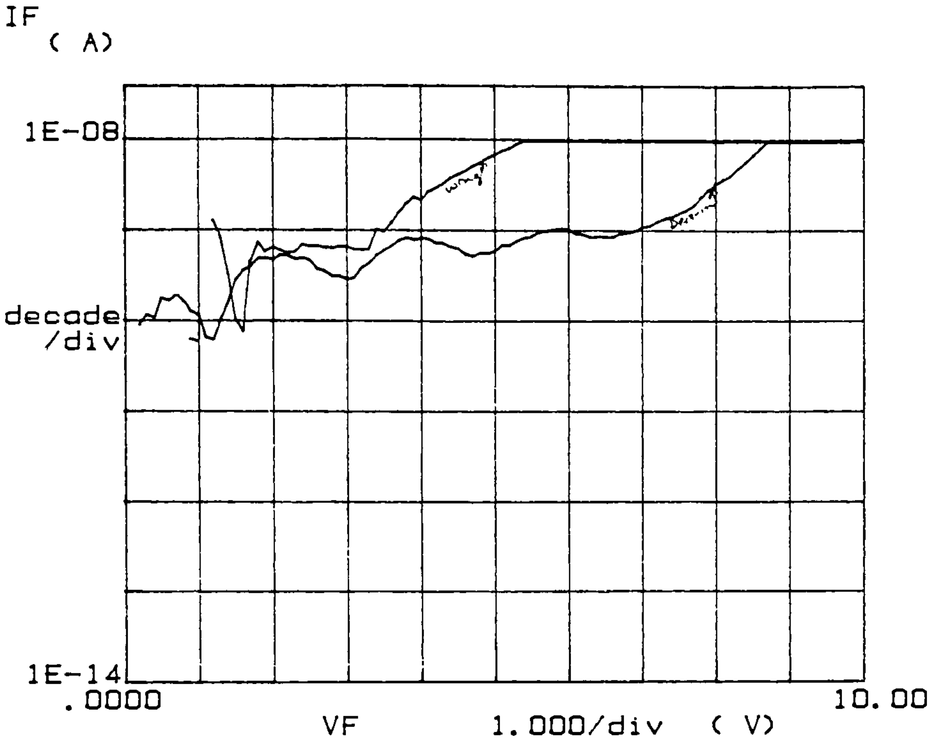


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B01, 100K, POLY, D/W

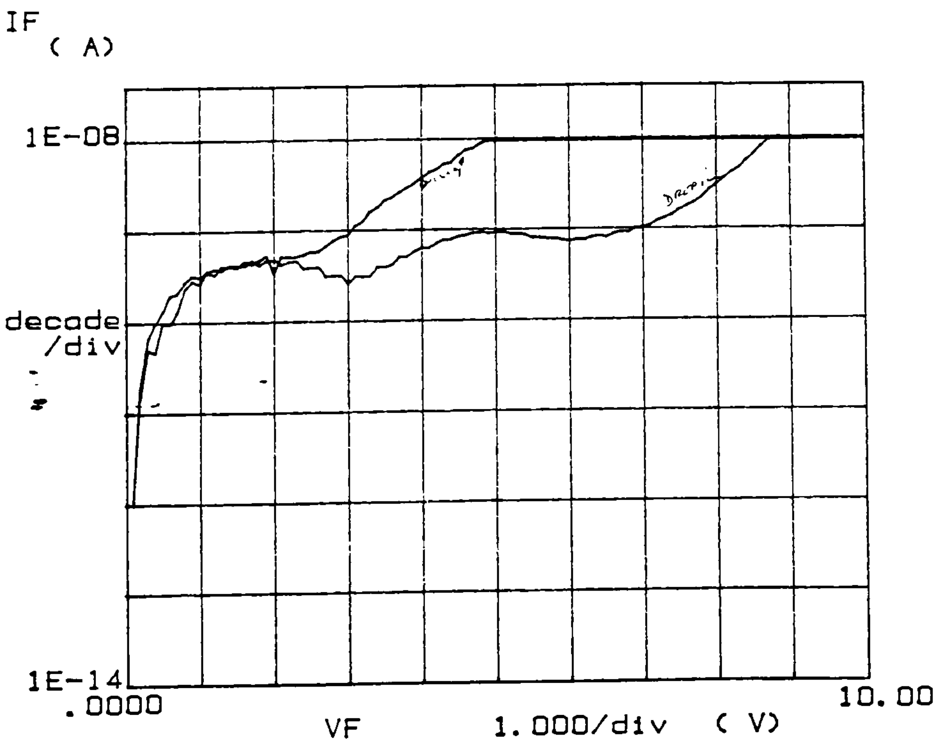


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

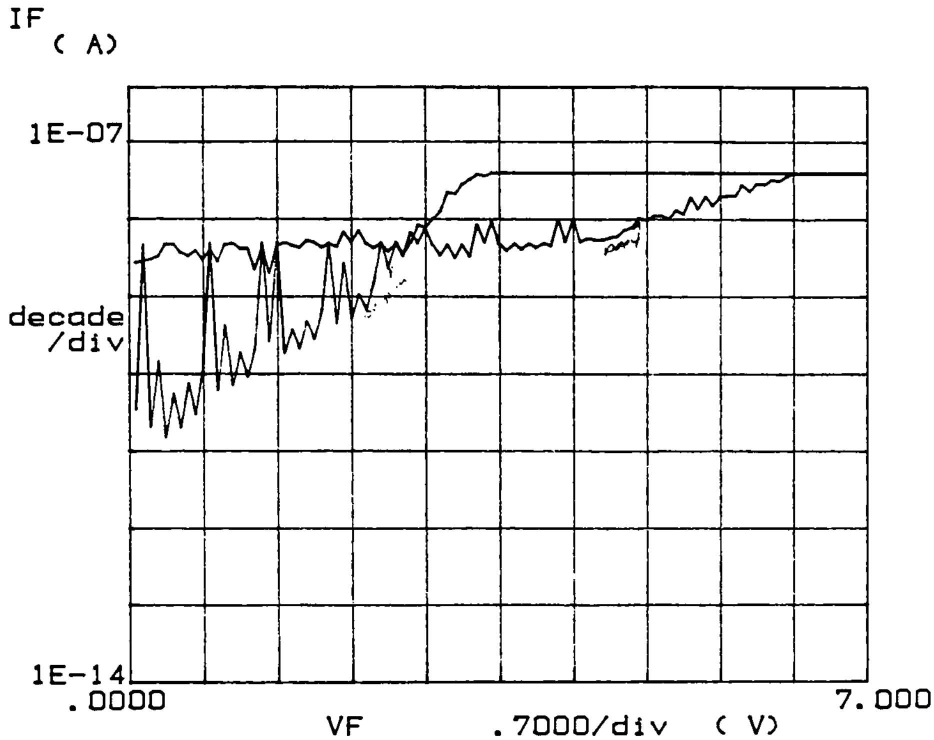
B01, 100K, POLY, D/W



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

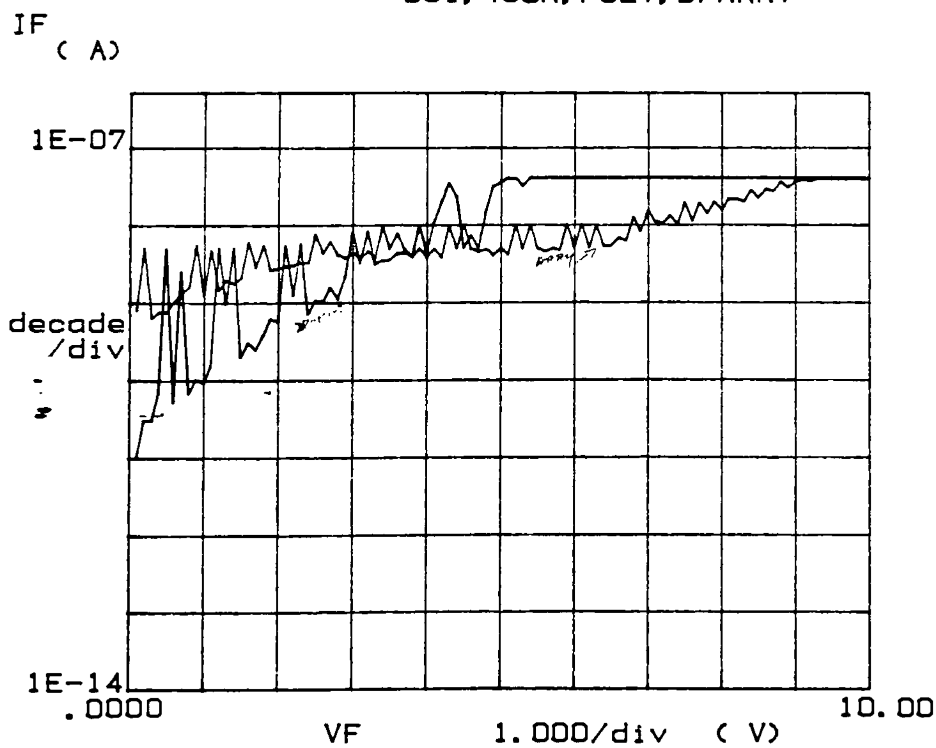
****** GRAPHICS PLOT ******
B01, 400K, POLY, D/ARRY



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 7.0000V
Step .0700V

Constants:
V -Ch3 .0000V

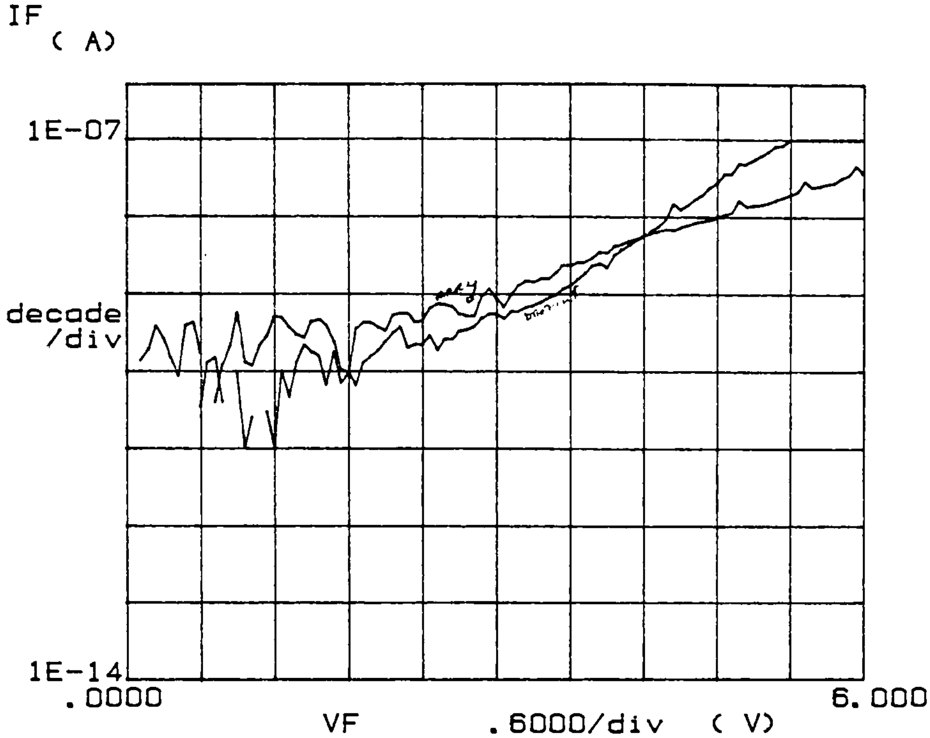
****** GRAPHICS PLOT ******
B01, 400K, POLY, D/ARRY



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

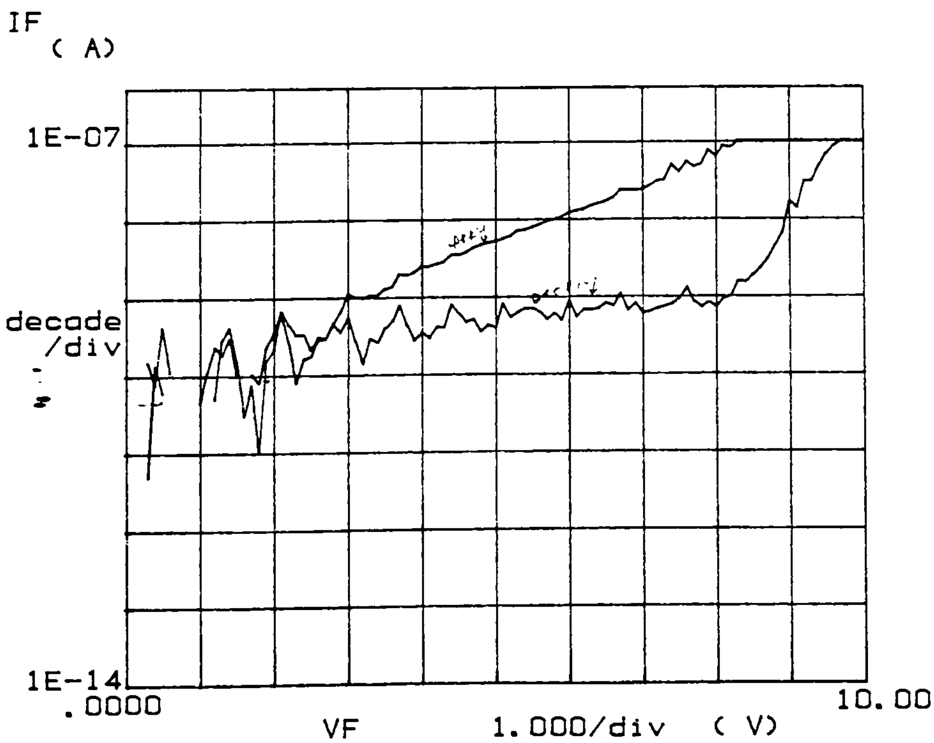
****** GRAPHICS PLOT ******
B01, 1MEG, POLY, D/ARRY



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 6.0000V
Step .0600V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******
B01, 1MEG, POLY, D/ARRY

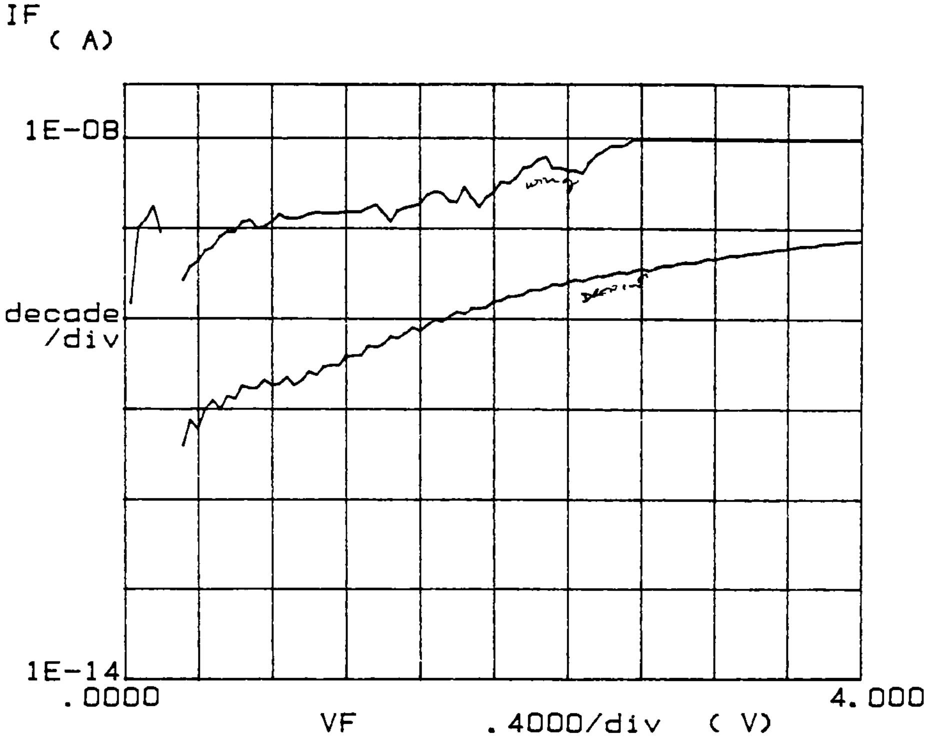


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

808, 100K, AL, D/W

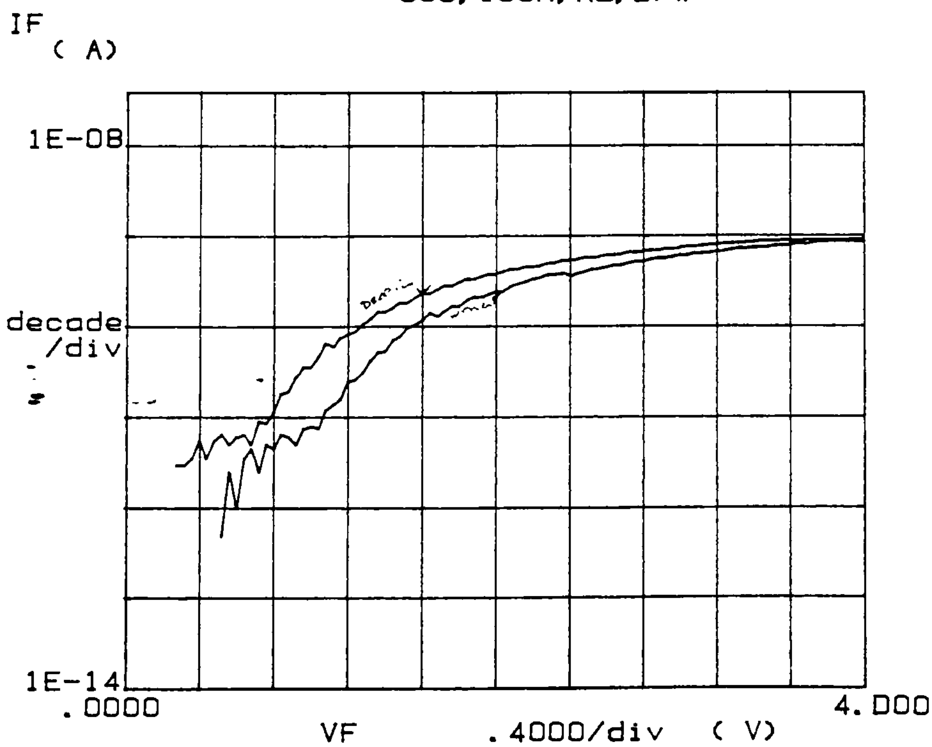


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

808, 100K, AL, D/W

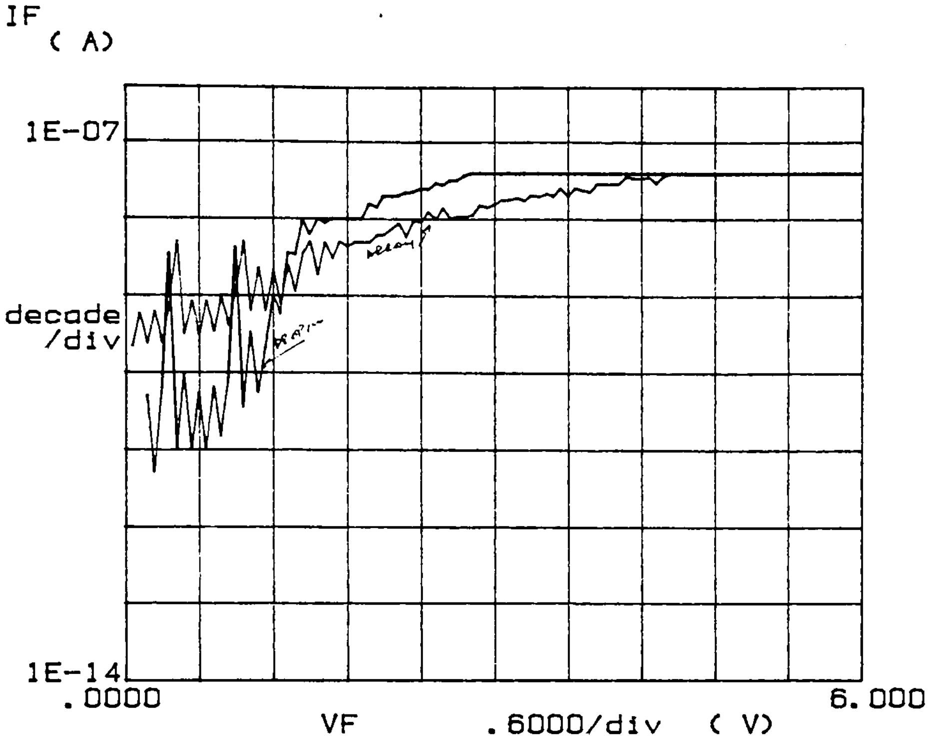


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 4.0000V
Step .0400V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

808, 400K, AL, D/ARRY

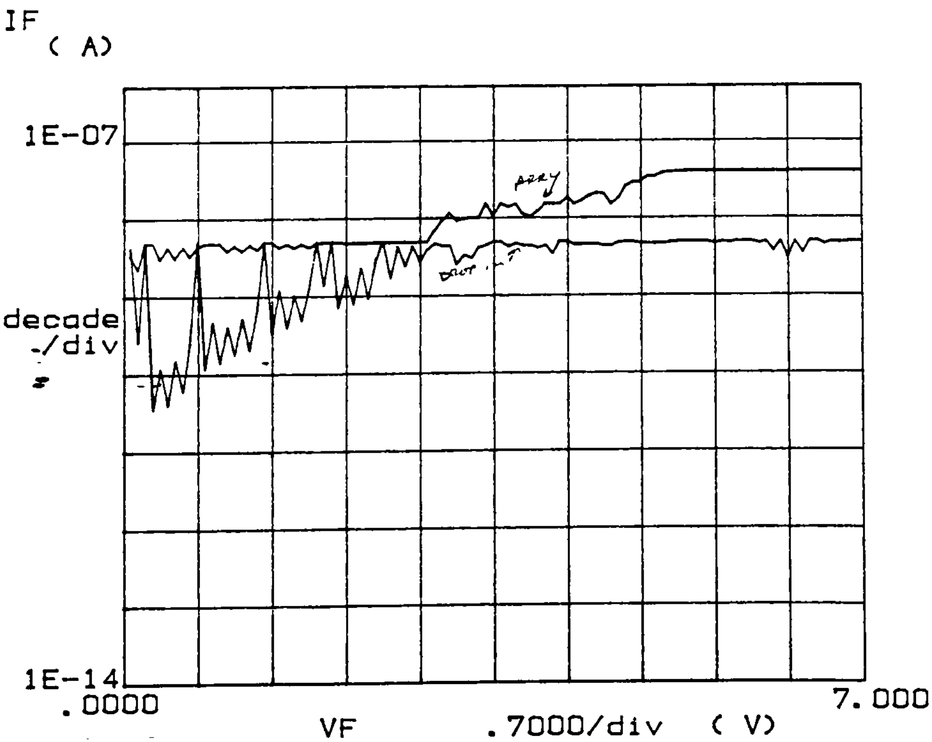


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 6.0000V
Step .0600V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

808, 400K, AL, D/ARRY

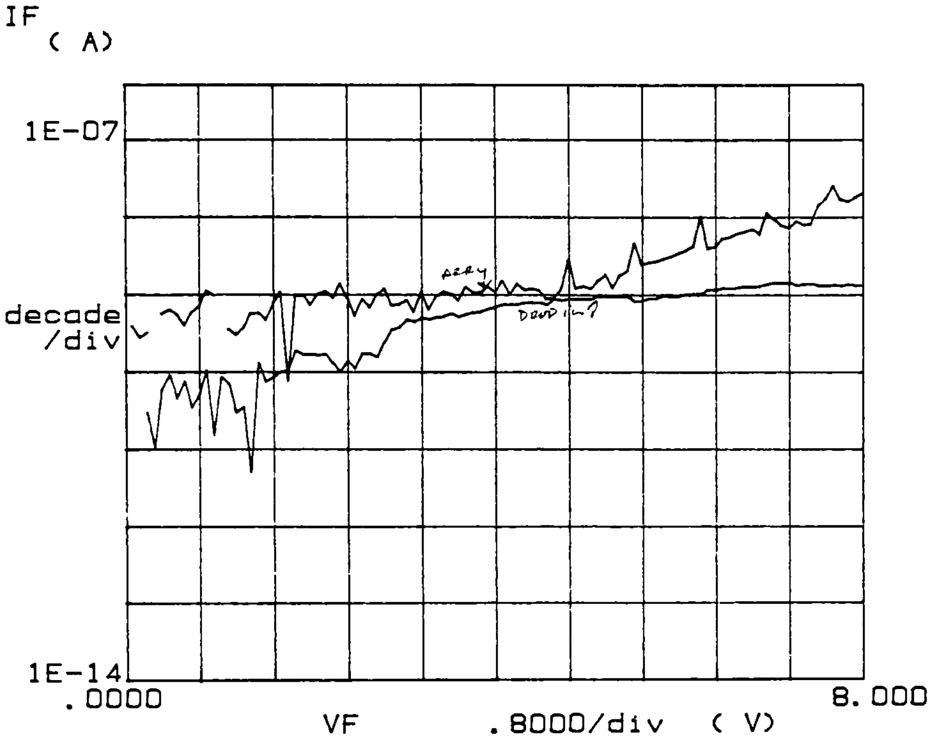


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 7.0000V
Step .0700V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B08, 1MEG, AL, D/ARRY

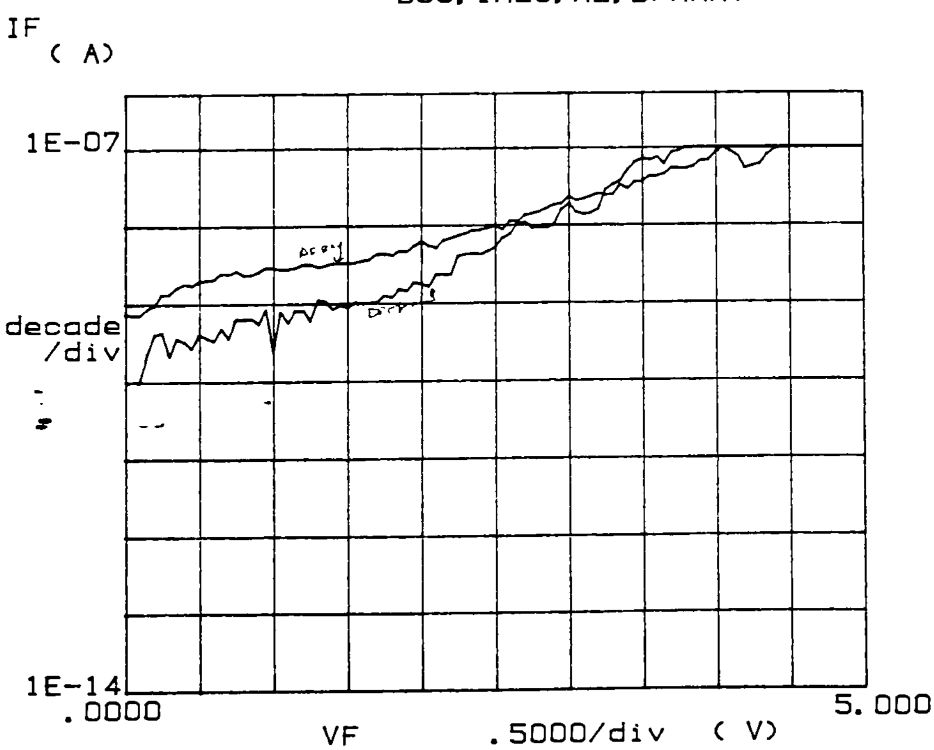


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 8.0000V
Step .0800V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B08, 1MEG, AL, D/ARRY

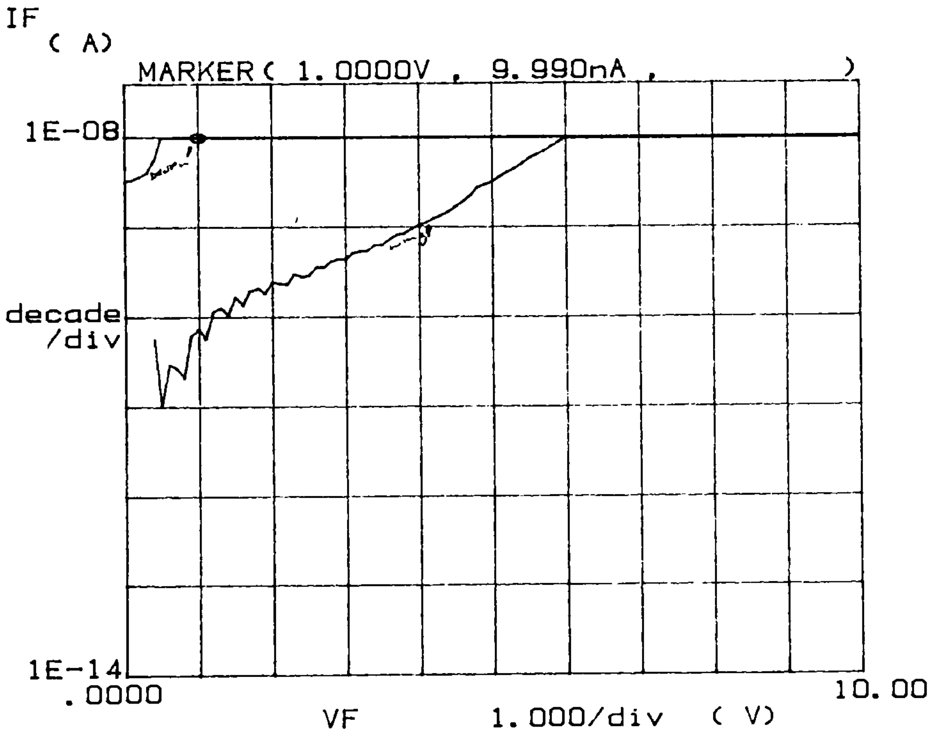


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 5.0000V
Step .0500V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B16, 100K, POLY, D/W

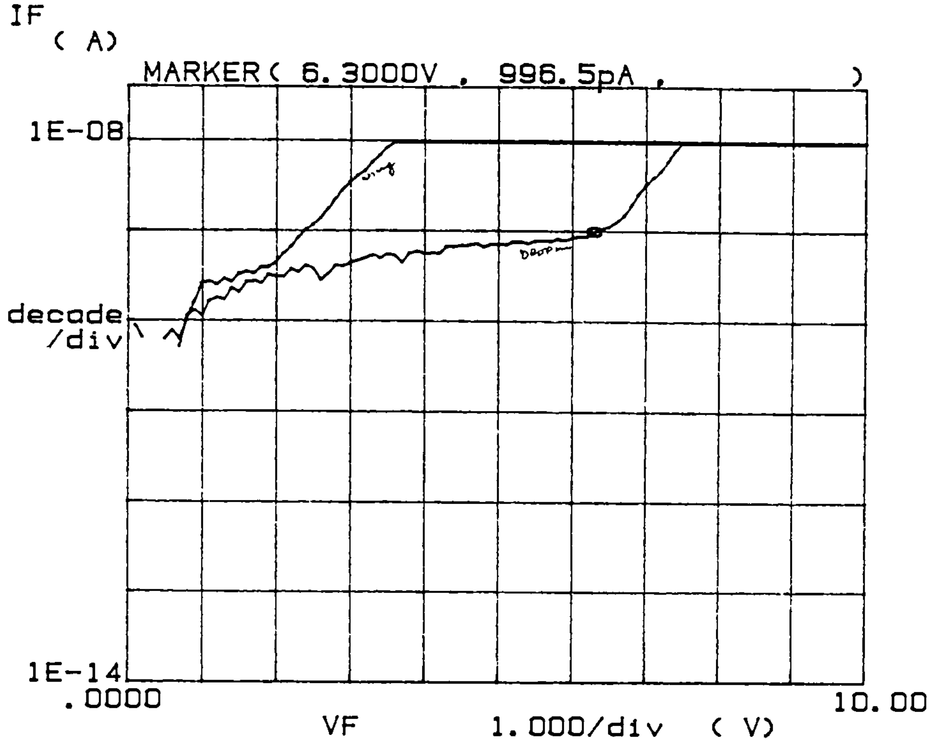


Variables:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B16, 100K, POLY, D/W

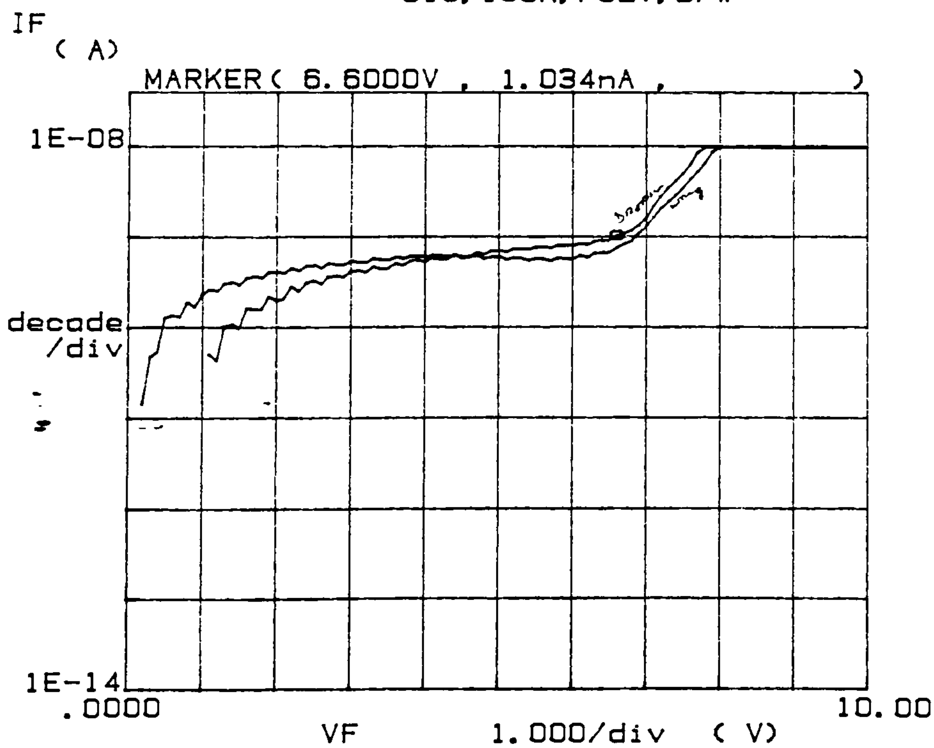


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B16, 100K, POLY, D/W

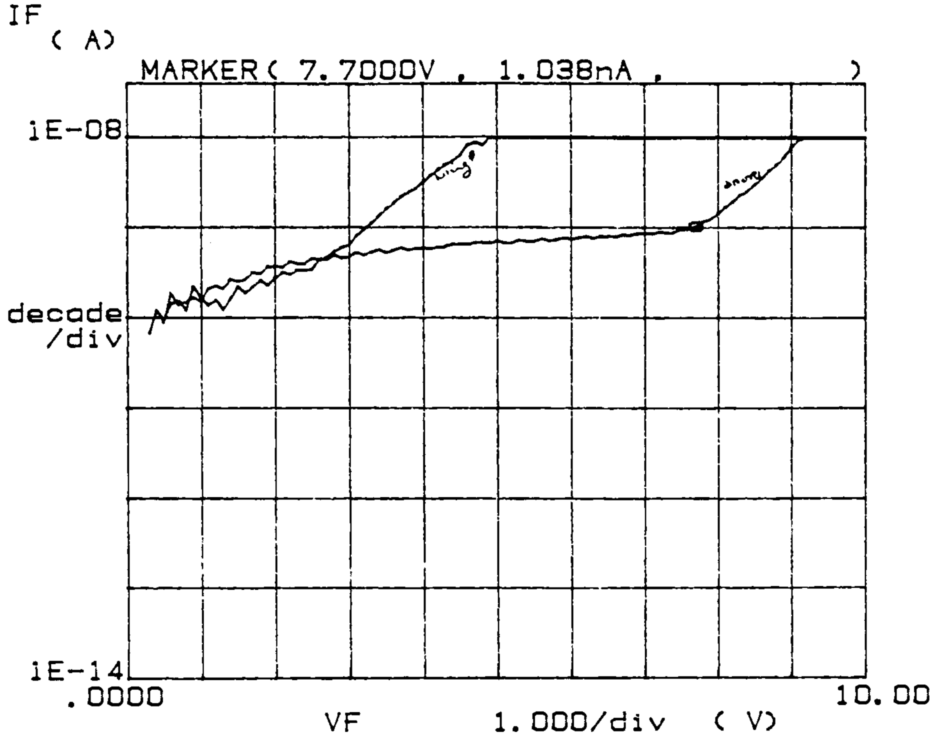


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B16, 100K, POLY, D/W

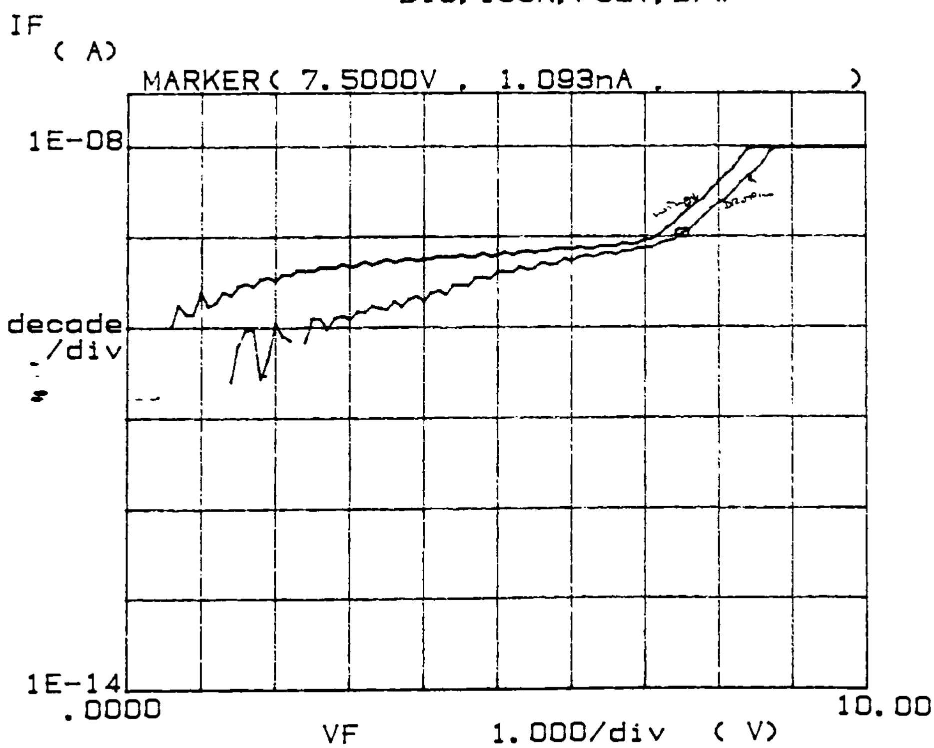


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B16, 100K, POLY, D/W

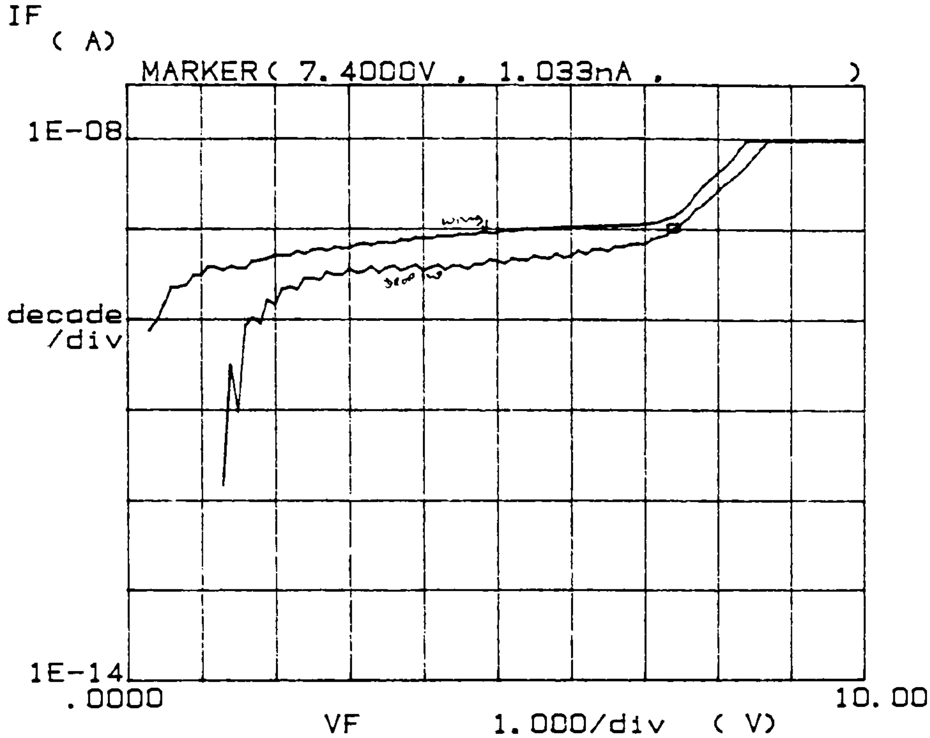


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B16, 100K, POLY, D/W

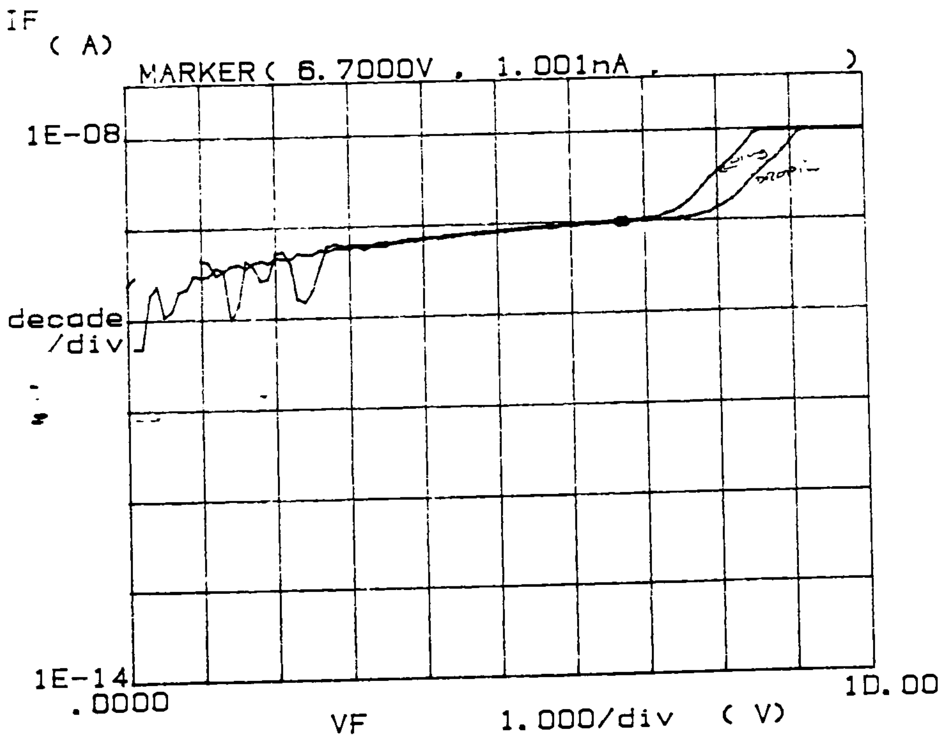


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V

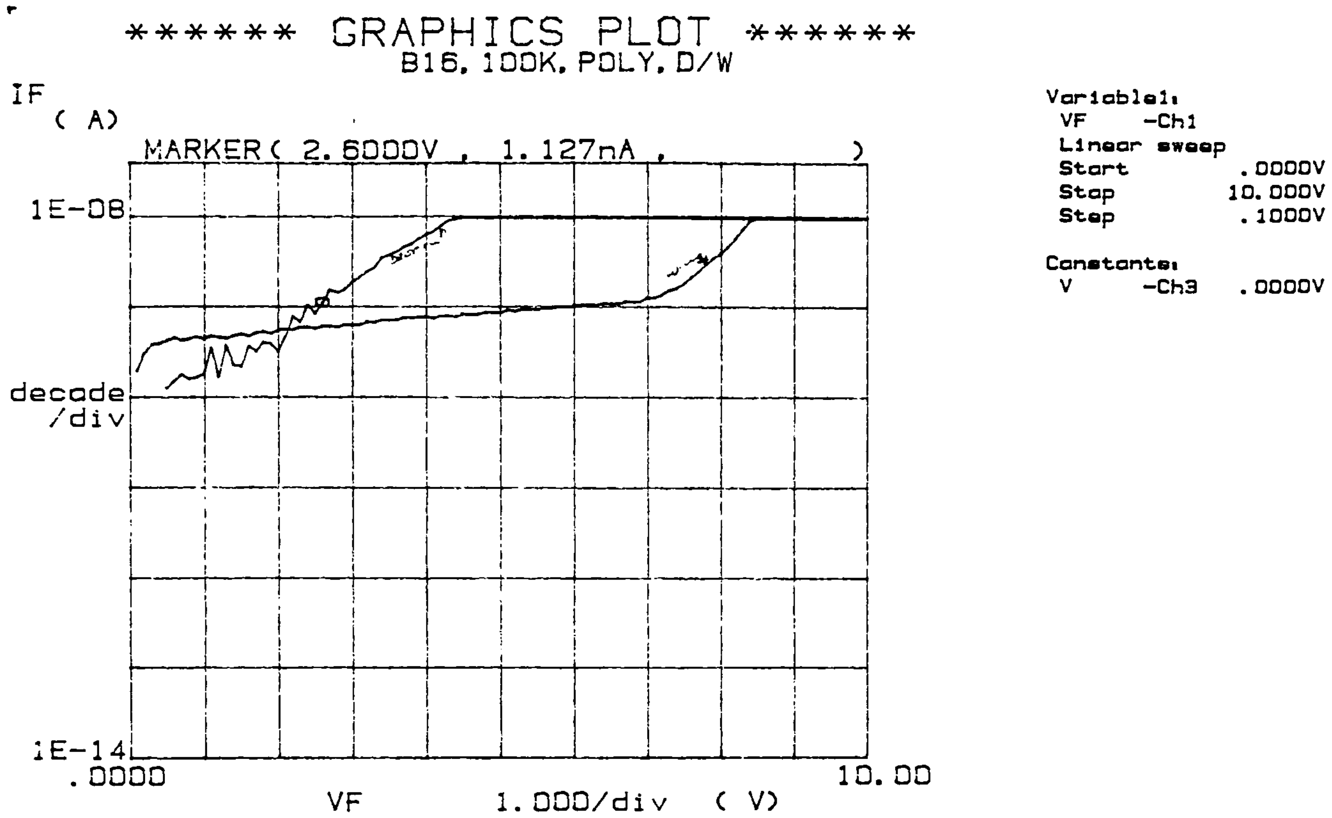
****** GRAPHICS PLOT ******

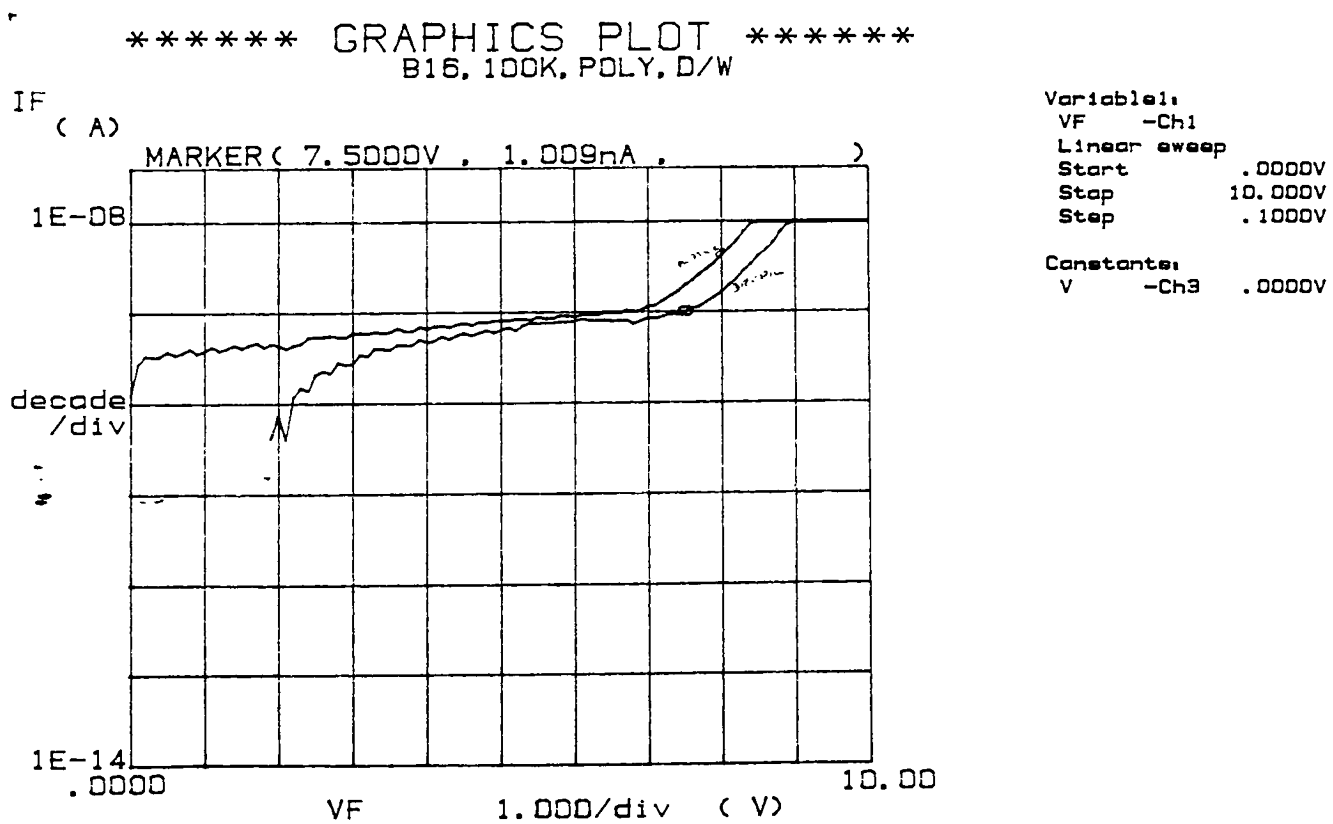
B16, 100K, POLY, D/W



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Constants:
V -Ch3 .0000V





$A = 10^{-3}$ cm^2, NO I^2

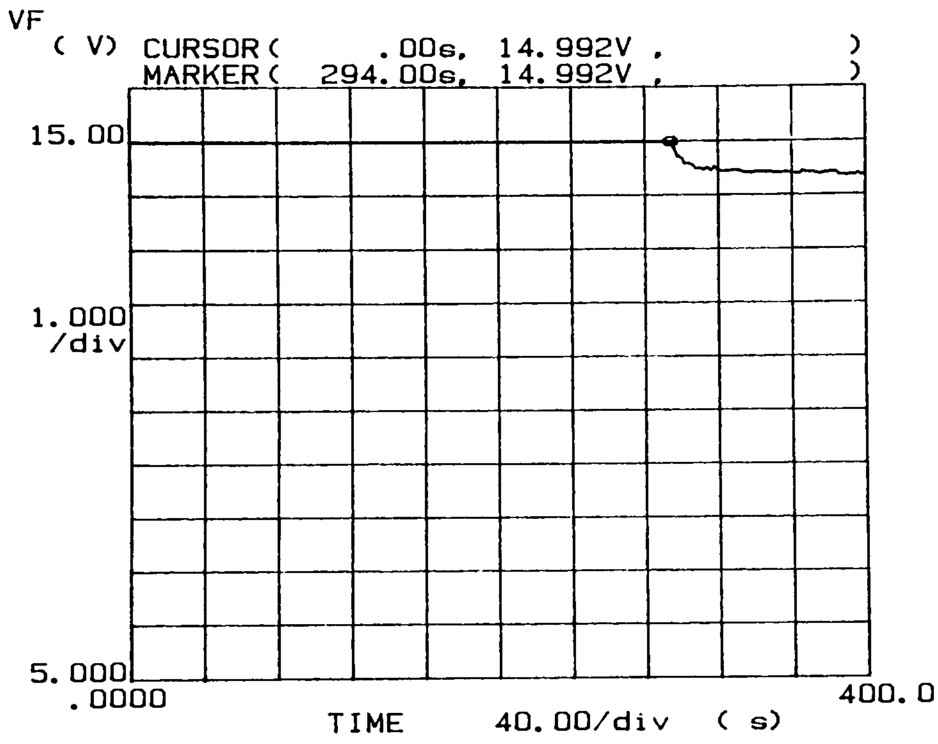
Appendix E

Charge to Breakdown plots of test structures

1500 Å Etch Back Results

****** GRAPHICS PLOT ******

B05, 100K, POLY, WINGS

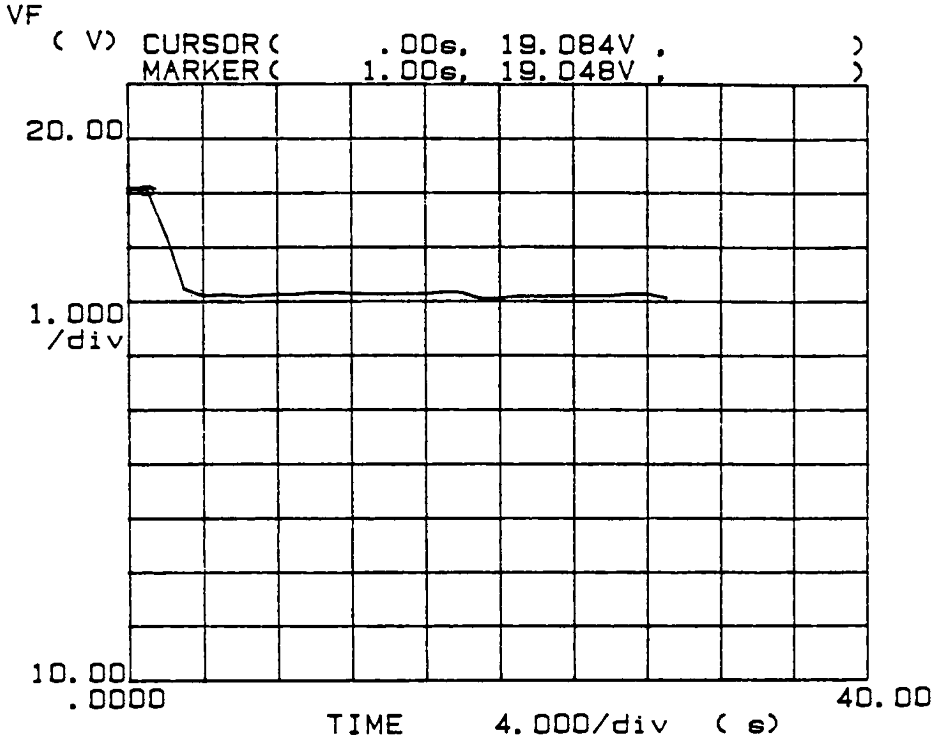


Time:
Wait time .00s
Interval 2.00s
Readings 300

Constants:
IF -Ch1 500.0uA
V -Ch3 .0000V

****** GRAPHICS PLOT ******

B05, 100K, POLY, WINGS

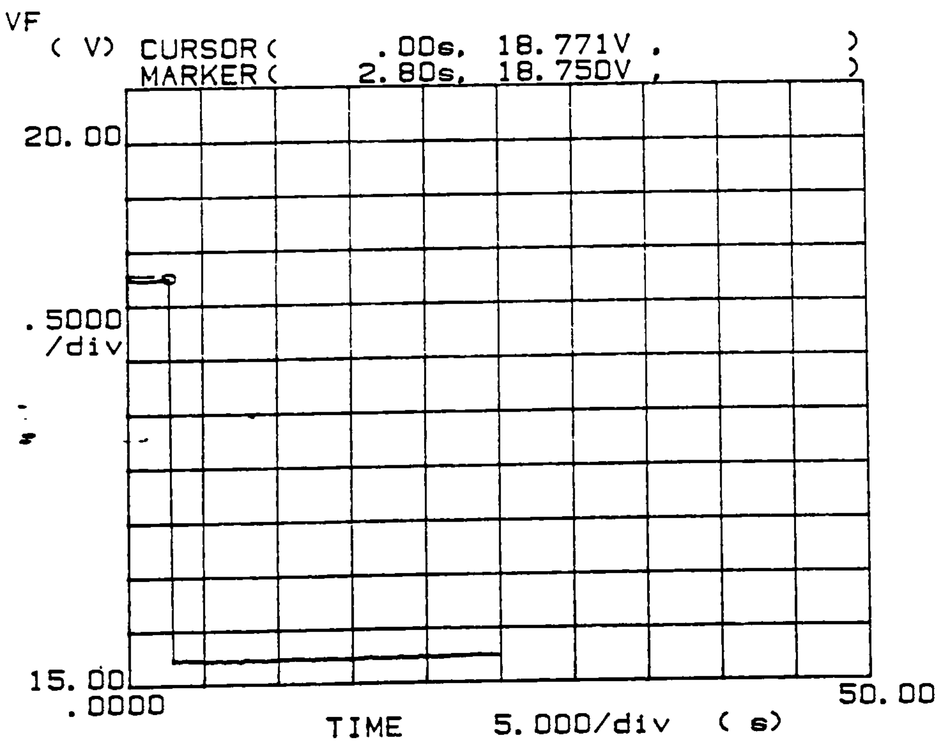


Time:
Wait time .00s
Interval 1.00s
Readings 30

Constants:
IF -Ch1 1.000mA
V -Ch3 .0000V

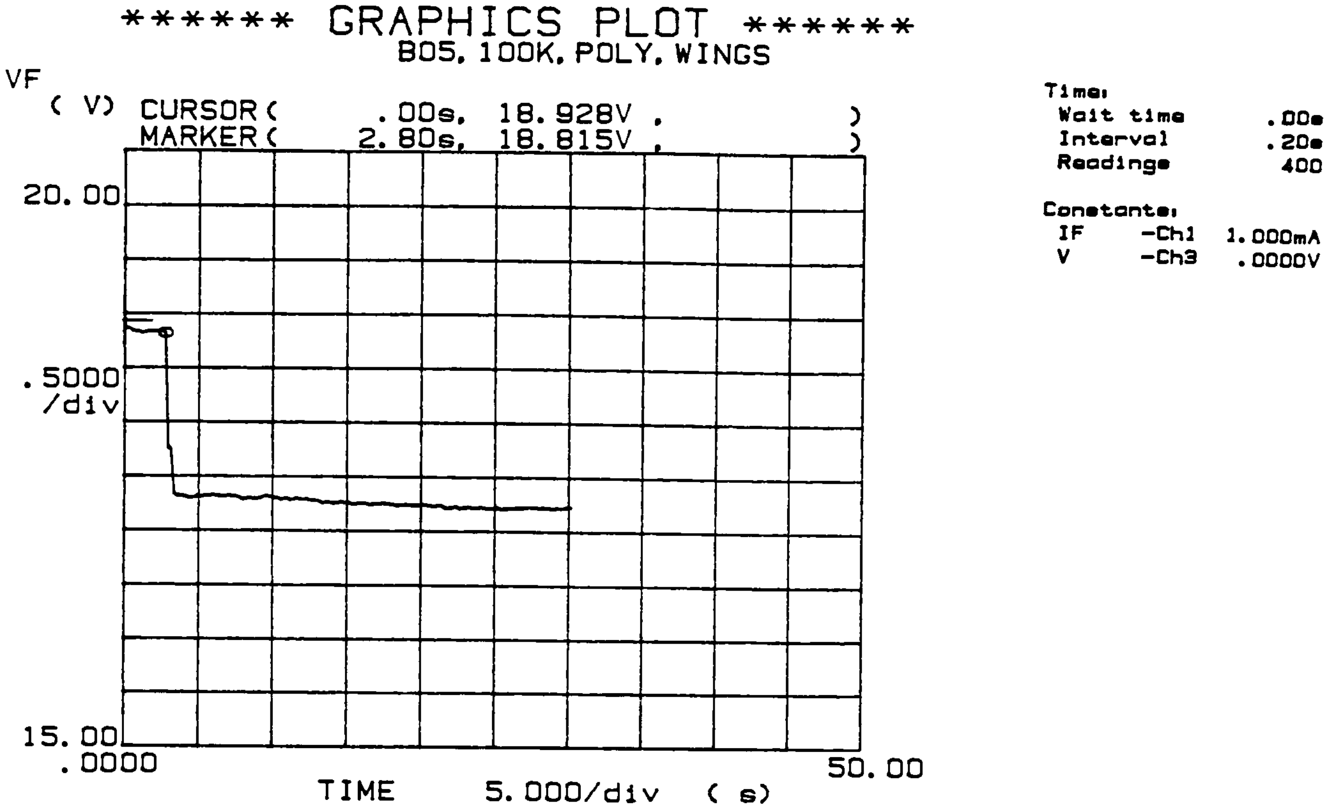
****** GRAPHICS PLOT ******

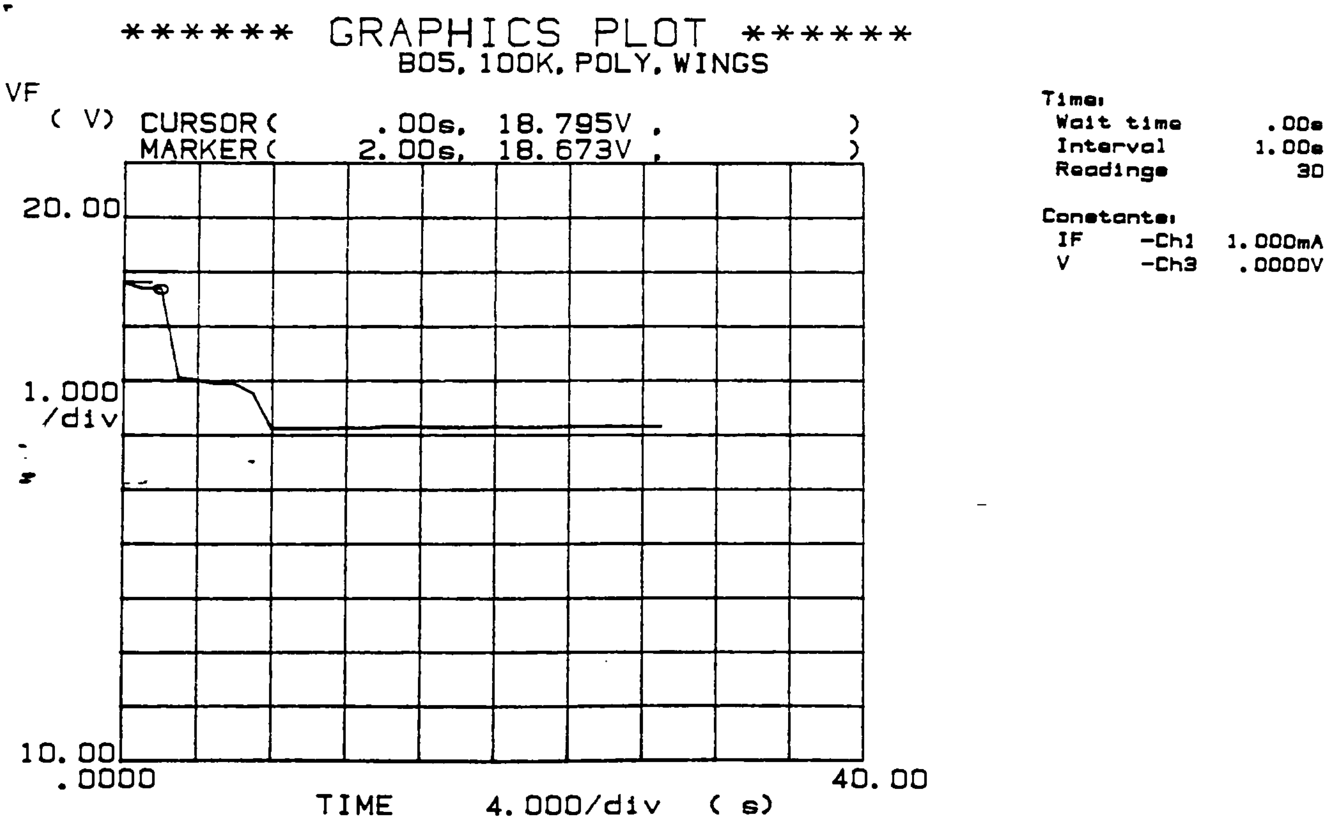
B05, 100K, POLY, WINGS

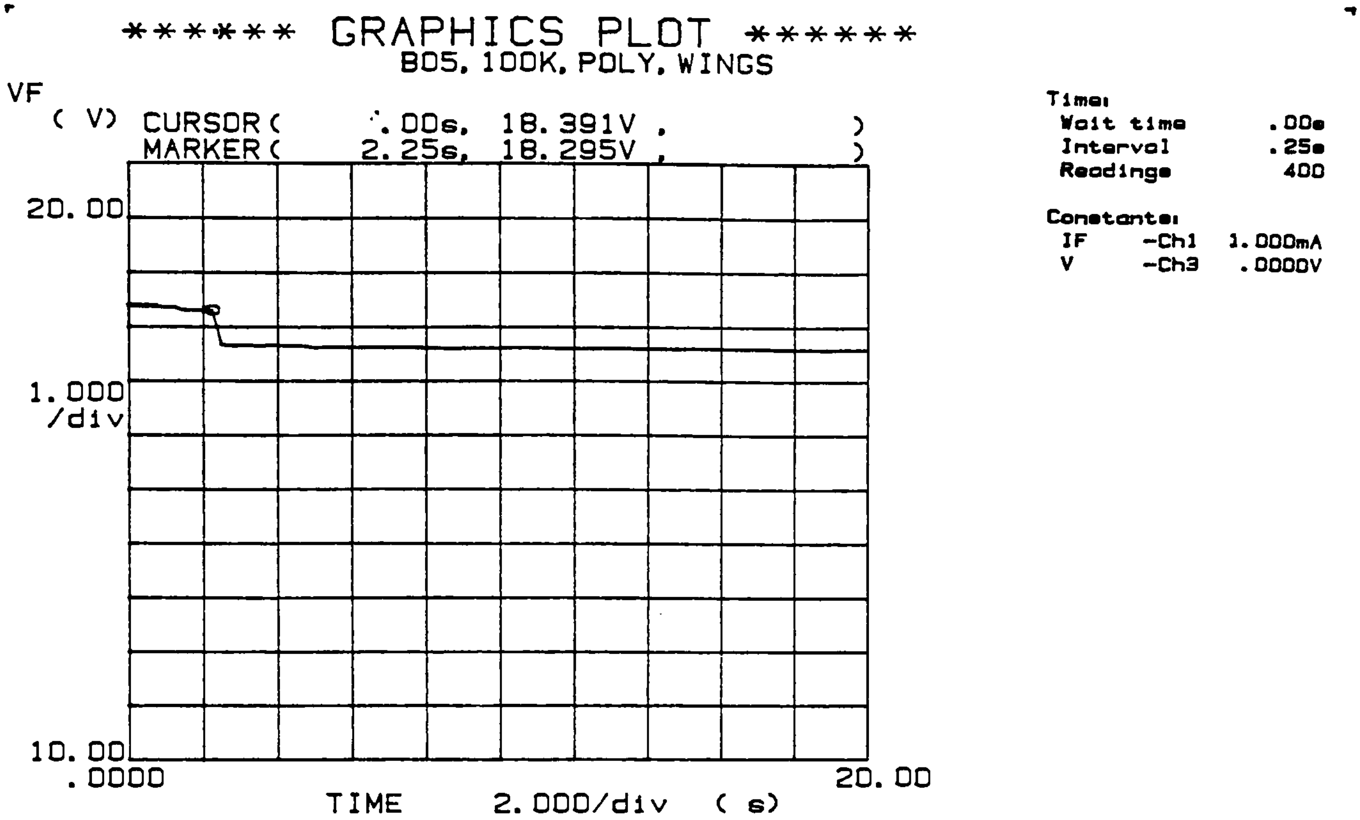


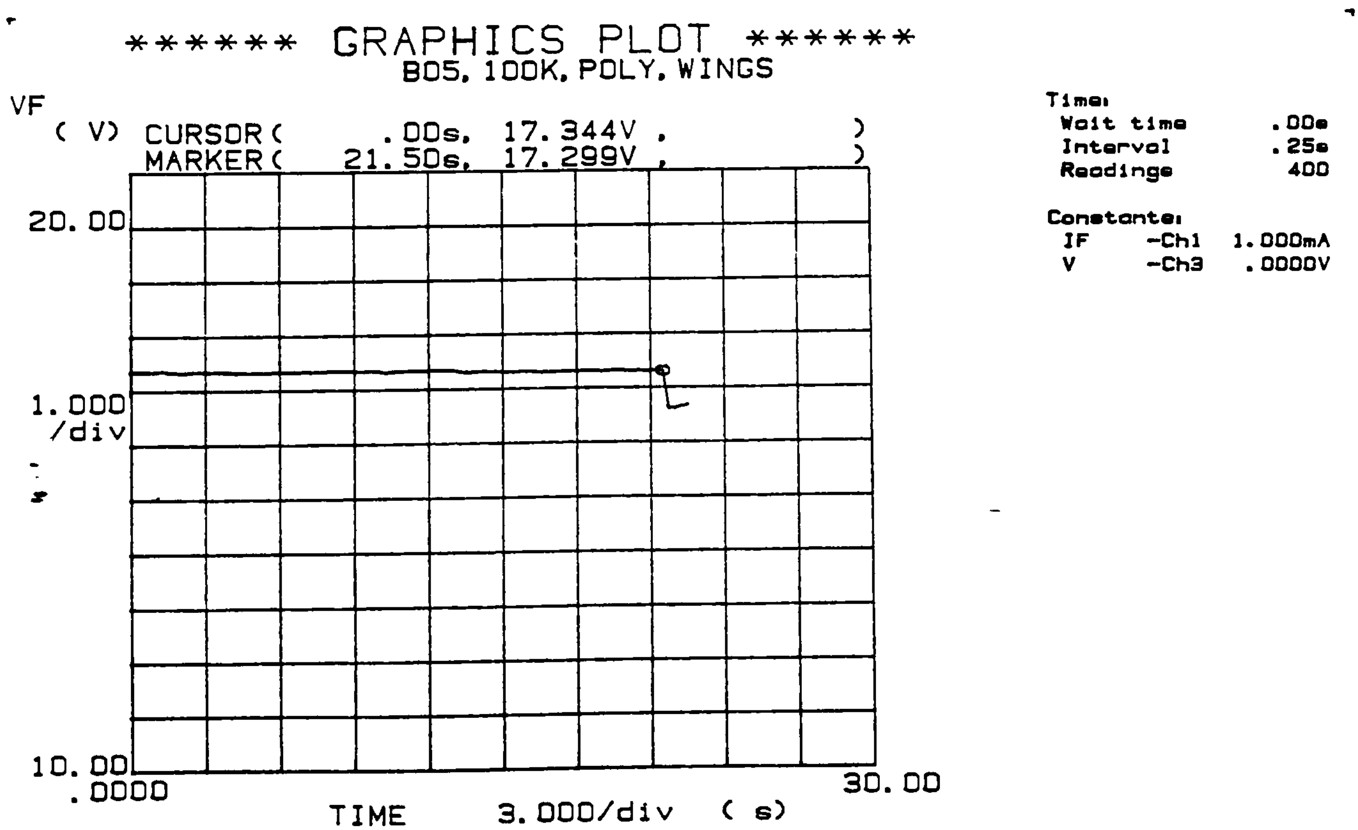
Time:
Wait time .00s
Interval .20s
Readings 400

Constants:
IF -Ch1 1.000mA
V -Ch3 .0000V

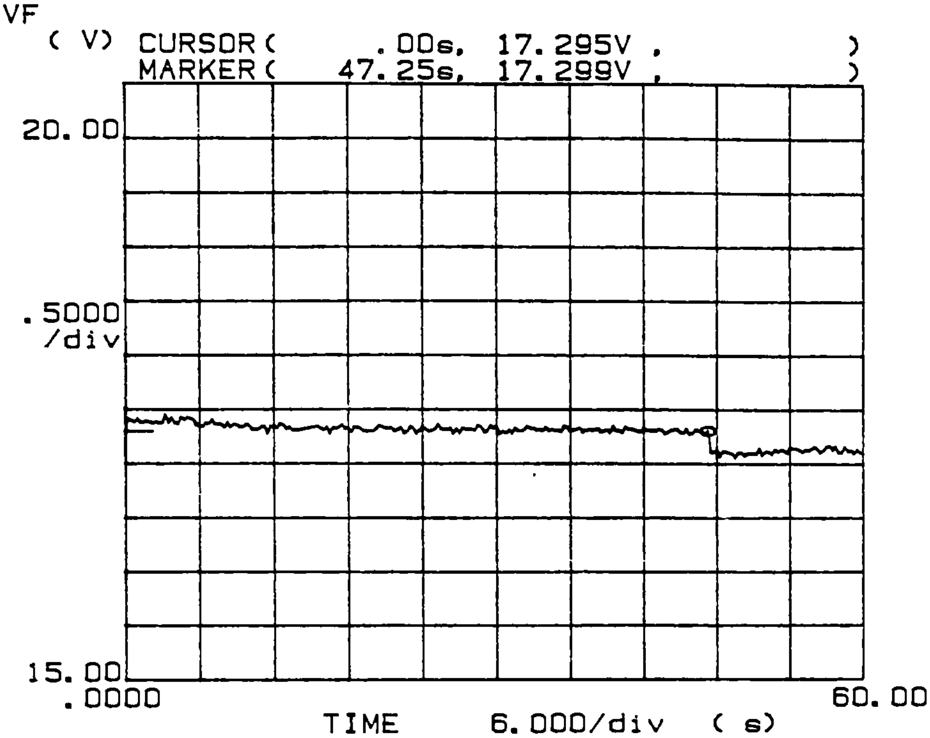

****** GRAPHICS PLOT ******
B05, 100K, POLY, WINGS
VF
(V) CURSOR (.00s, 18.928V ,)
MARKER (2.80s, 18.815V ,)
20.00
.5000
/div
15.00
.0000
50.00
TIME 5.000/div (s)
Time:
Wait time .00s
Interval .20s
Readings 400
Constants:
IF -Ch1 1.000mA
V -Ch3 .0000V


****** GRAPHICS PLOT ******
B05, 100K, POLY, WINGS
VF
(V) CURSOR (.00s, 18.795V ,)
MARKER (2.00s, 18.673V ,)
20.00
1.000
/div
10.00
.0000
40.00
TIME 4.000/div (s)
Time:
Wait time .00s
Interval 1.00s
Readings 30
Constants:
IF -Ch1 1.000mA
V -Ch3 .0000V


****** GRAPHICS PLOT ******
B05, 100K, POLY, WINGS
VF
(V) CURSOR (.00s, 18.391V ,)
MARKER (2.25s, 18.295V ,)
20.00
1.000
/div
10.00
.0000
20.00
TIME 2.000/div (s)
Time:
Wait time .00s
Interval .25s
Readings 400
Constants:
IF -Ch1 1.000mA
V -Ch3 .0000V


****** GRAPHICS PLOT ******
B05, 100K, POLY, WINGS
VF
(V) CURSOR (.00s, 17.344V ,)
MARKER (21.50s, 17.299V ,)
20.00
1.000
/div
10.00
.0000
30.00
TIME 3.000/div (s)
Time:
Wait time .00s
Interval .25s
Readings 400
Constants:
IF -Ch1 1.000mA
V -Ch3 .0000V

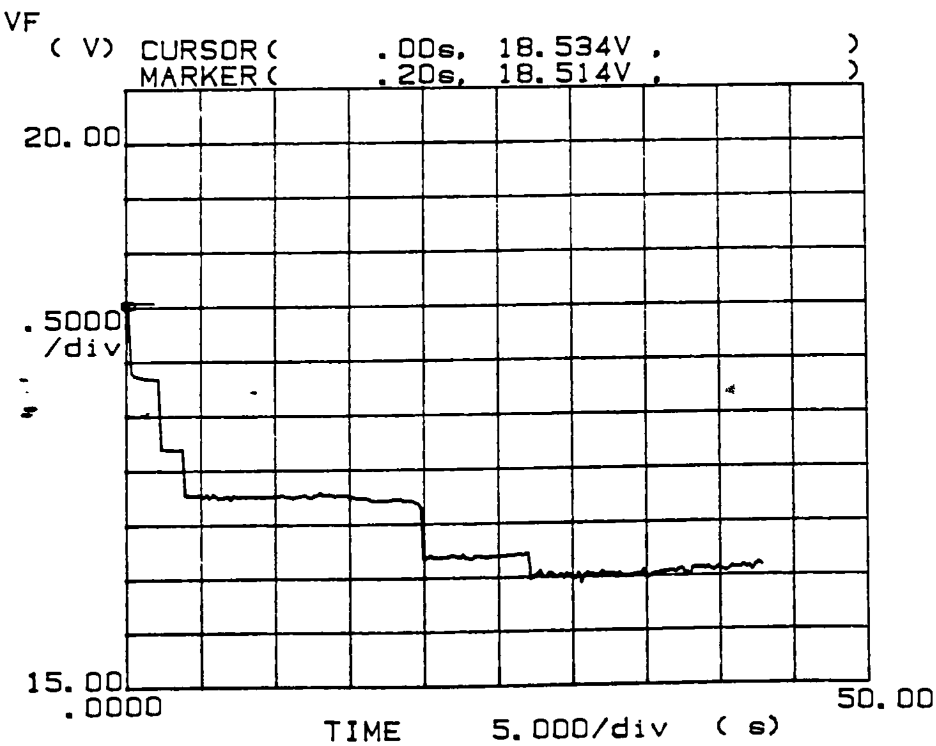
****** GRAPHICS PLOT ******
B05, 100K, POLY, WINGS



Time:
Wait time .00s
Interval .25s
Readings 400

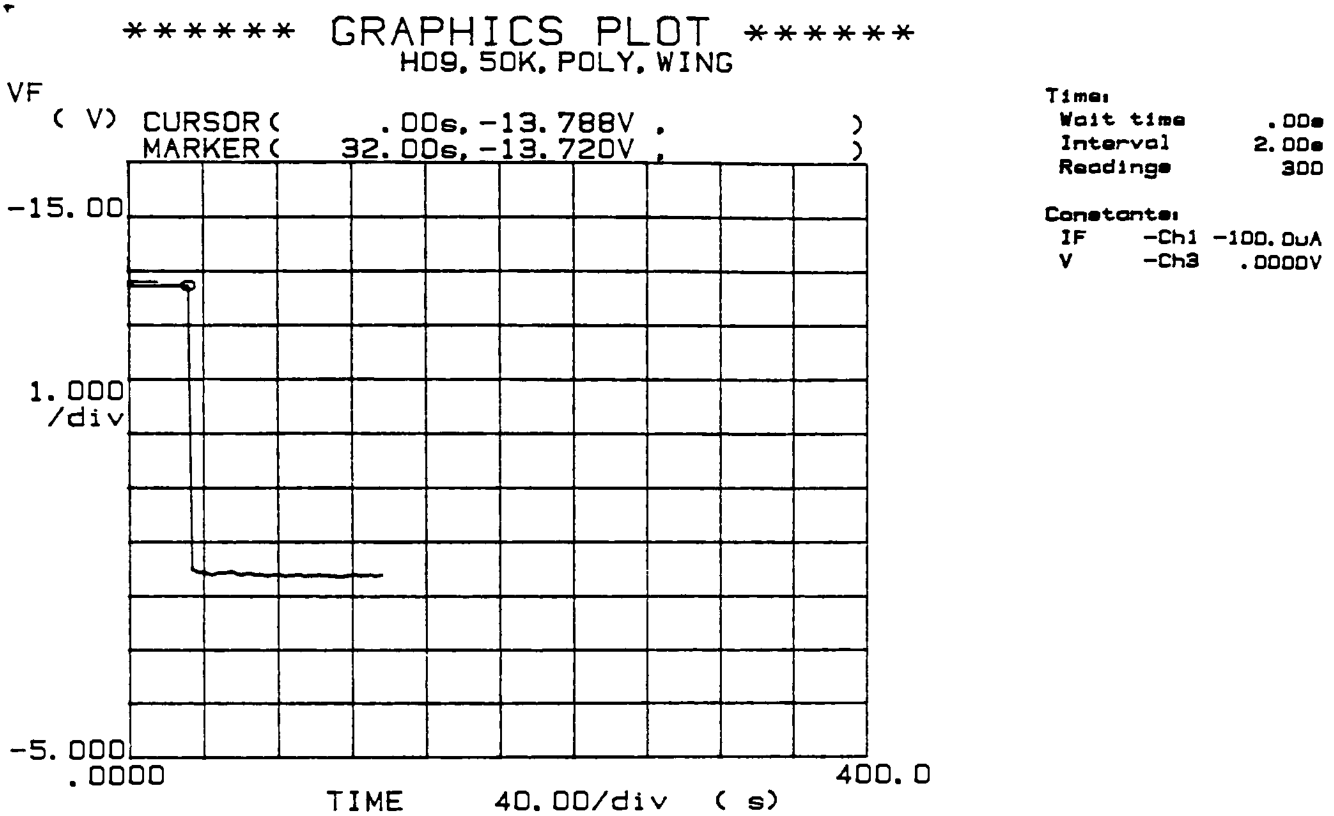
Constants:
IF -Ch1 1.000mA
V -Ch3 .0000V

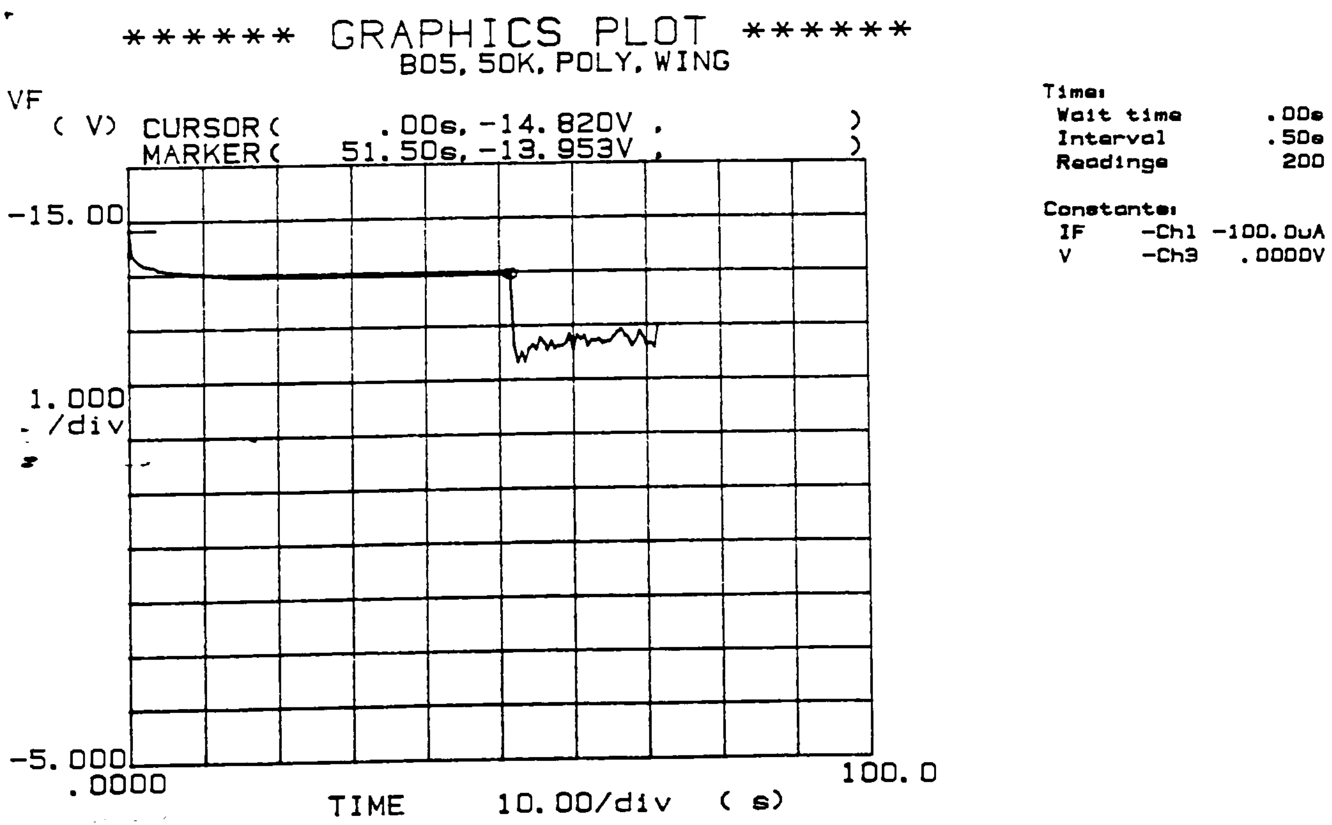
****** GRAPHICS PLOT ******
B05, 100K, POLY, WINGS

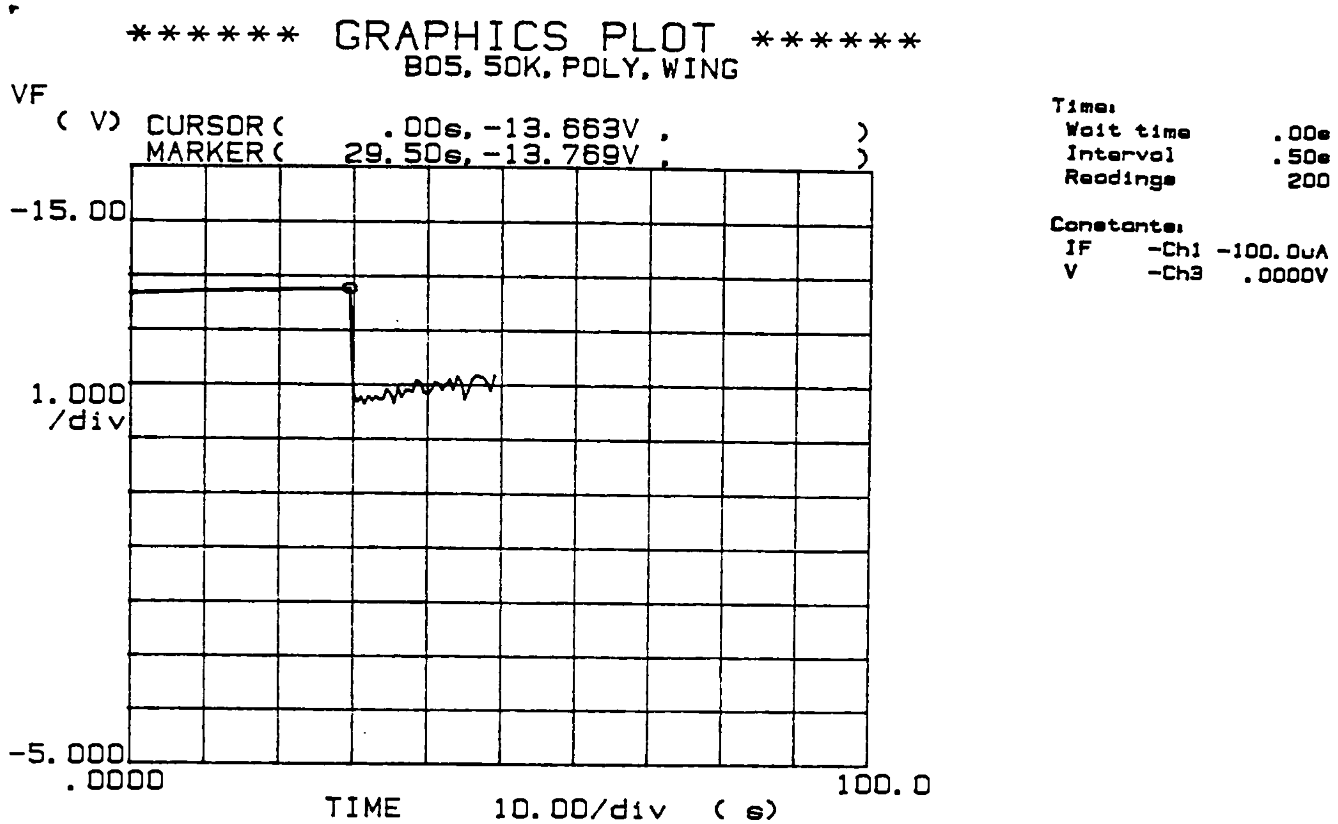


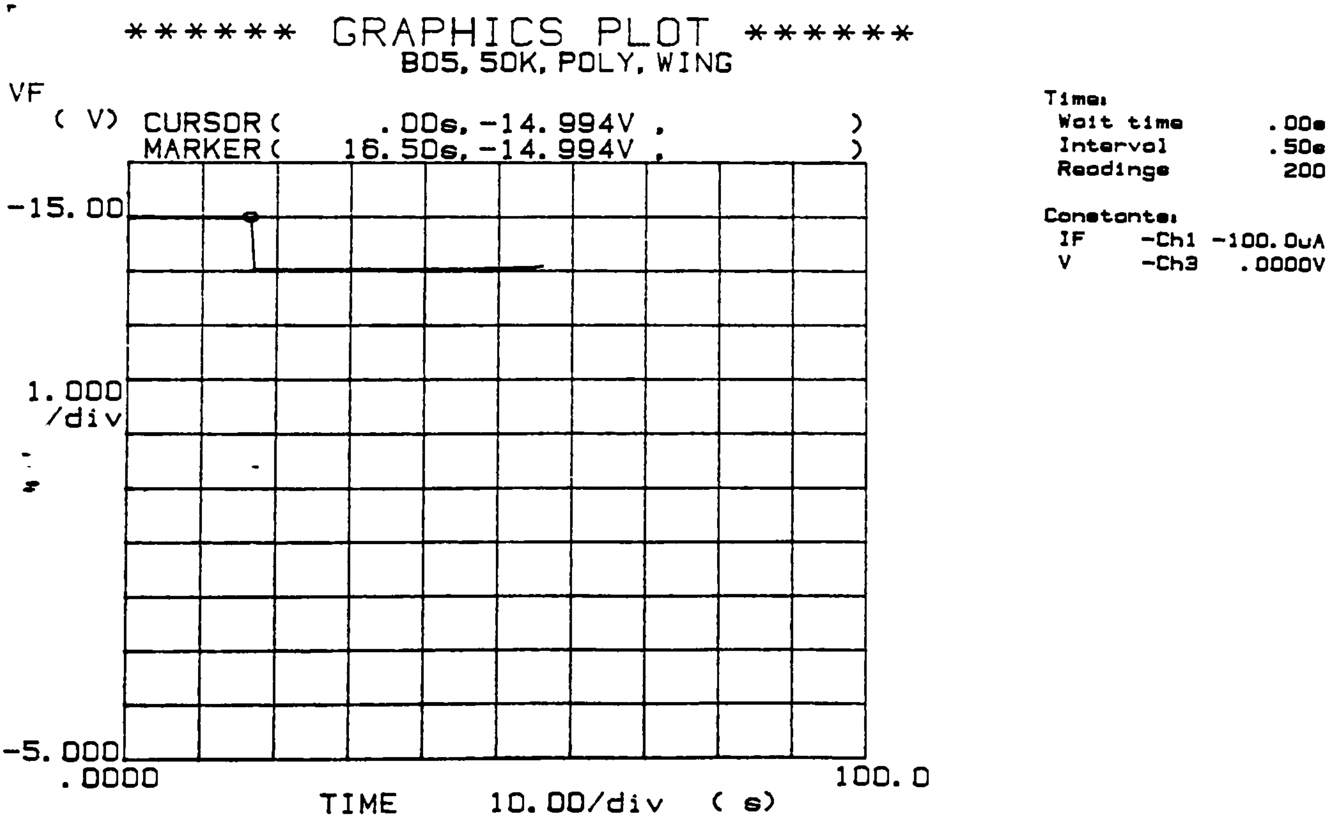
Time:
Wait time .00s
Interval .20s
Readings 400

Constants:
IF -Ch1 1.000mA
V -Ch3 .0000V

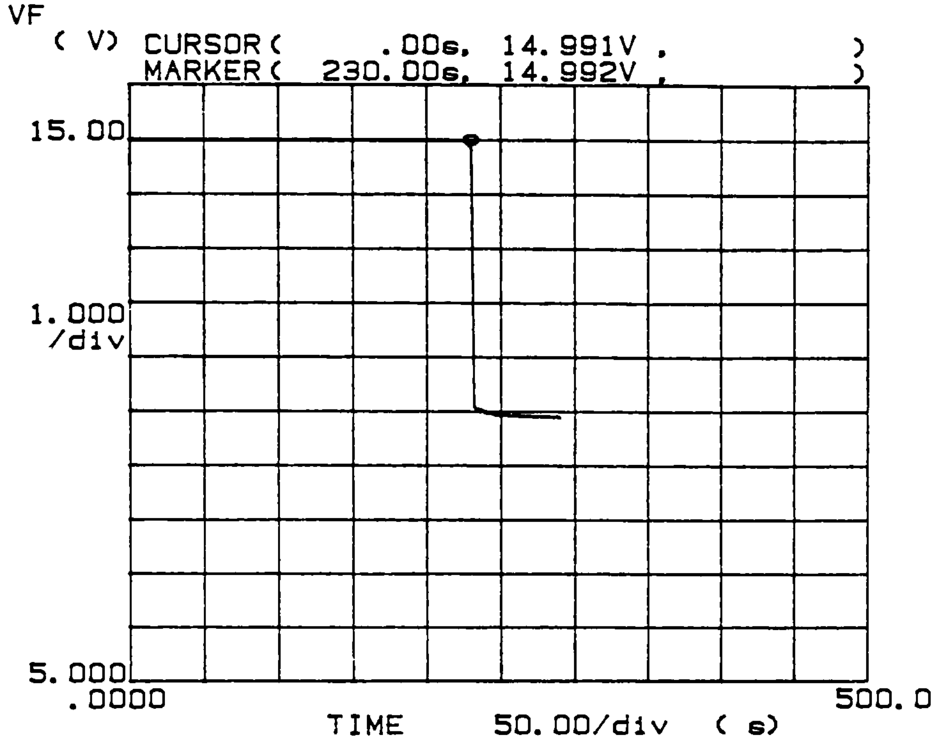

****** GRAPHICS PLOT ******
H09, 50K, POLY, WING
VF
(V) CURSOR (.00s, -13.788V ,)
MARKER (32.00s, -13.720V ,)
-15.00
1.000
/div
-5.000
.0000
400.0
TIME 40.00/div (s)
Time:
Wait time .00s
Interval 2.00s
Readings 300
Constants:
IF -Ch1 -100.0uA
V -Ch3 .0000V


****** GRAPHICS PLOT ******
B05, 50K, POLY, WING
VF
(V) CURSOR (.00s, -14.820V ,)
MARKER (51.50s, -13.953V ,)
-15.00
1.000
/div
-5.000
.0000
100.0
TIME 10.00/div (s)
Time:
Wait time .00s
Interval .50s
Readings 200
Constants:
IF -Ch1 -100.0uA
V -Ch3 .0000V


****** GRAPHICS PLOT ******
B05, 50K, POLY, WING
VF
(V) CURSOR (.00s, -13.663V ,)
MARKER (29.50s, -13.769V ,)
-15.00
1.000
/div
-5.000
.0000
100.0
TIME 10.00/div (s)
Time:
Wait time .00s
Interval .50s
Readings 200
Constants:
IF -Ch1 -100.0uA
V -Ch3 .0000V


****** GRAPHICS PLOT ******
B05, 50K, POLY, WING
VF
(V) CURSOR (.00s, -14.994V ,)
MARKER (16.50s, -14.994V ,)
-15.00
1.000
/div
-5.000
.0000
100.0
TIME 10.00/div (s)
Time:
Wait time .00s
Interval .50s
Readings 200
Constants:
IF -Ch1 -100.0uA
V -Ch3 .0000V

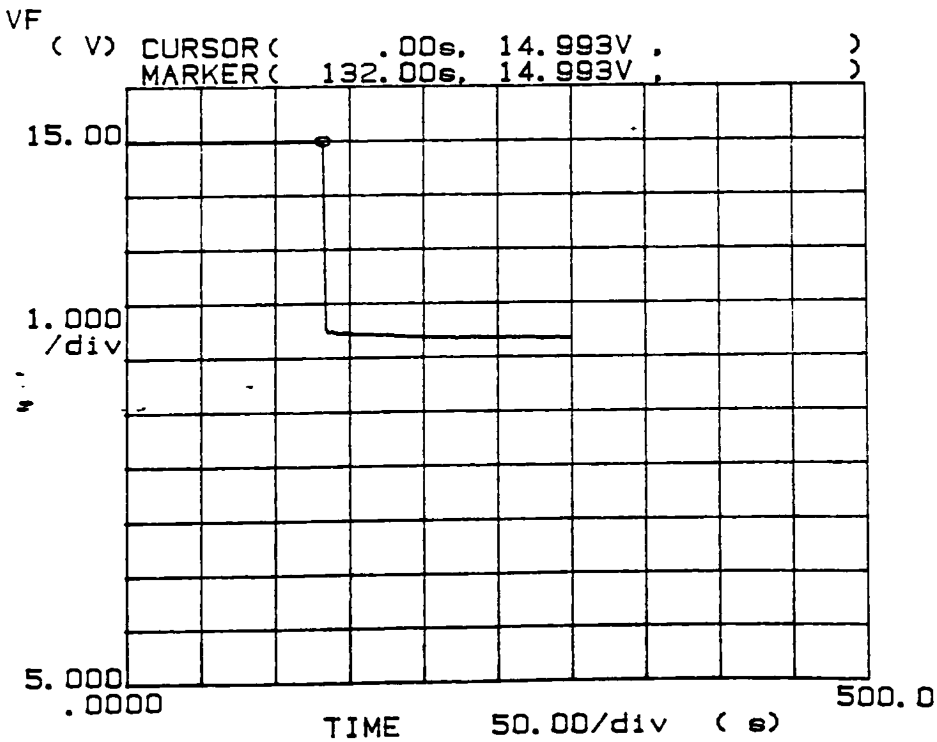
****** GRAPHICS PLOT ******
B03, 100K, POLY, WING



Time:
Wait time .00s
Interval 2.00s
Readings 250

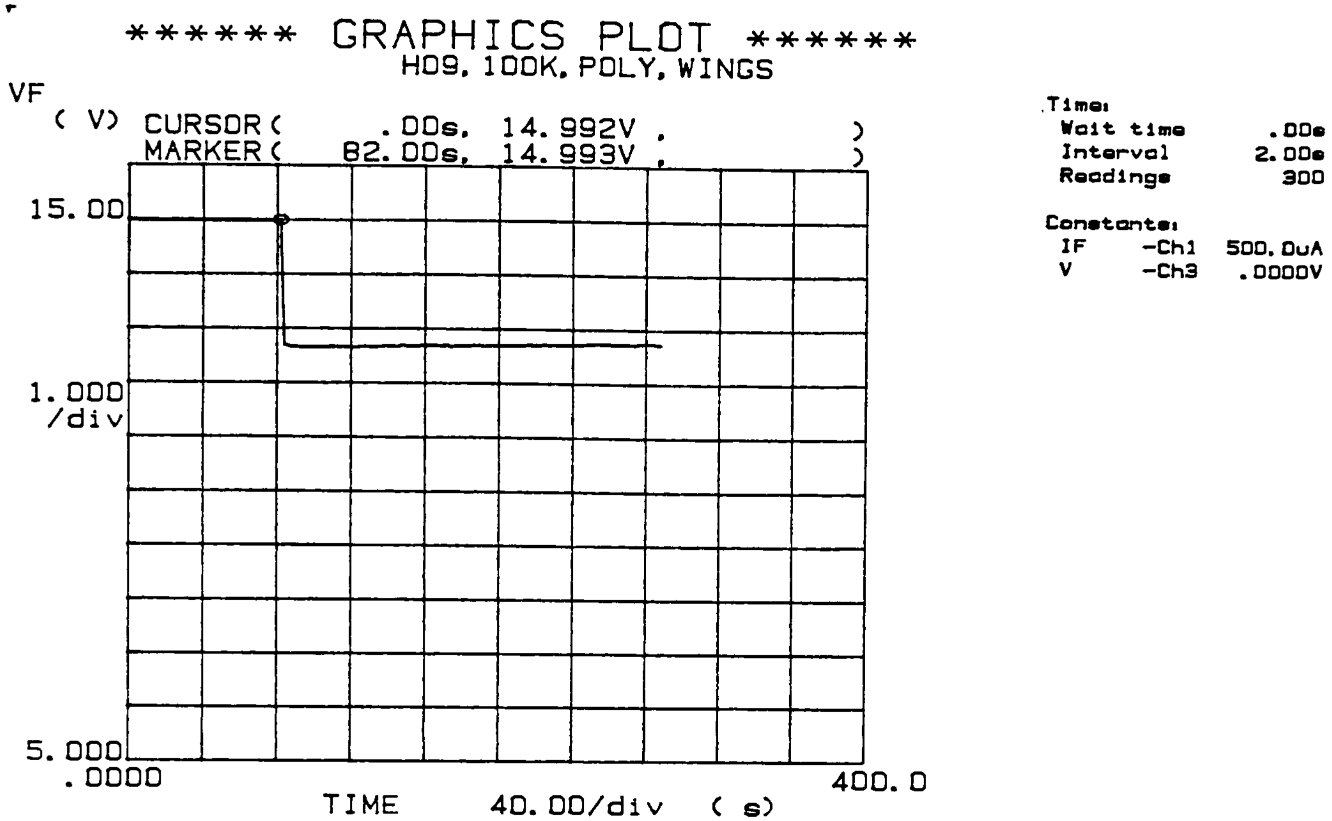
Constants:
IF -Ch1 500.0uA
V -Ch3 .0000V

****** GRAPHICS PLOT ******
B03, 100K, POLY, WING

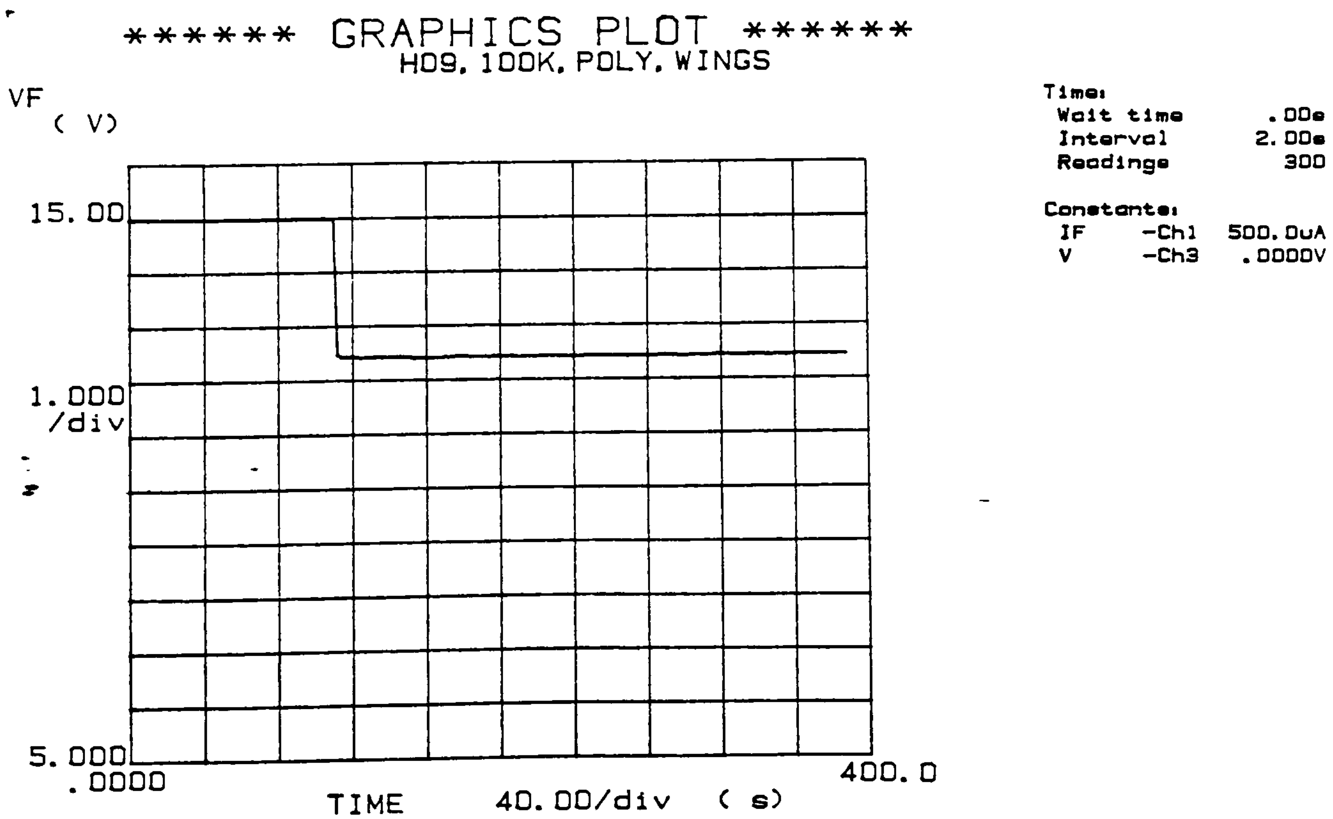


Time:
Wait time .00s
Interval 2.00s
Readings 250

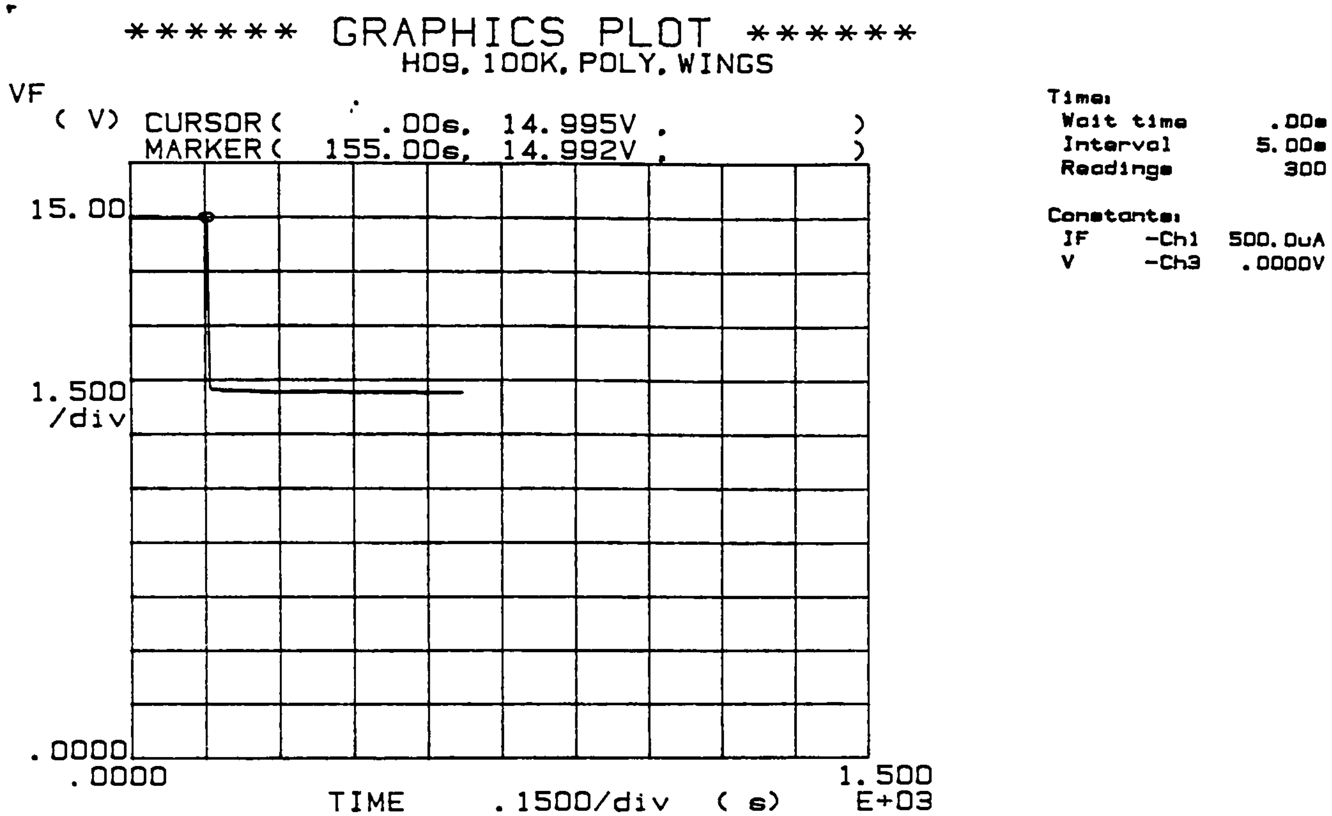
Constants:
IF -Ch1 500.0uA
V -Ch3 .0000V

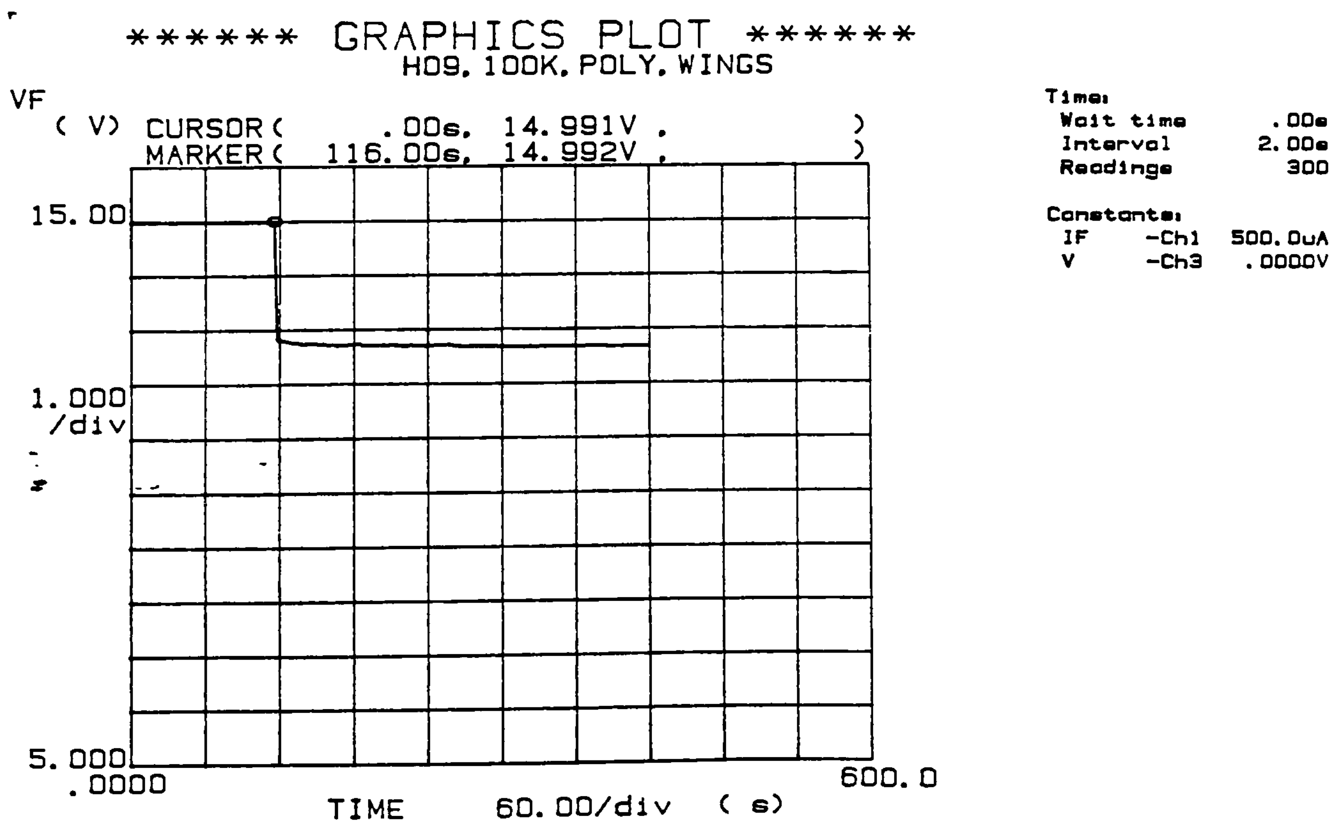


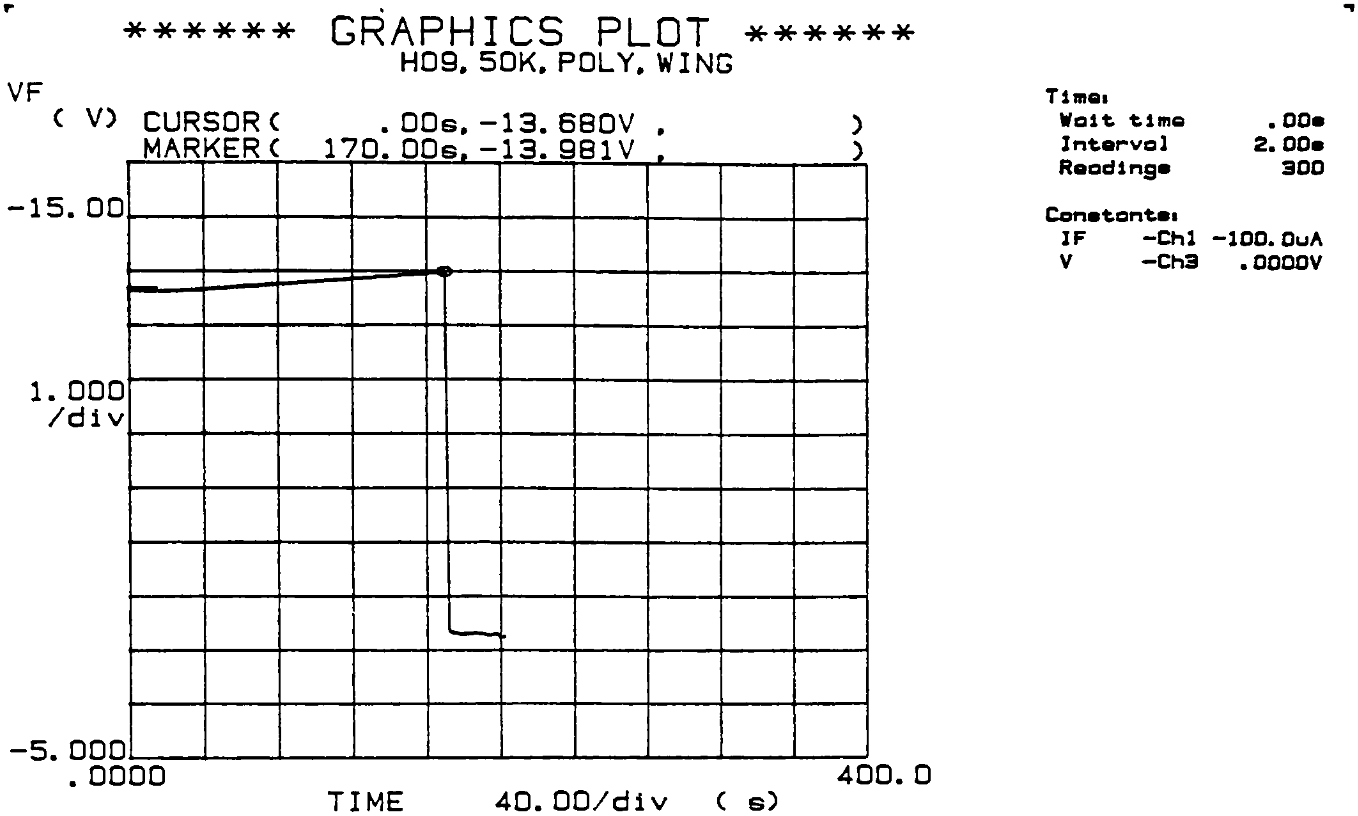
****** GRAPHICS PLOT ******
HD9, 100K, POLY, WINGS
VF
(V)
CURSOR (.00s, 14.992V ,)
MARKER (82.00s, 14.993V ,)
15.00
1.000
/div
5.000
.0000
400.0
TIME 40.00/div (s)
Time:
Wait time .00s
Interval 2.00s
Readings 300
Constants:
IF -Ch1 500.0uA
V -Ch3 .0000V

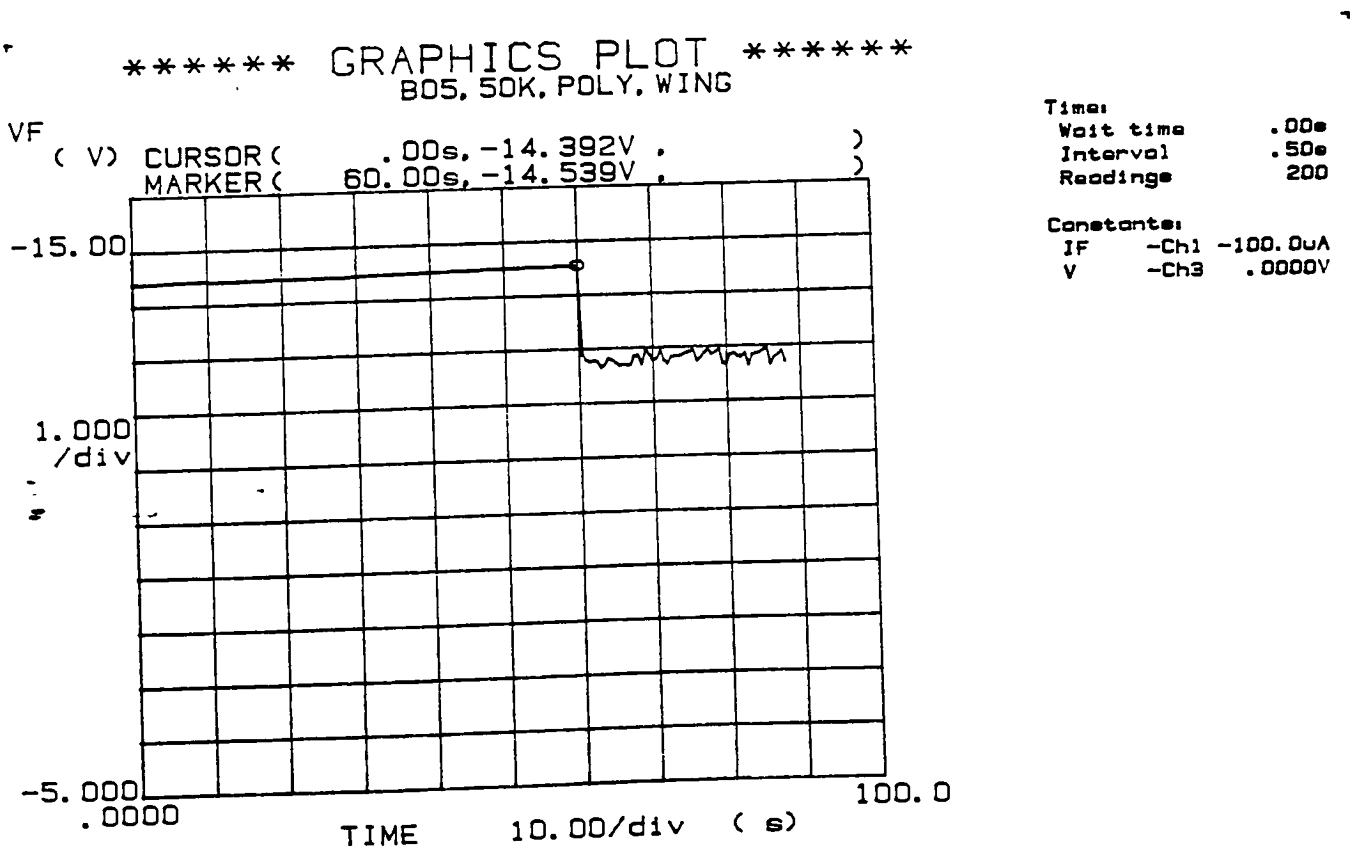


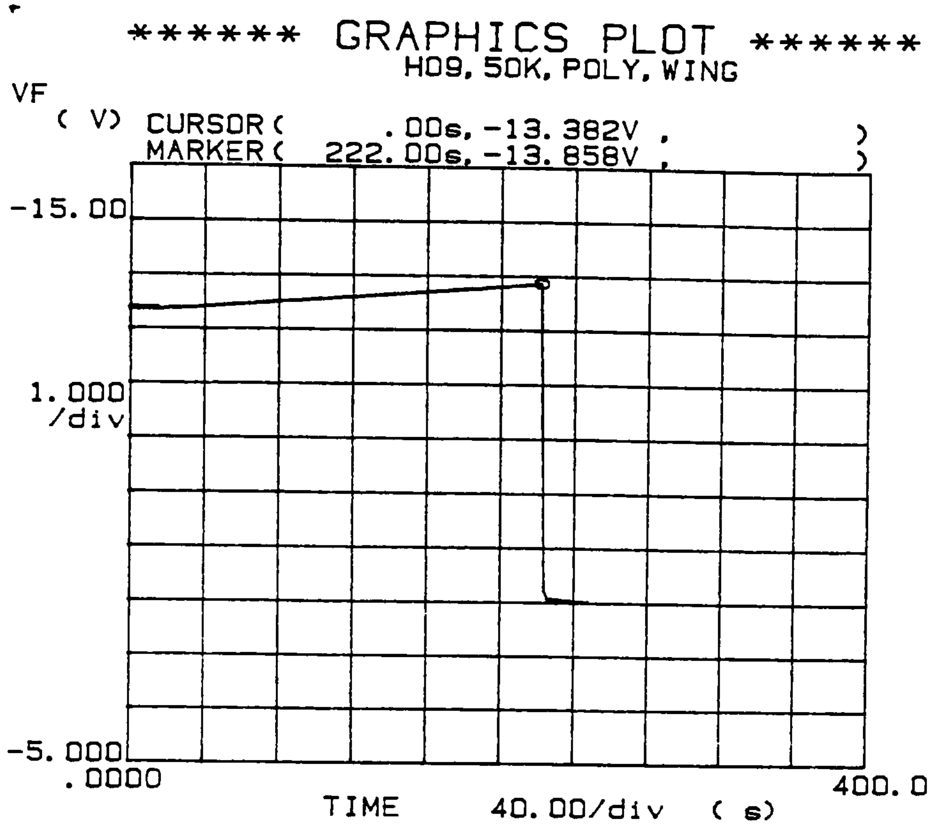
****** GRAPHICS PLOT ******
HD9, 100K, POLY, WINGS
VF
(V)
15.00
1.000
/div
5.000
.0000
400.0
TIME 40.00/div (s)
Time:
Wait time .00s
Interval 2.00s
Readings 300
Constants:
IF -Ch1 500.0uA
V -Ch3 .0000V


****** GRAPHICS PLOT ******
H09, 100K, POLY, WINGS
VF (V)
CURSOR (.00s, 14.995V ,)
MARKER (155.00s, 14.992V ,)
15.00
1.500 /div
.0000
.0000
1.500 E+03
TIME .1500/div (s)
Time:
Wait time .00s
Interval 5.00s
Readings 300
Constants:
IF -Ch1 500.0uA
V -Ch3 .0000V


****** GRAPHICS PLOT ******
H09, 100K, POLY, WINGS
VF (V)
CURSOR (.00s, 14.991V ,)
MARKER (116.00s, 14.992V ,)
15.00
1.000 /div
5.000
.0000
600.0
TIME 60.00/div (s)
Time:
Wait time .00s
Interval 2.00s
Readings 300
Constants:
IF -Ch1 500.0uA
V -Ch3 .0000V

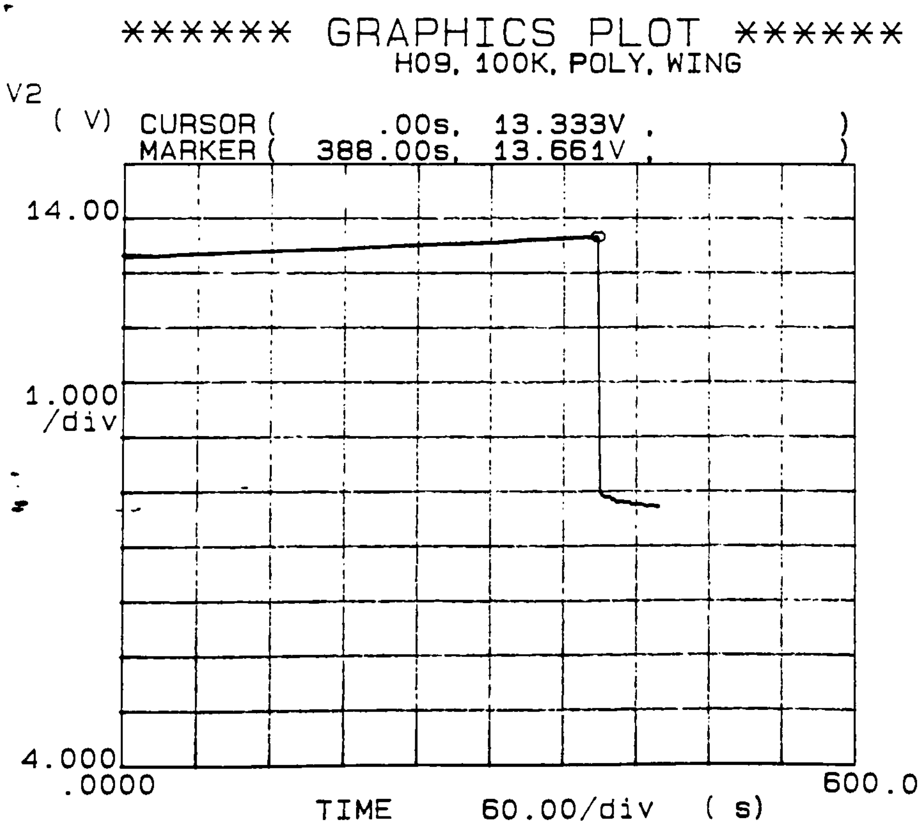

****** GRAPHICS PLOT ******
H09, 50K, POLY, WING
VF
(V) CURSOR (.00s, -13.680V ,)
MARKER (170.00s, -13.981V ,)
-15.00
1.000
/div
-5.000
.0000
400.0
TIME 40.00/div (s)
Time:
Wait time .00s
Interval 2.00s
Readings 300
Constants:
IF -Ch1 -100.0uA
V -Ch3 .0000V


****** GRAPHICS PLOT ******
B05, 50K, POLY, WING
VF
(V) CURSOR (.00s, -14.392V ,)
MARKER (60.00s, -14.539V ,)
-15.00
1.000
/div
-5.000
.0000
100.0
TIME 10.00/div (s)
Time:
Wait time .00s
Interval .50s
Readings 200
Constants:
IF -Ch1 -100.0uA
V -Ch3 .0000V



Time:
Wait time .00s
Interval 2.00s
Readings 300

Constants:
IF -Ch1 -100.0uA
V -Ch3 .0000V

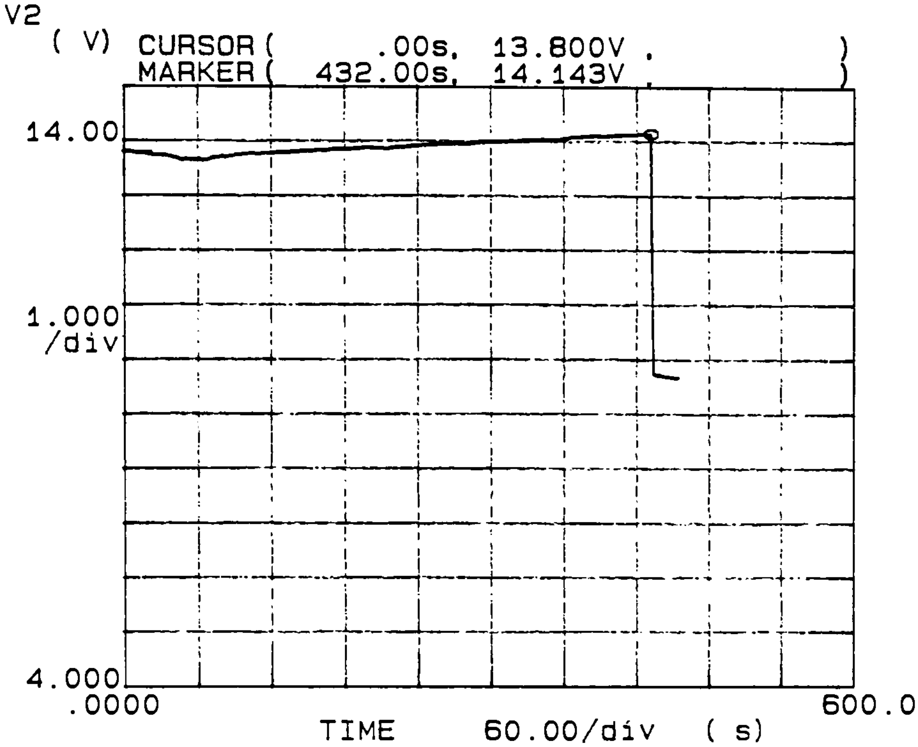


Time:
Wait time .00s
Interval 2.00s
Readings 300

Constants:
V1 -Ch1 .0000V
I2 -Ch2 100.0uA

****** GRAPHICS PLOT ******

H09, 100K, POLY, WING



Time:

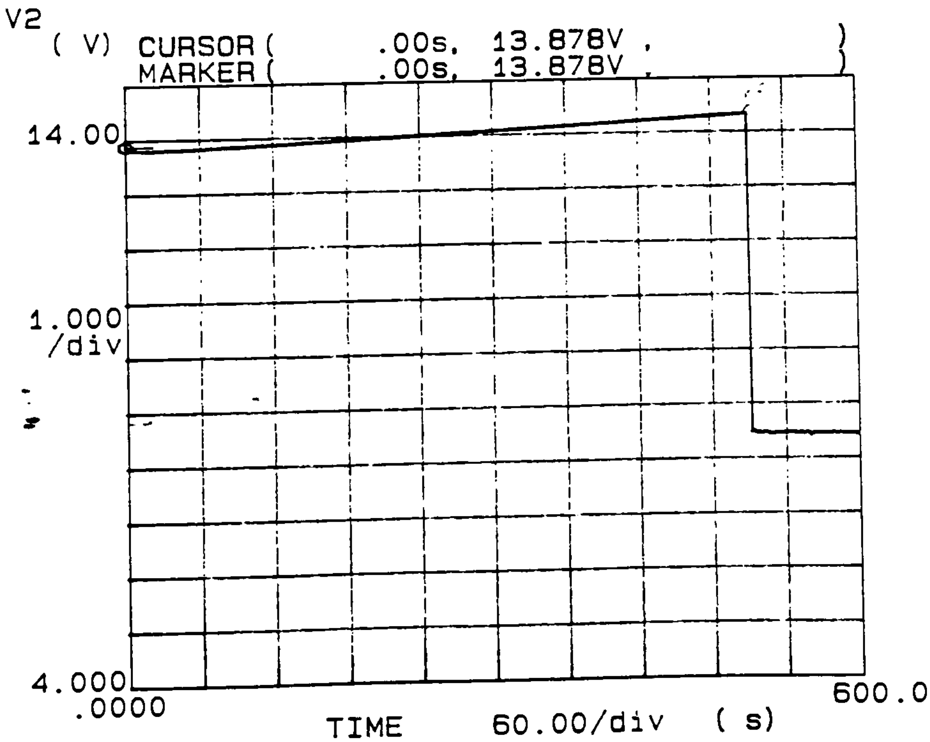
Wait time	.00s
Interval	2.00s
Readings	300

Constants:

V1	-Ch1	.0000V
I2	-Ch2	100.0uA

****** GRAPHICS PLOT ******

H09, 100K, POLY, WING



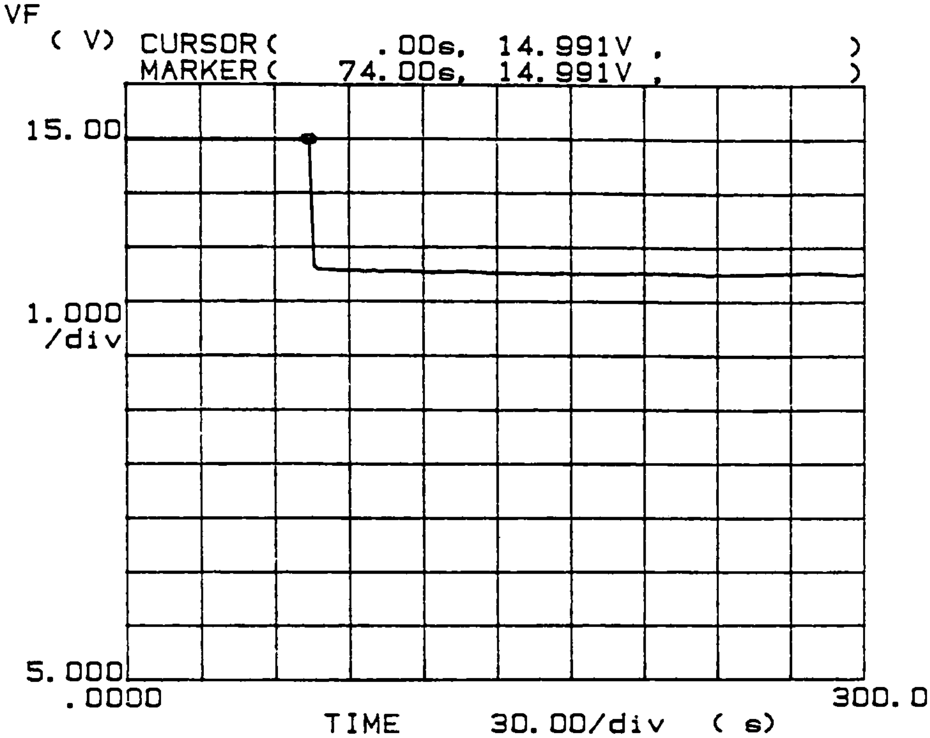
Time:

Wait time	.00s
Interval	2.00s
Readings	300

Constants:

V1	-Ch1	.0000V
I2	-Ch2	100.0uA

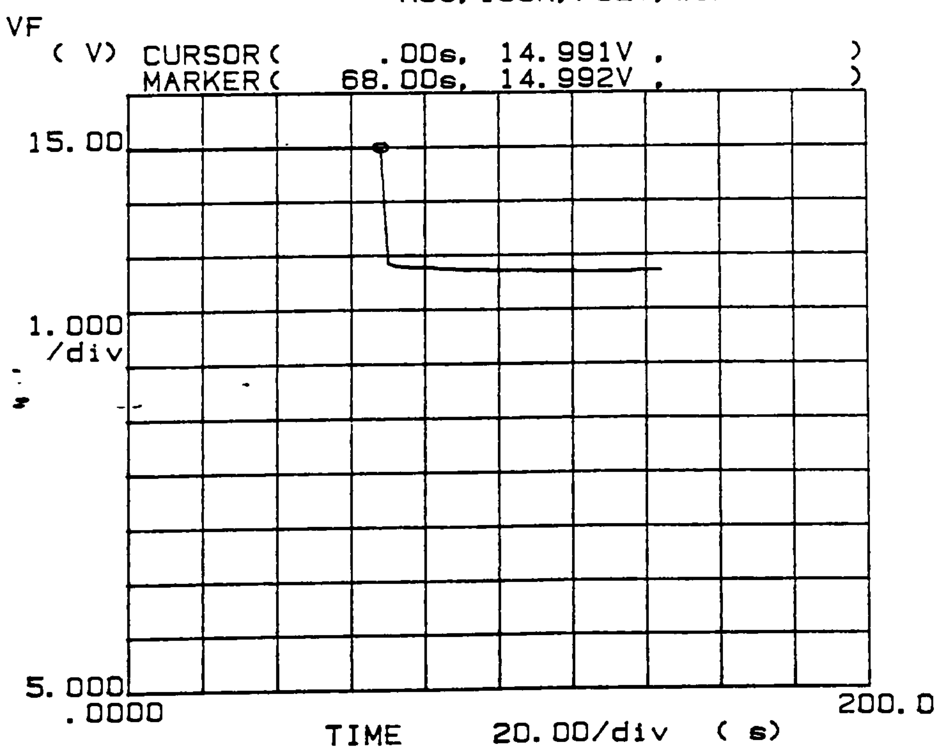
****** GRAPHICS PLOT ******
H09, 100K, POLY, WINGS



Time:
Wait time .00s
Interval 2.00s
Readings 300

Constants:
IF -Ch1 500.0uA
V -Ch3 .0000V

****** GRAPHICS PLOT ******
H09, 100K, POLY, WINGS

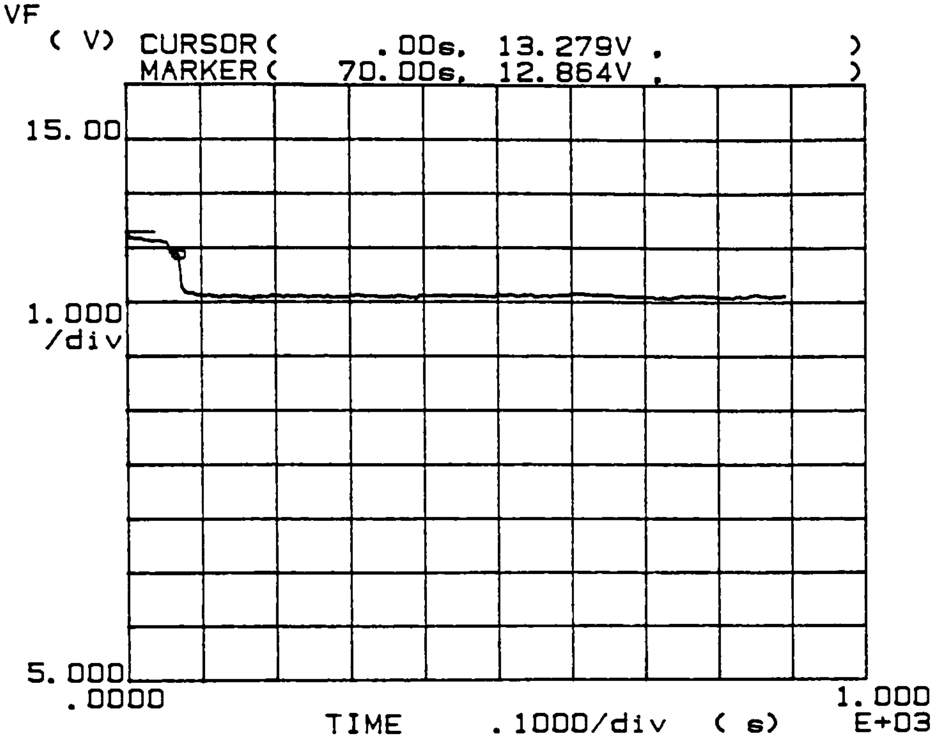


Time:
Wait time .00s
Interval 2.00s
Readings 300

Constants:
IF -Ch1 500.0uA
V -Ch3 .0000V

****** GRAPHICS PLOT ******

HD9, 100K, POLY, WINGS

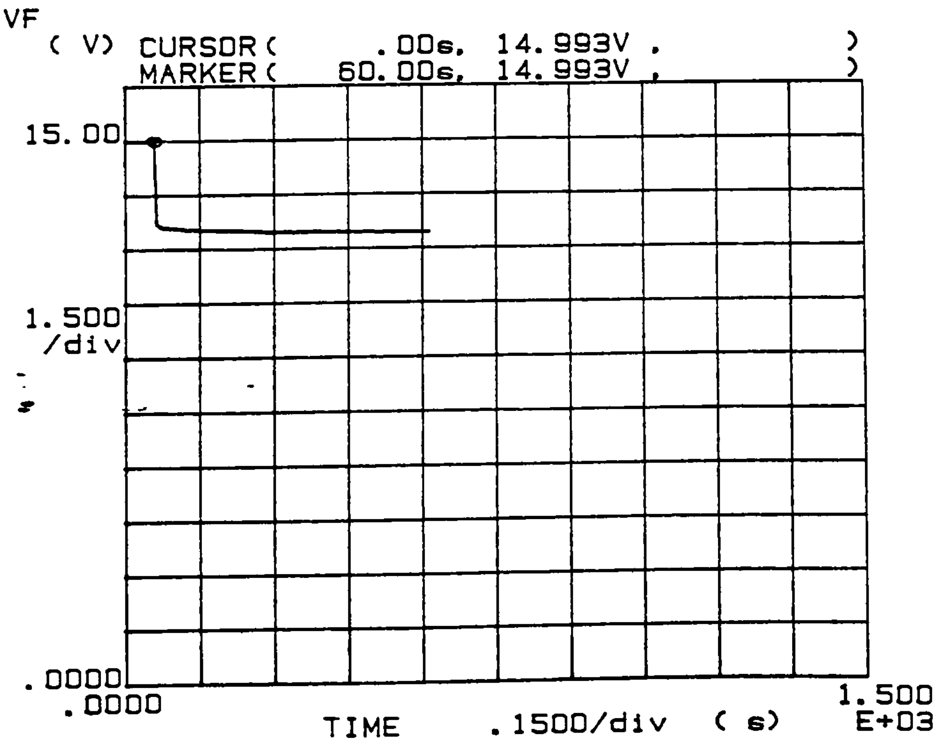


Time:
Wait time .00s
Interval 5.00s
Readings 200

Constants:
IF -Ch1 500.0uA
V -Ch3 .0000V

****** GRAPHICS PLOT ******

HD9, 100K, POLY, WINGS

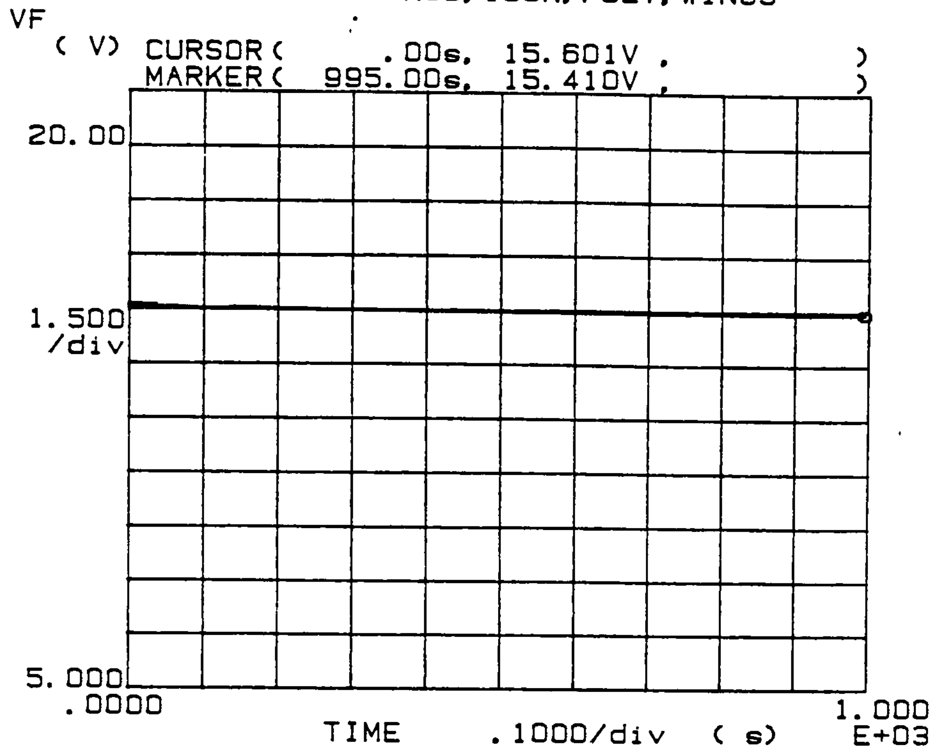


Time:
Wait time .00s
Interval 5.00s
Readings 300

Constants:
IF -Ch1 500.0uA
V -Ch3 .0000V

****** GRAPHICS PLOT ******

H09, 100K, POLY, WINGS



15,36V

Time:

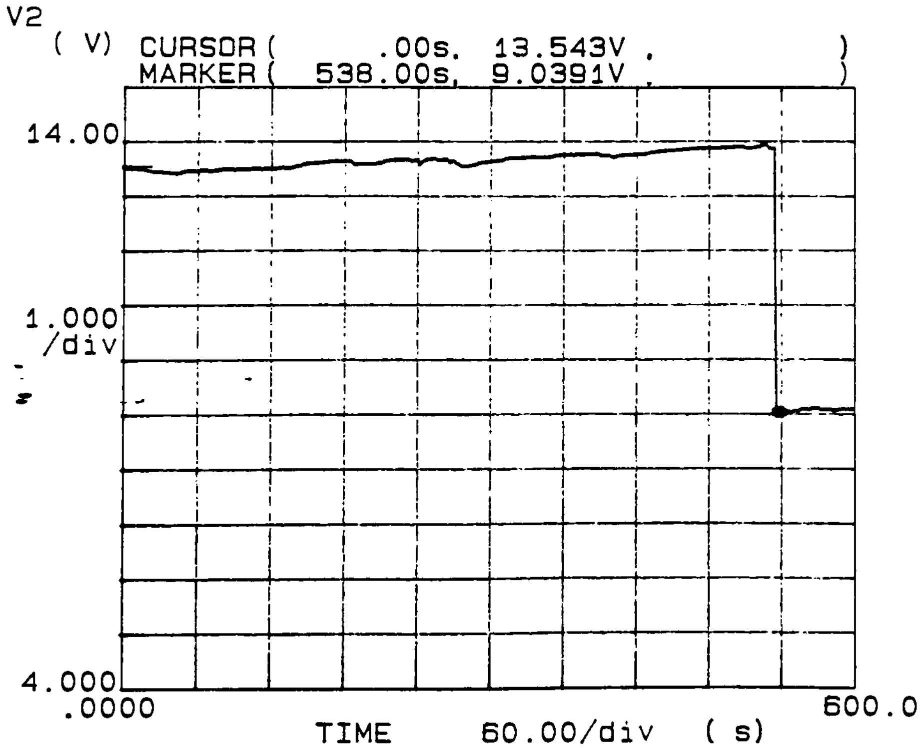
Wait time	.00s
Interval	5.00s
Readings	200

Constants:

IF	-Ch1	1.000mA
V	-Ch3	.0000V

****** GRAPHICS PLOT ******

H09, 100K, POLY, WING

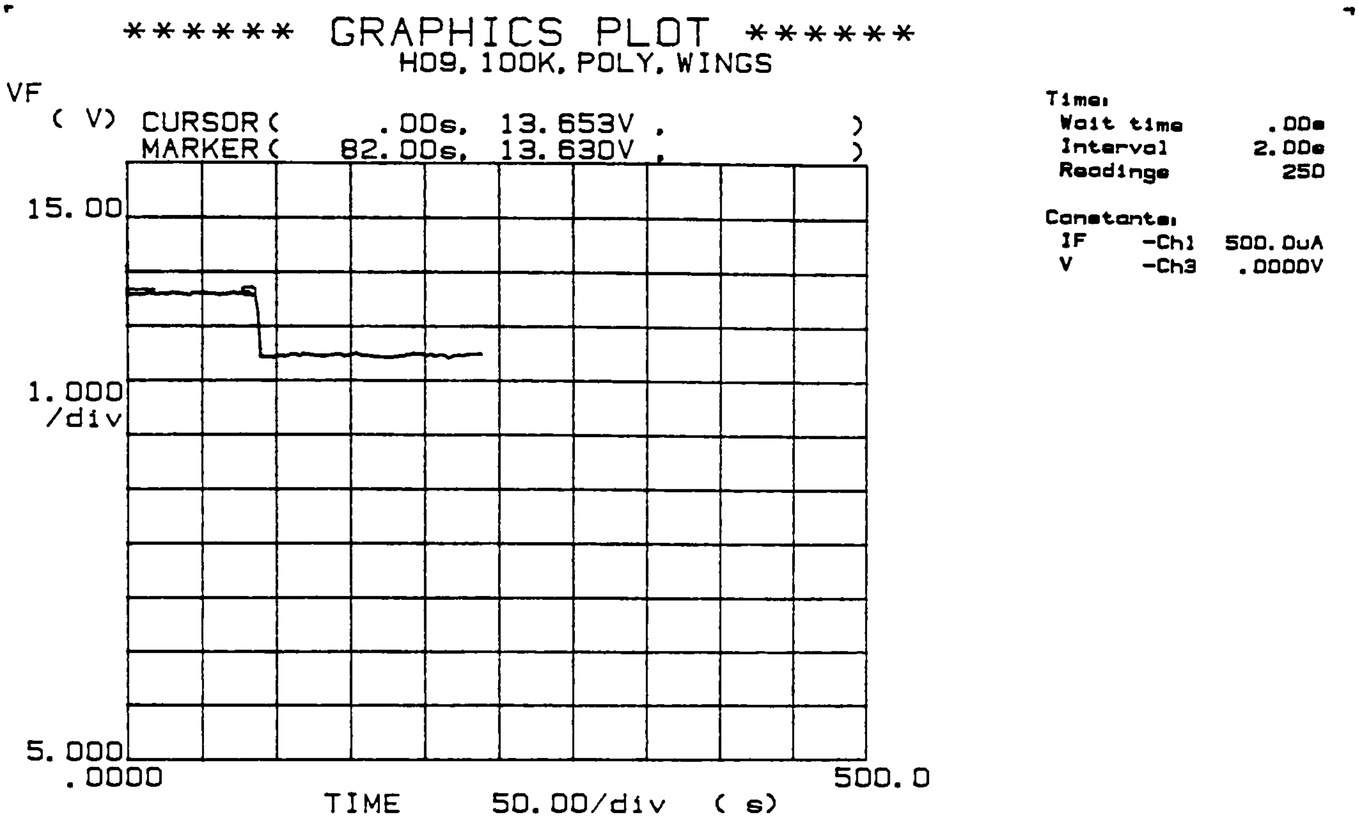


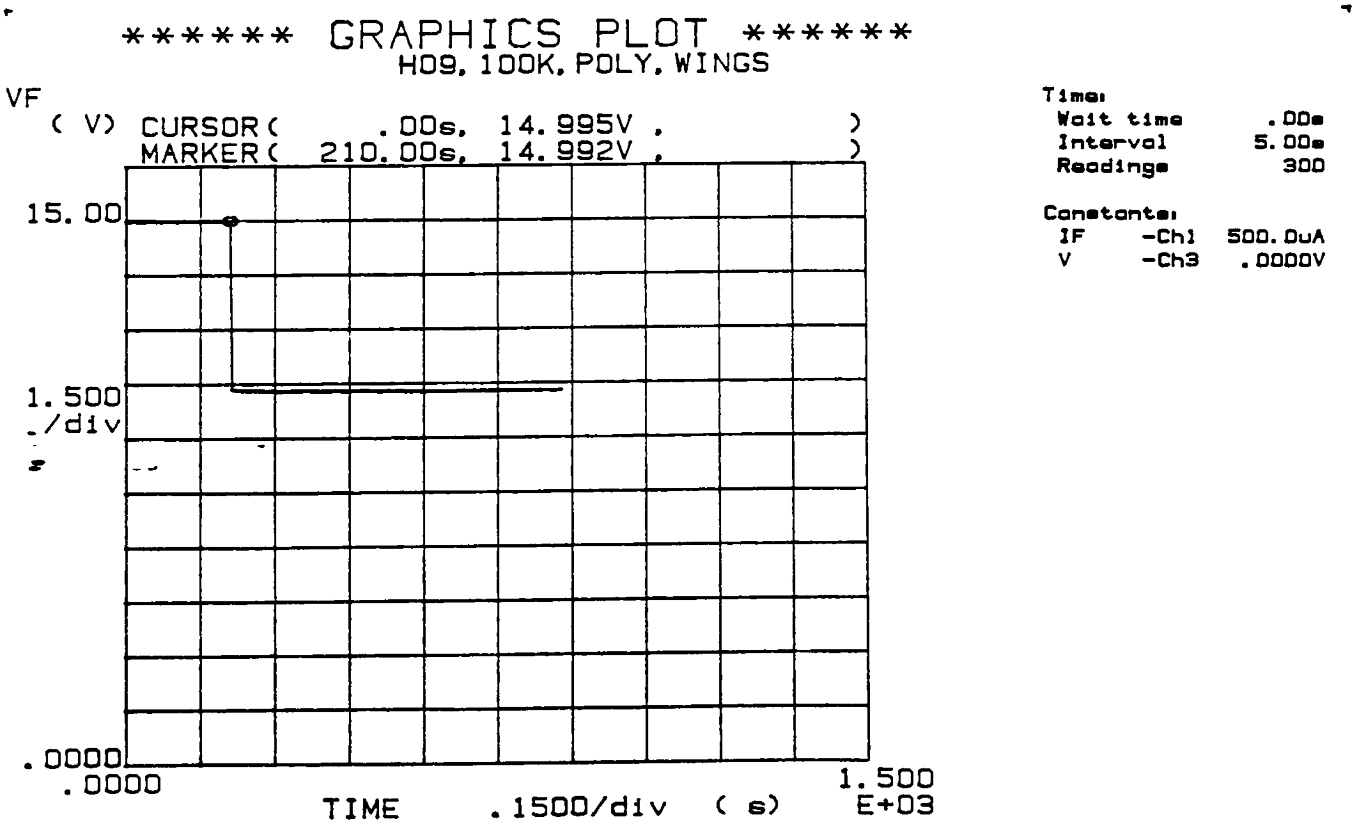
Time:

Wait time	.00s
Interval	2.00s
Readings	300

Constants:

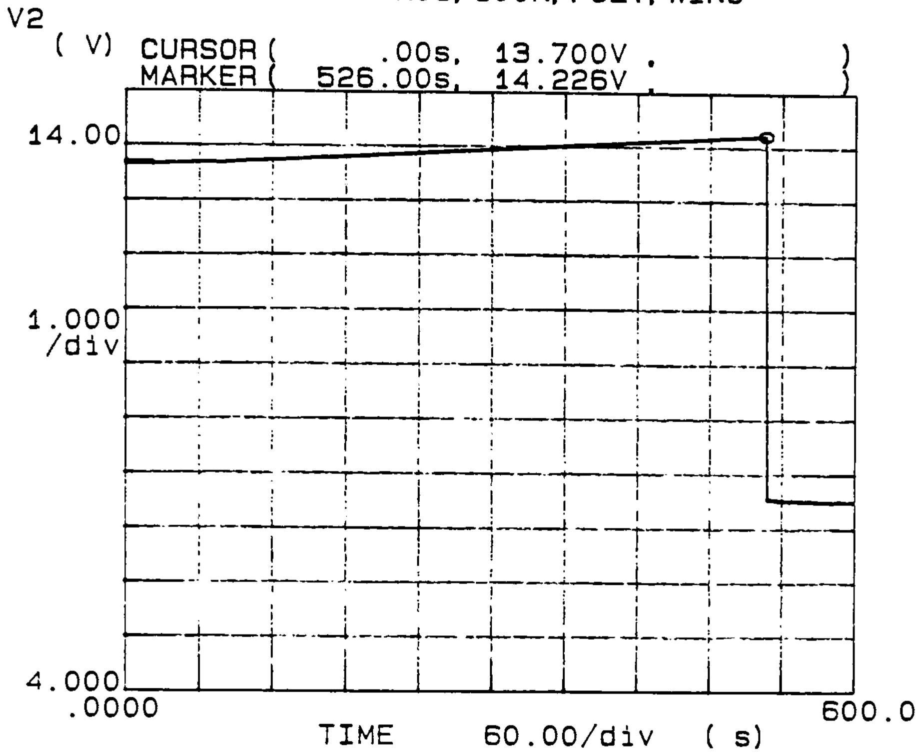
V1	-Ch1	.0000V
I2	-Ch2	100.0uA


****** GRAPHICS PLOT ******
H09, 100K, POLY, WINGS
VF
(V) CURSOR (.00s, 13.653V ,)
MARKER (82.00s, 13.630V ,)
15.00
1.000
/div
5.000
.0000
500.0
TIME 50.00/div (s)
Time:
Wait time .00s
Interval 2.00s
Readings 250
Constants:
IF -Ch1 500.0uA
V -Ch3 .0000V


****** GRAPHICS PLOT ******
H09, 100K, POLY, WINGS
VF
(V) CURSOR (.00s, 14.995V ,)
MARKER (210.00s, 14.992V ,)
15.00
1.500
/div
.0000
.0000
1.500
E+03
TIME .1500/div (s)
Time:
Wait time .00s
Interval 5.00s
Readings 300
Constants:
IF -Ch1 500.0uA
V -Ch3 .0000V

****** GRAPHICS PLOT ******

H09, 100K, POLY, WING

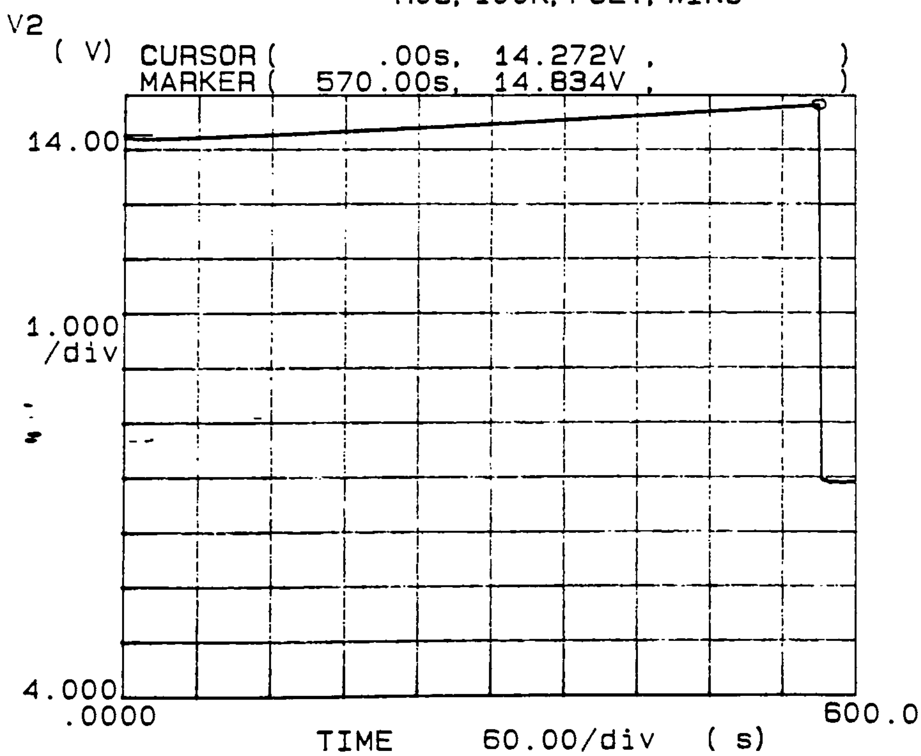


Time:
Wait time .00s
Interval 2.00s
Readings 300

Constants:
V1 -Ch1 .0000V
I2 -Ch2 100.0uA

****** GRAPHICS PLOT ******

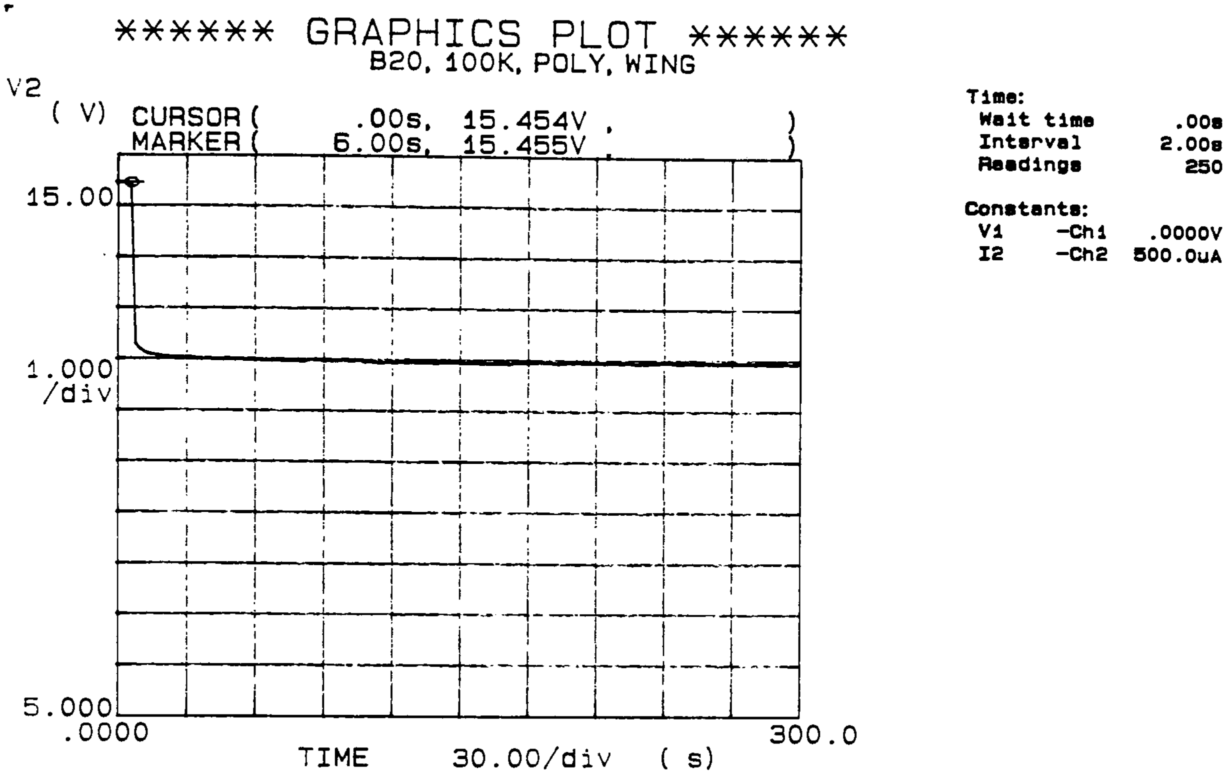
H09, 100K, POLY, WING

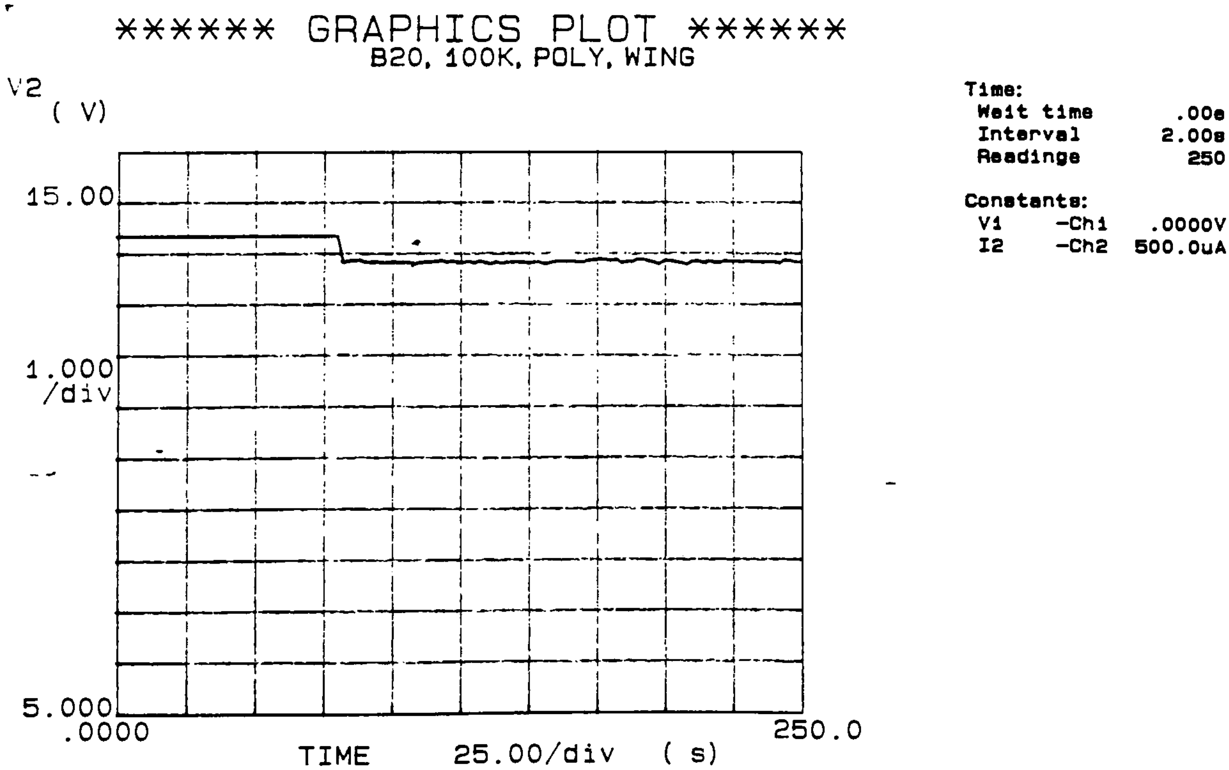


Time:
Wait time .00s
Interval 2.00s
Readings 300

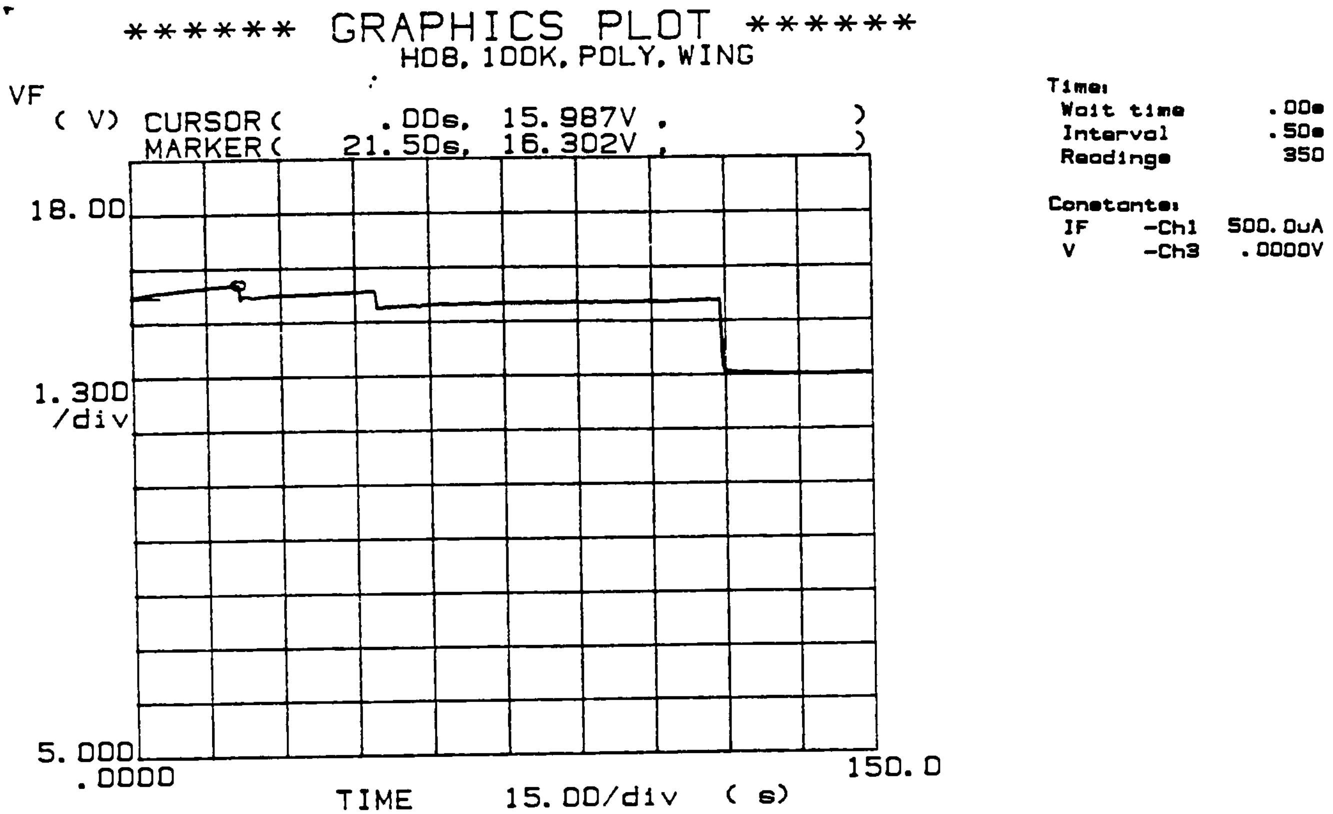
Constants:
V1 -Ch1 .0000V
I2 -Ch2 100.0uA

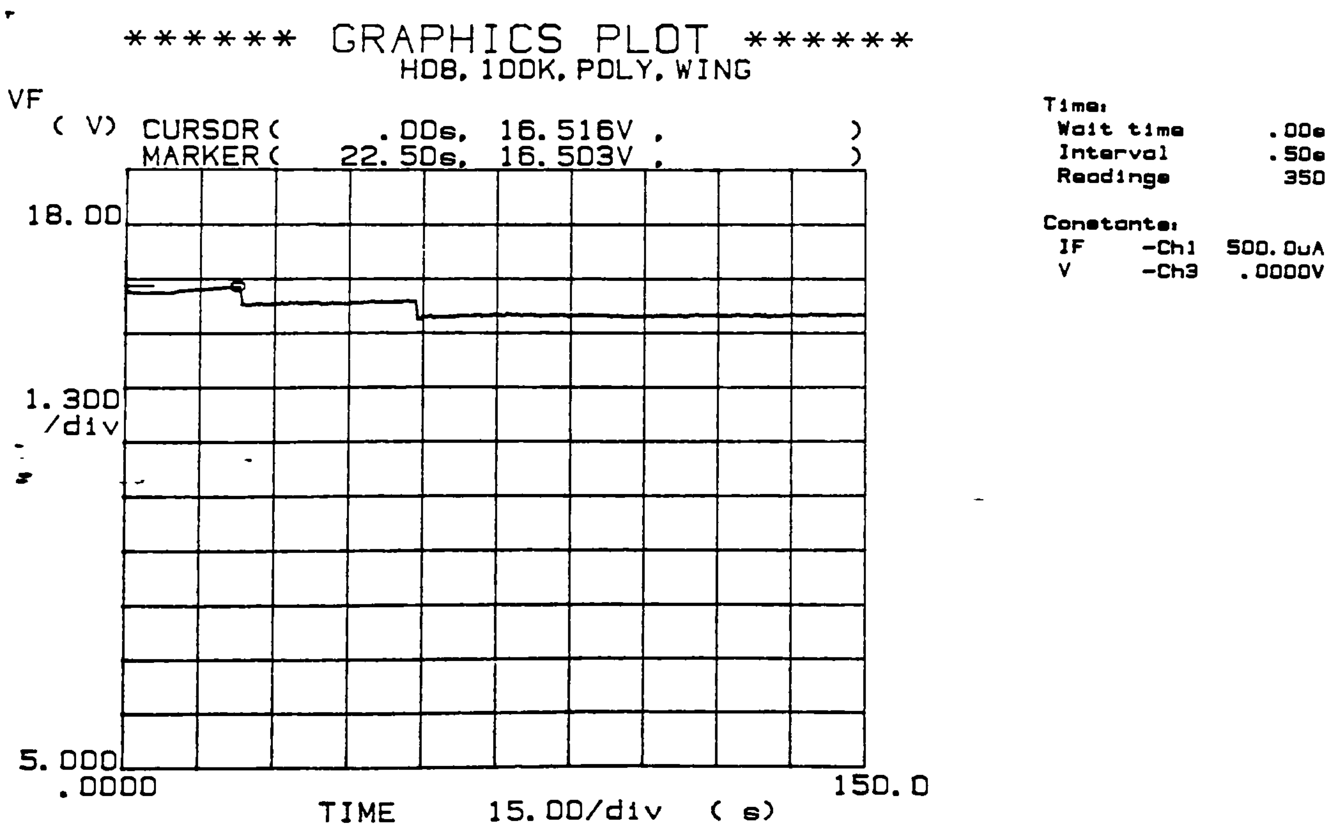
3500 Å Etch Back Results

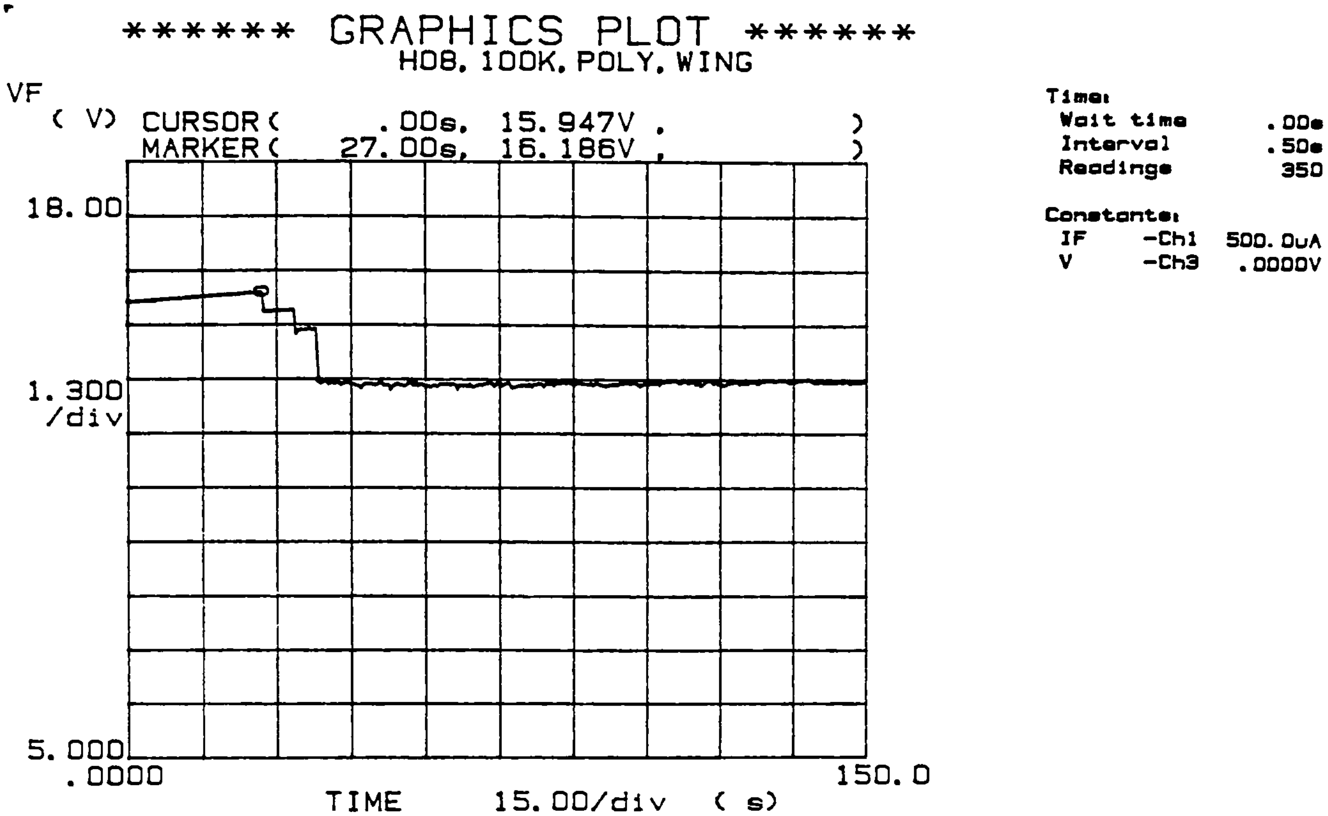

****** GRAPHICS PLOT ******
B20, 100K, POLY, WING
V2
(V)
CURSOR (.00s, 15.454V ,)
MARKER (6.00s, 15.455V ,)
15.00
1.000
/div
5.000
.0000
300.0
TIME 30.00/div (s)
Time:
Wait time .00s
Interval 2.00s
Readings 250
Constants:
V1 -Ch1 .0000V
I2 -Ch2 500.0uA


****** GRAPHICS PLOT ******
B20, 100K, POLY, WING
V2
(V)
15.00
1.000
/div
5.000
.0000
250.0
TIME 25.00/div (s)
Time:
Wait time .00s
Interval 2.00s
Readings 250
Constants:
V1 -Ch1 .0000V
I2 -Ch2 500.0uA

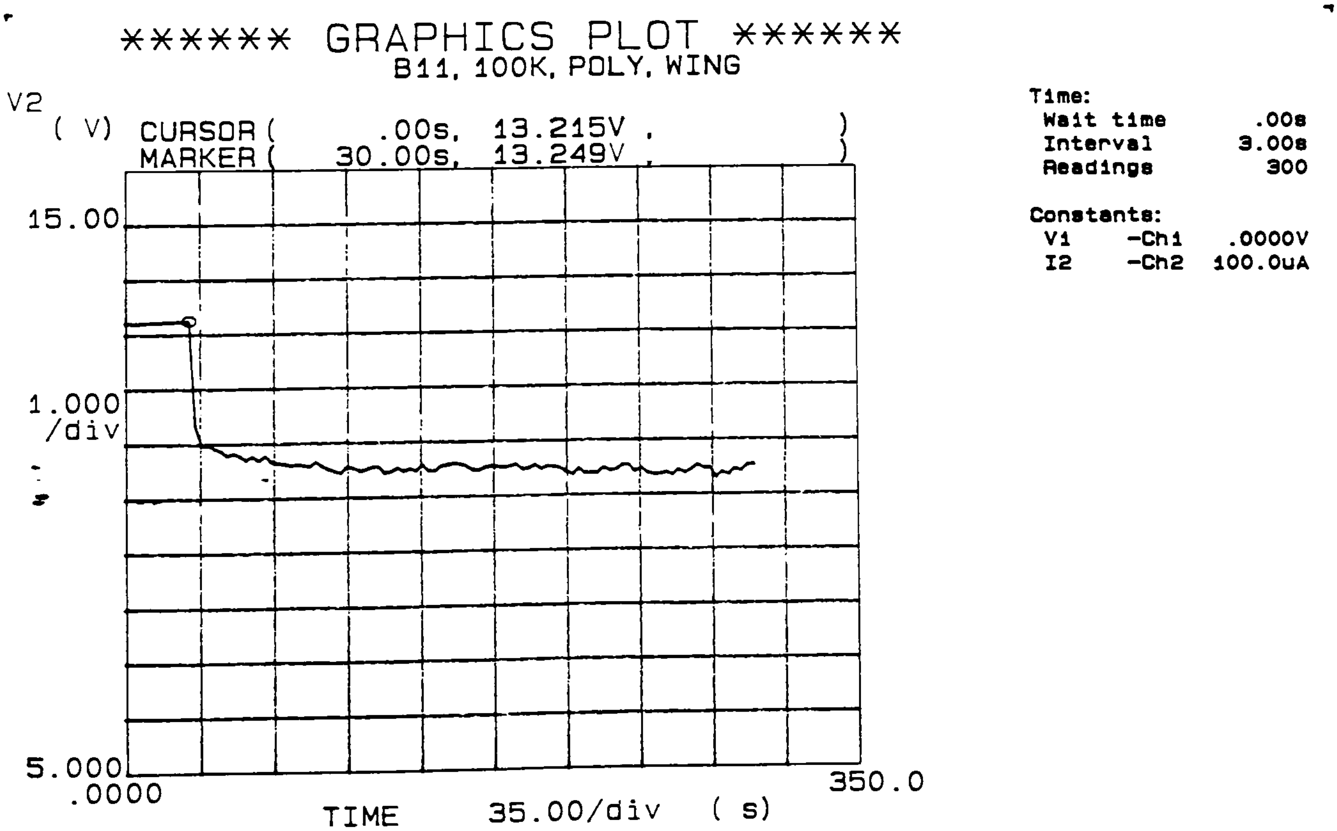
4500 Å Etch Back Results


****** GRAPHICS PLOT ******
HD8, 100K, POLY, WING
VF
(V) CURSOR (.00s, 15.987V ,)
MARKER (21.50s, 16.302V ,)
18.00
1.300
/div
5.000
.0000
150.0
TIME 15.00/div (s)
Time:
Wait time .00s
Interval .50s
Readings 350
Constants:
IF -Ch1 500.0uA
V -Ch3 .0000V


****** GRAPHICS PLOT ******
HD8, 100K, POLY, WING
VF
(V) CURSOR (.00s, 16.516V ,)
MARKER (22.50s, 16.503V ,)
18.00
1.300
/div
5.000
.0000
150.0
TIME 15.00/div (s)
Time:
Wait time .00s
Interval .50s
Readings 350
Constants:
IF -Ch1 500.0uA
V -Ch3 .0000V



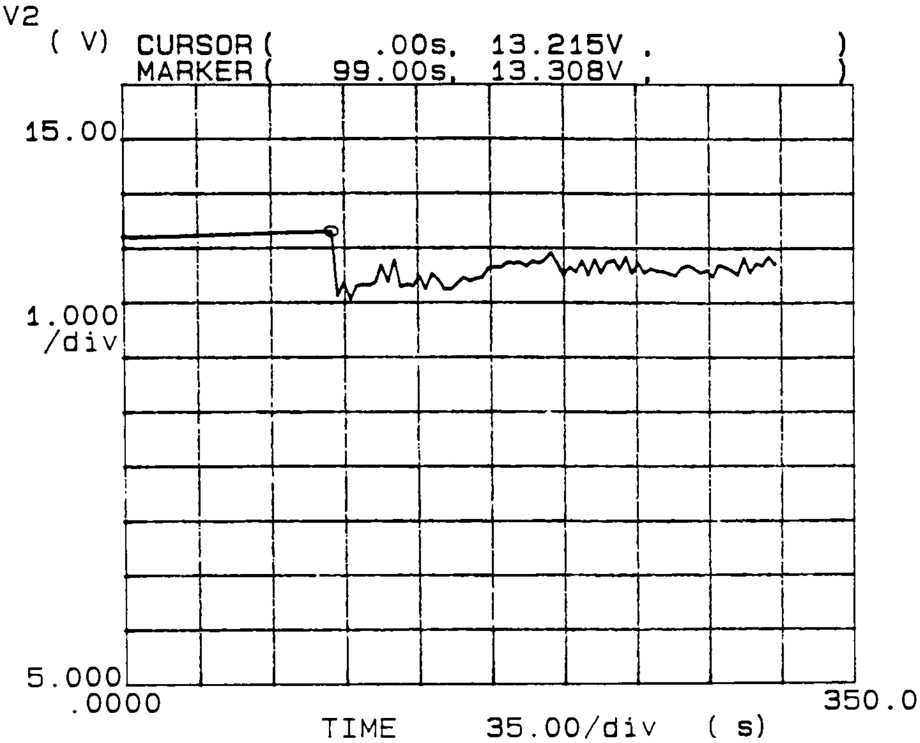
****** GRAPHICS PLOT ******
H08, 100K, POLY, WING
VF
(V) CURSOR (.00s, 15.947V ,)
MARKER (27.00s, 16.186V ,)
18.00
1.300
/div
5.000
.0000
150.0
TIME 15.00/div (s)
Time:
Wait time .00s
Interval .50s
Readings 350
Constants:
IF -Ch1 500.0uA
V -Ch3 .0000V



****** GRAPHICS PLOT ******
B11, 100K, POLY, WING
V2
(V) CURSOR (.00s, 13.215V ,)
MARKER (30.00s, 13.249V ,)
15.00
1.000
/div
5.000
.0000
350.0
TIME 35.00/div (s)
Time:
Wait time .00s
Interval 3.00s
Readings 300
Constants:
V1 -Ch1 .0000V
I2 -Ch2 100.0uA

****** GRAPHICS PLOT ******

B11, 100K, POLY, WING

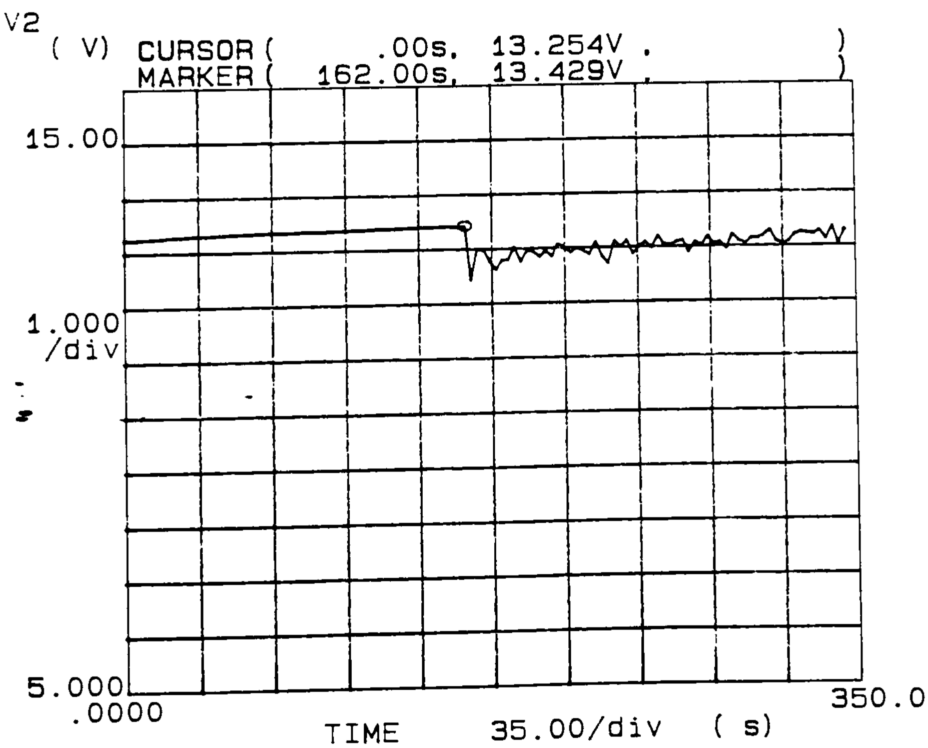


Time:
Wait time .00s
Interval 3.00s
Readings 300

Constants:
V1 -Ch1 .0000V
I2 -Ch2 100.0uA

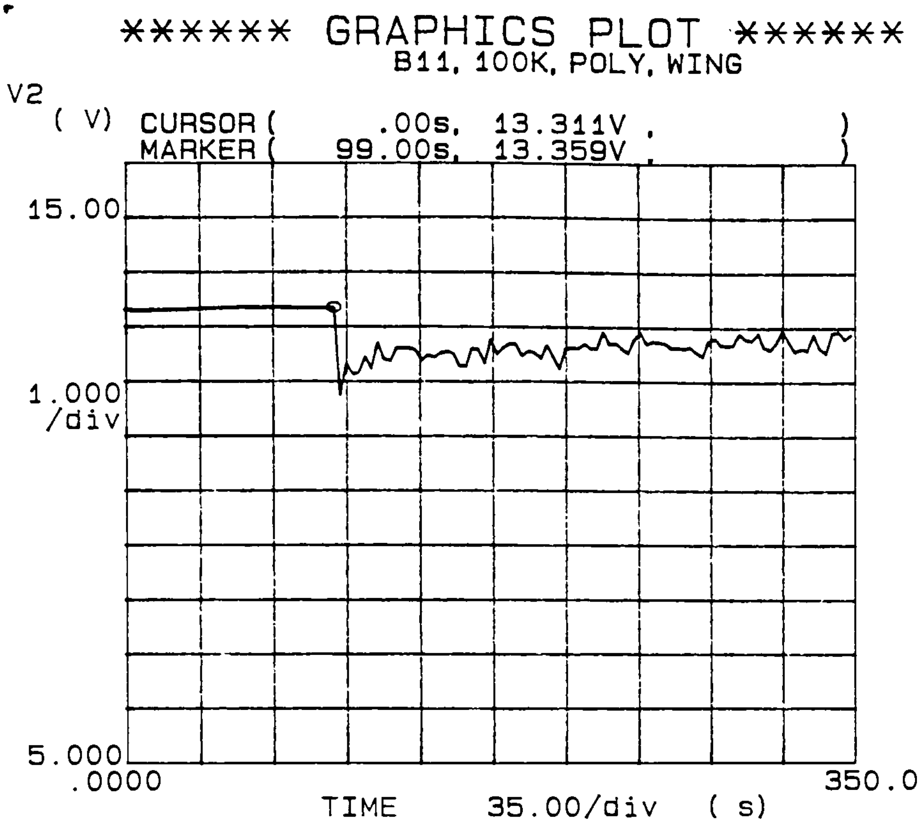
****** GRAPHICS PLOT ******

B11, 100K, POLY, WING



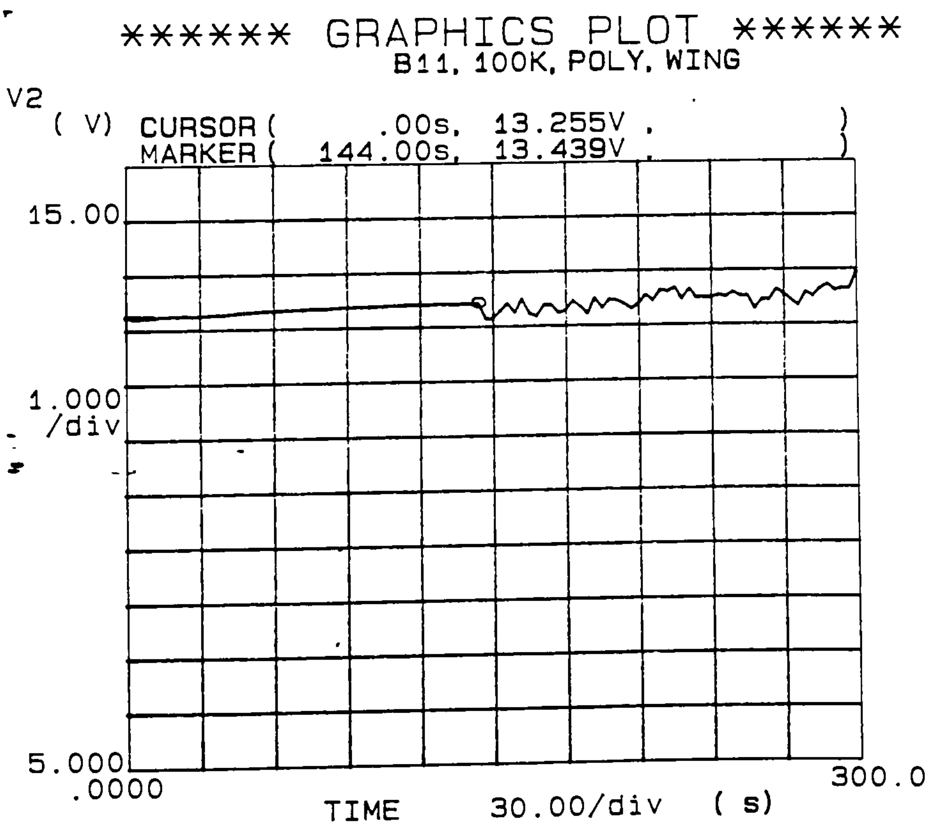
Time:
Wait time .00s
Interval 3.00s
Readings 300

Constants:
V1 -Ch1 .0000V
I2 -Ch2 100.0uA



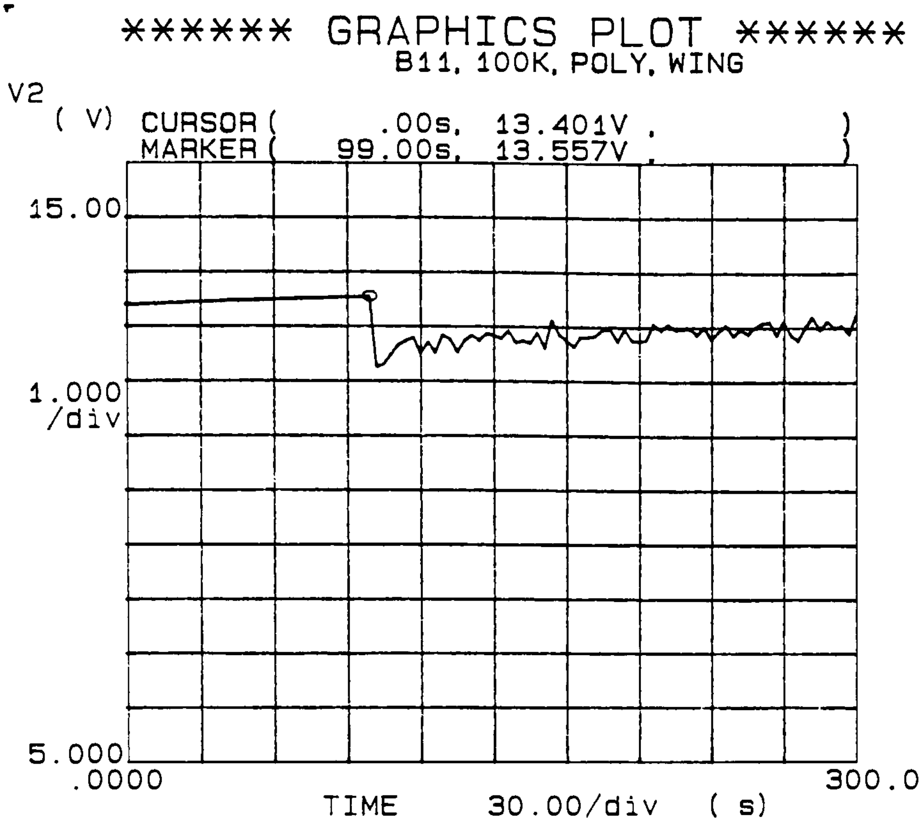
Time:
Wait time .00s
Interval 3.00s
Readings 300

Constants:
V1 -Ch1 .0000V
I2 -Ch2 100.0uA



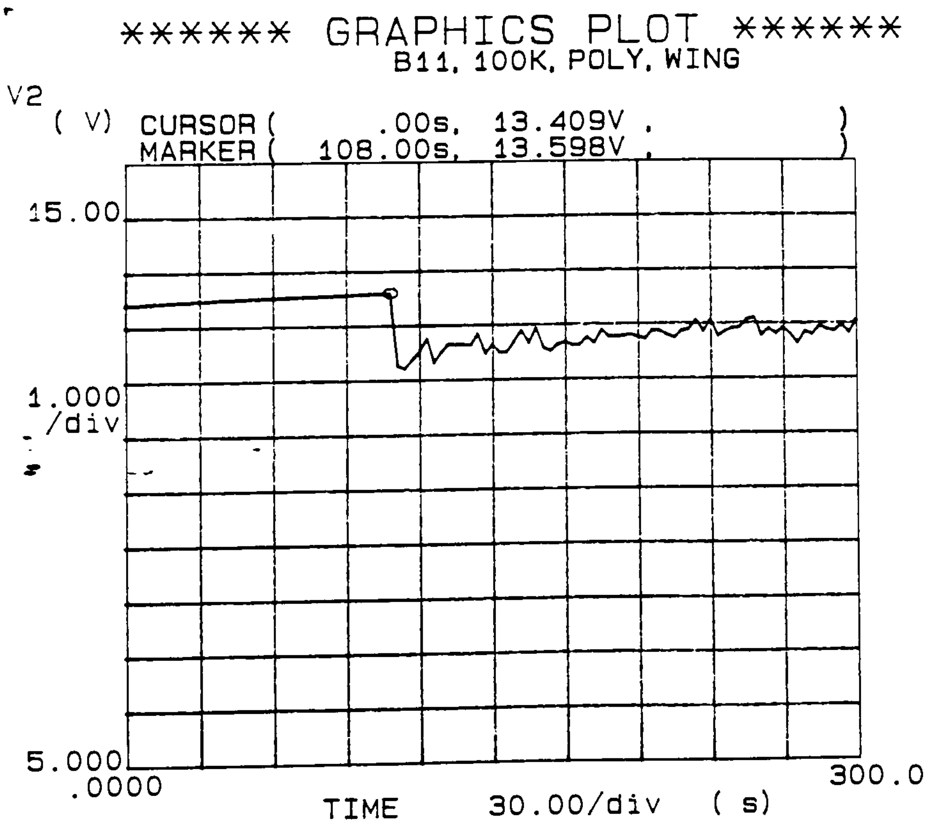
Time:
Wait time .00s
Interval 3.00s
Readings 300

Constants:
V1 -Ch1 .0000V
I2 -Ch2 100.0uA



Time:
Wait time .00s
Interval 3.00s
Readings 300

Constants:
V1 -Ch1 .0000V
I2 -Ch2 100.0uA



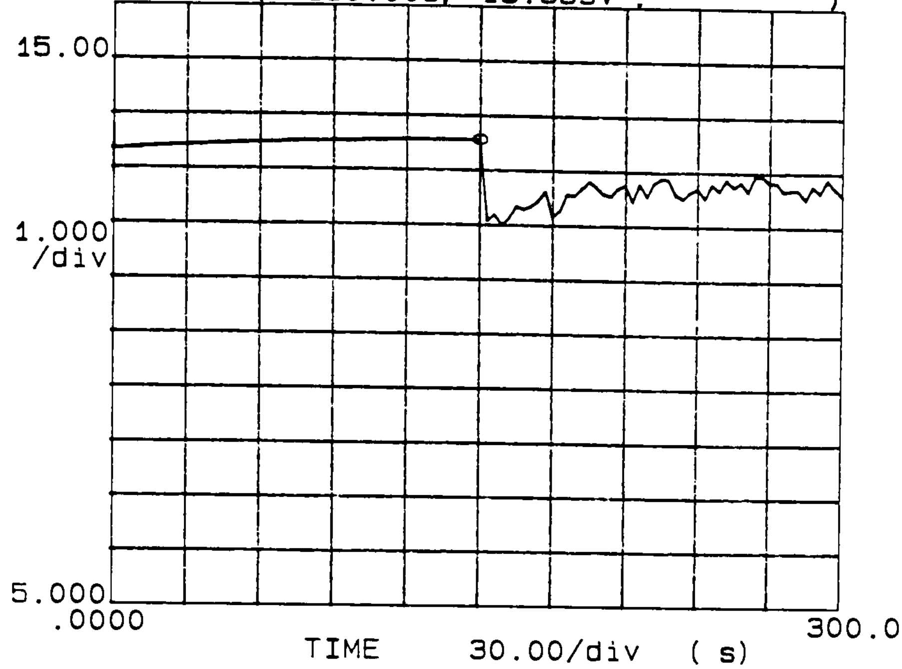
Time:
Wait time .00s
Interval 3.00s
Readings 300

Constants:
V1 -Ch1 .0000V
I2 -Ch2 100.0uA

****** GRAPHICS PLOT ******

B11, 100K, POLY, WING

V2 (V) CURSOR (.00s, 13.348V ,)
MARKER (150.00s, 13.559V ,)



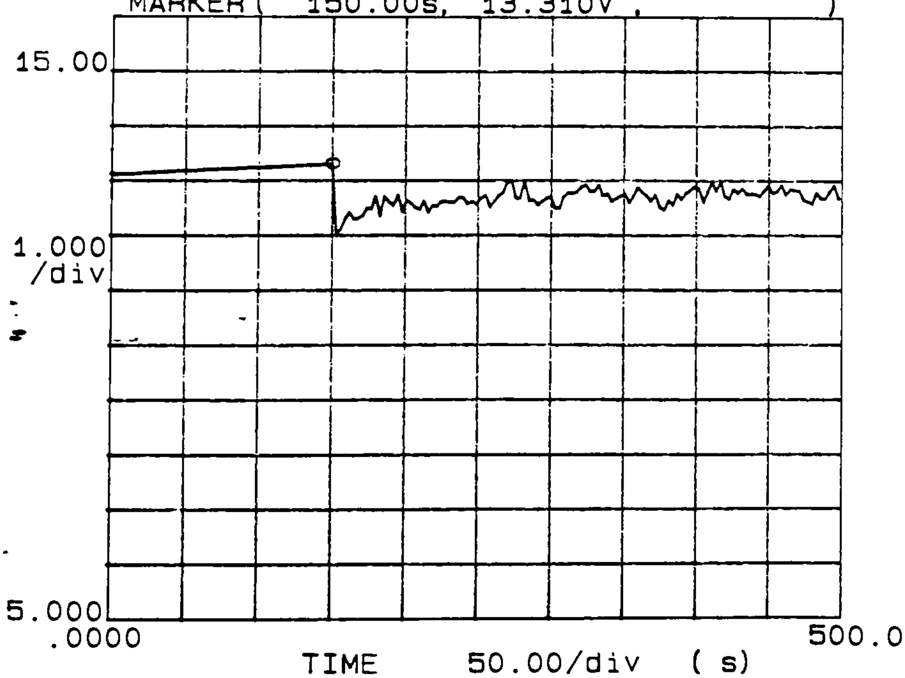
Time:
Wait time .00s
Interval 3.00s
Readings 300

Constants:
V1 -Ch1 .0000V
I2 -Ch2 100.0uA

****** GRAPHICS PLOT ******

B11, 100K, POLY, WING

V2 (V) CURSOR (.00s, 13.128V ,)
MARKER (150.00s, 13.310V ,)

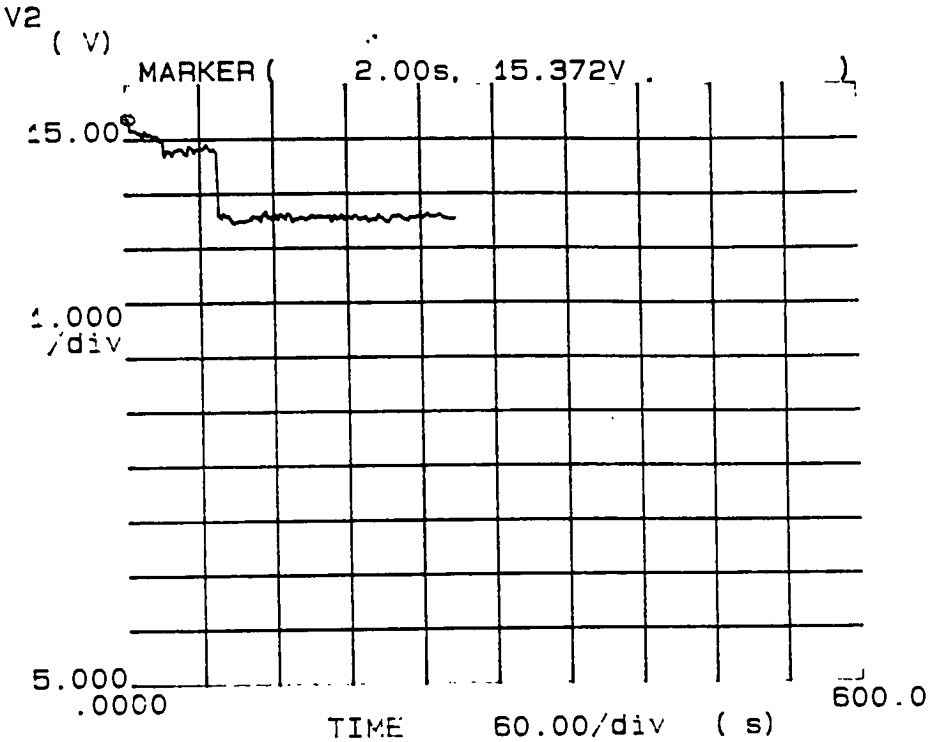


Time:
Wait time .00s
Interval 3.00s
Readings 300

Constants:
V1 -Ch1 .0000V
I2 -Ch2 100.0uA

****** GRAPHICS PLOT ******

B11, 100K, POLY, WINGS

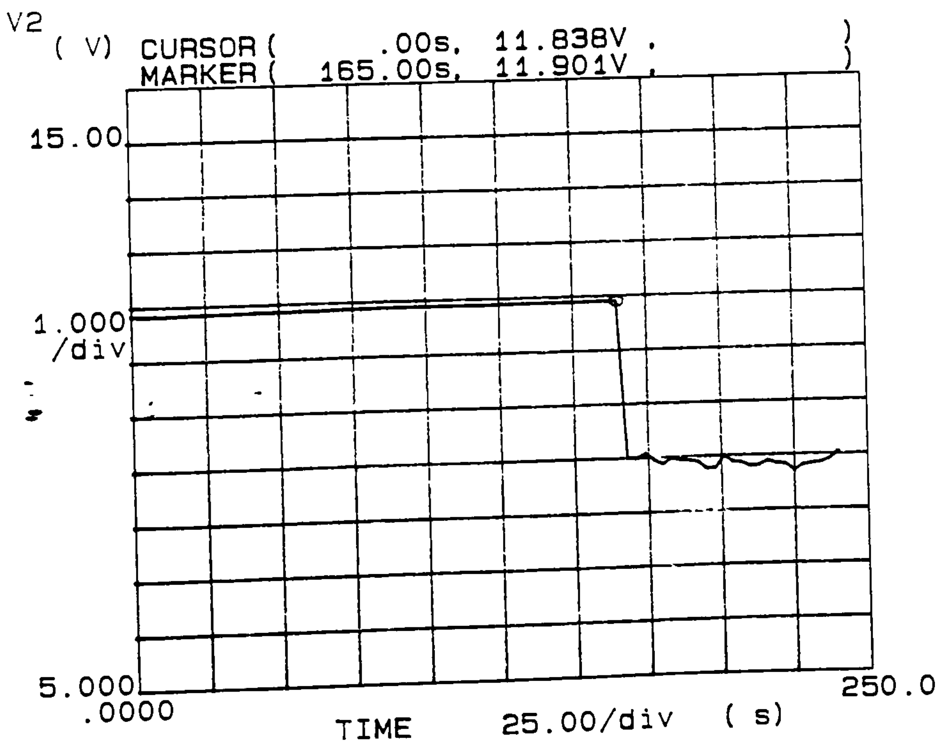


Time:
Wait time .00s
Interval 2.00s
Readings 300

Constants:
V1 -Ch1 .0000V
I2 -Ch2 500.0uA

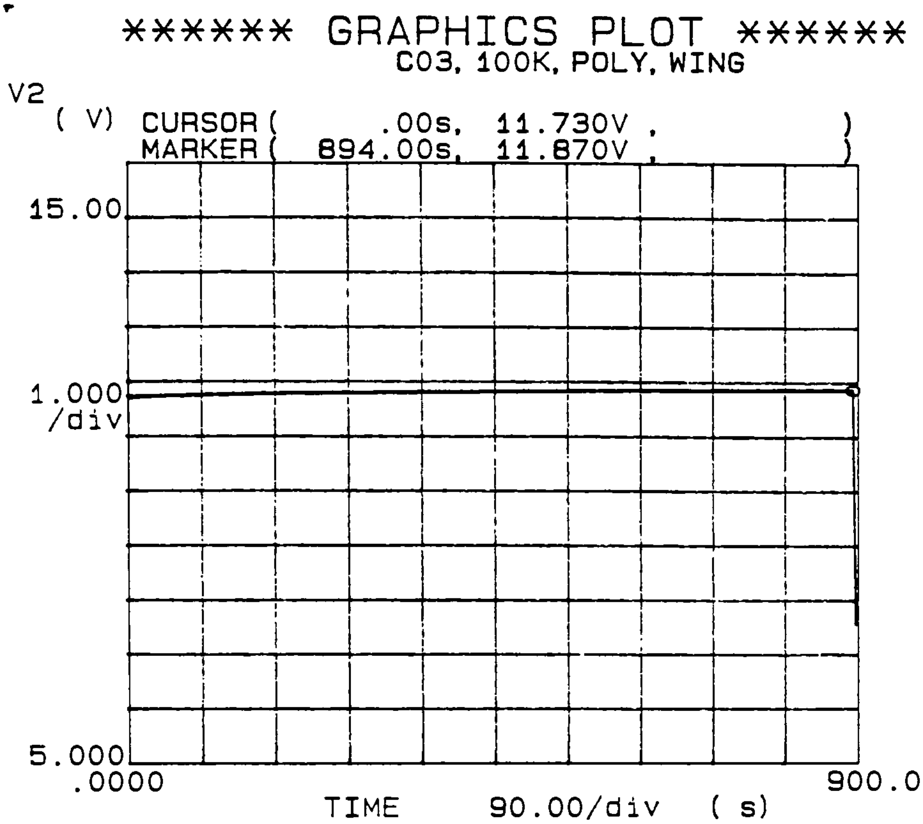
****** GRAPHICS PLOT ******

C03, 100K, POLY, WING



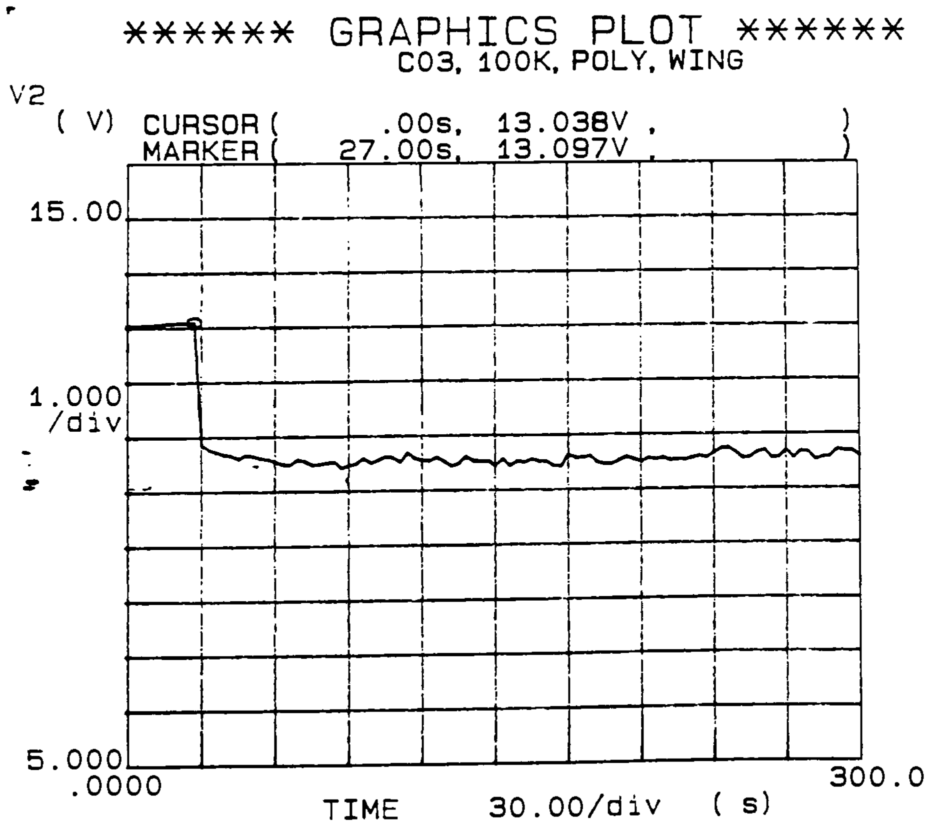
Time:
Wait time .00s
Interval 3.00s
Readings 300

Constants:
V1 -Ch1 .0000V
I2 -Ch2 10.00uA



Time:
Wait time .00s
Interval 3.00s
Readings 300

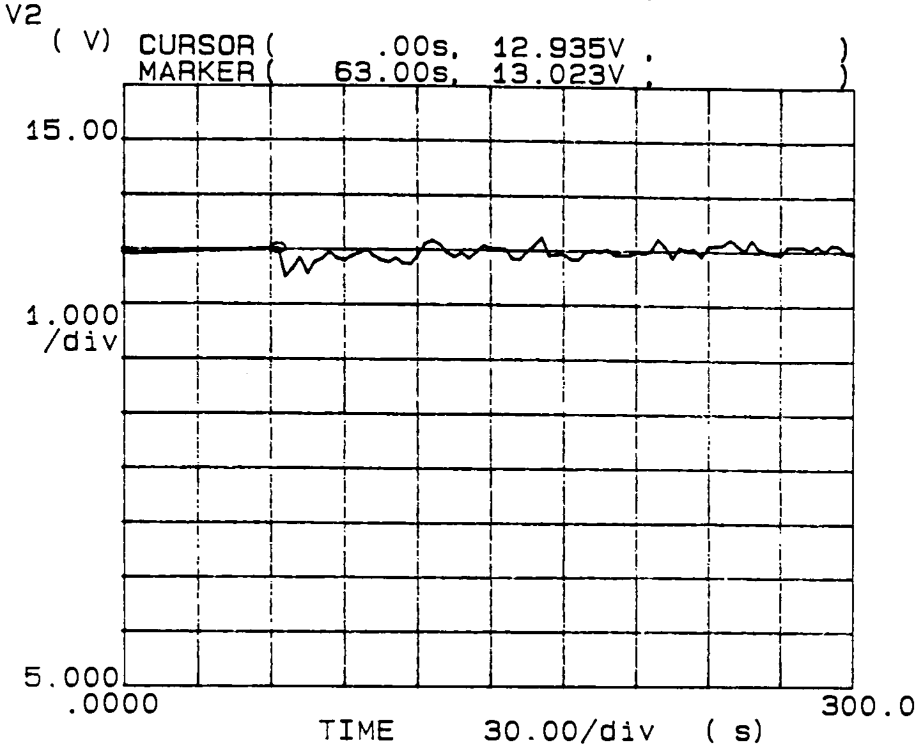
Constants:
V1 -Ch1 .0000V
I2 -Ch2 10.00uA



Time:
Wait time .00s
Interval 3.00s
Readings 300

Constants:
V1 -Ch1 .0000V
I2 -Ch2 100.0uA

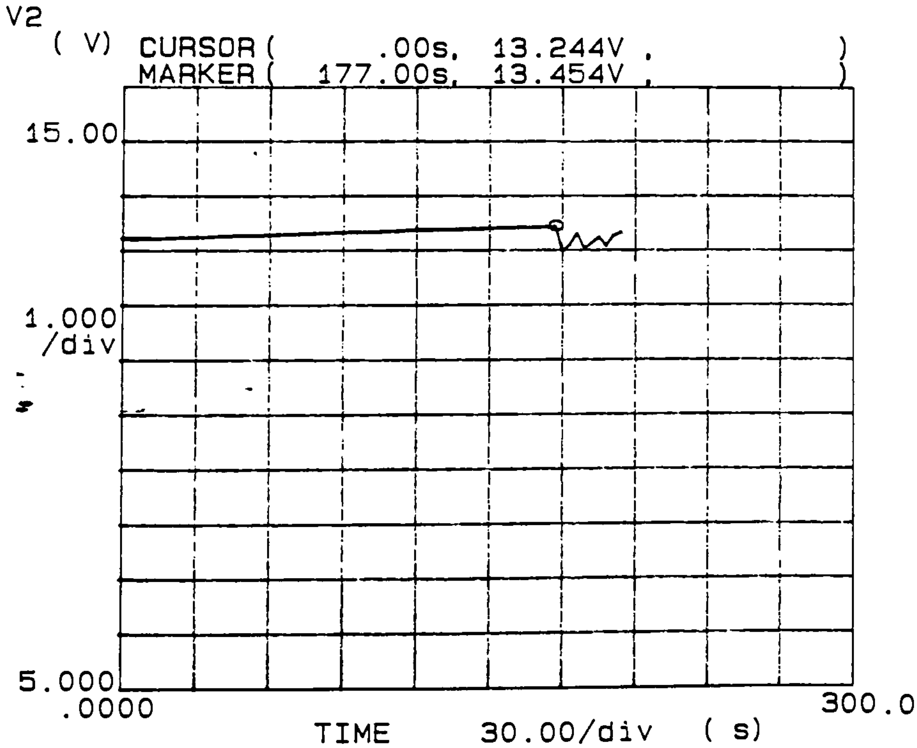
****** GRAPHICS PLOT ******
C03, 100K, POLY, WING



Time:
Wait time .00s
Interval 3.00s
Readings 300

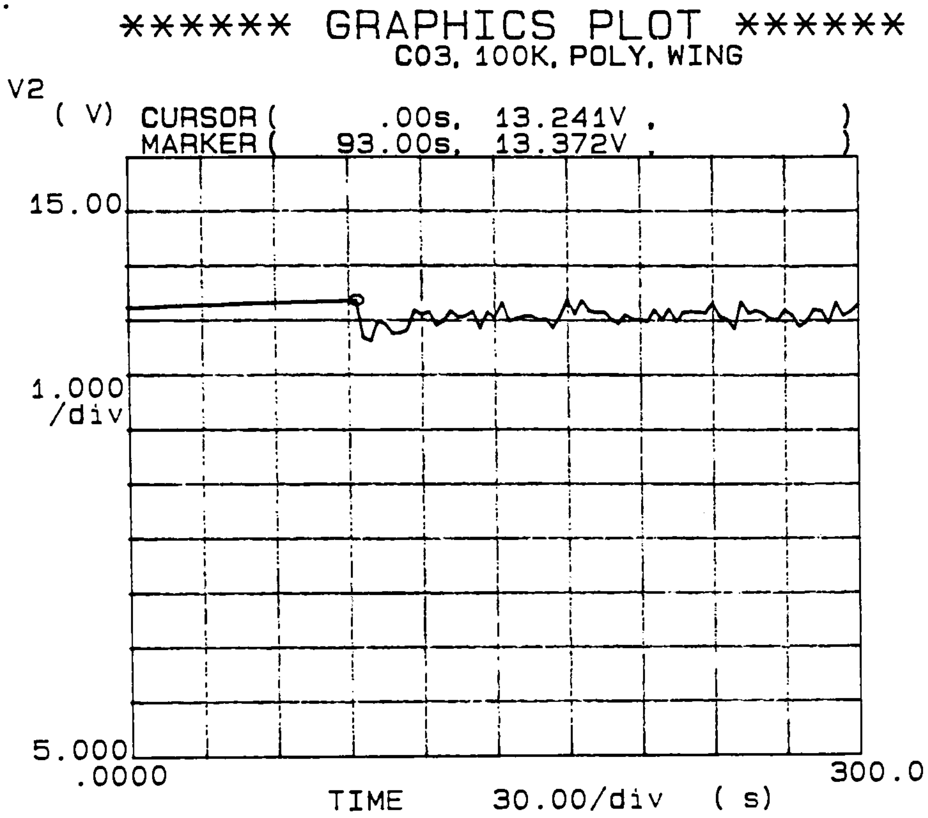
Constants:
V1 -Ch1 .0000V
I2 -Ch2 100.0uA

****** GRAPHICS PLOT ******
C03, 100K, POLY, WING



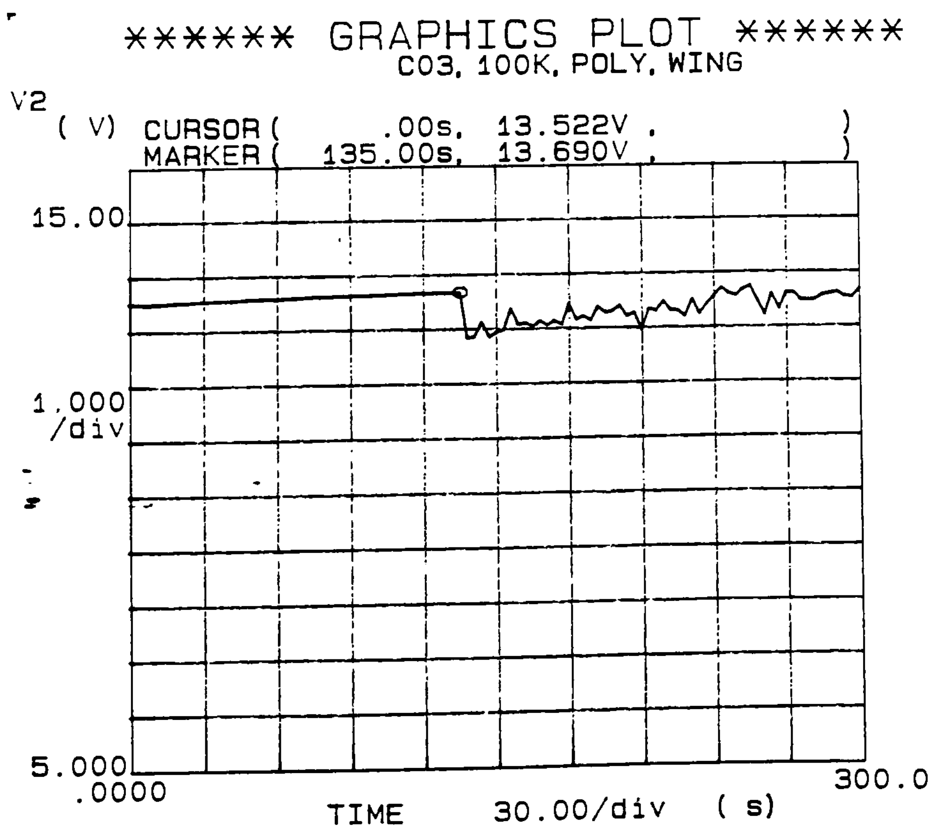
Time:
Wait time .00s
Interval 3.00s
Readings 300

Constants:
V1 -Ch1 .0000V
I2 -Ch2 100.0uA



Time:
Wait time .00s
Interval 3.00s
Readings 300

Constants:
V1 -Ch1 .0000V
I2 -Ch2 100.0uA



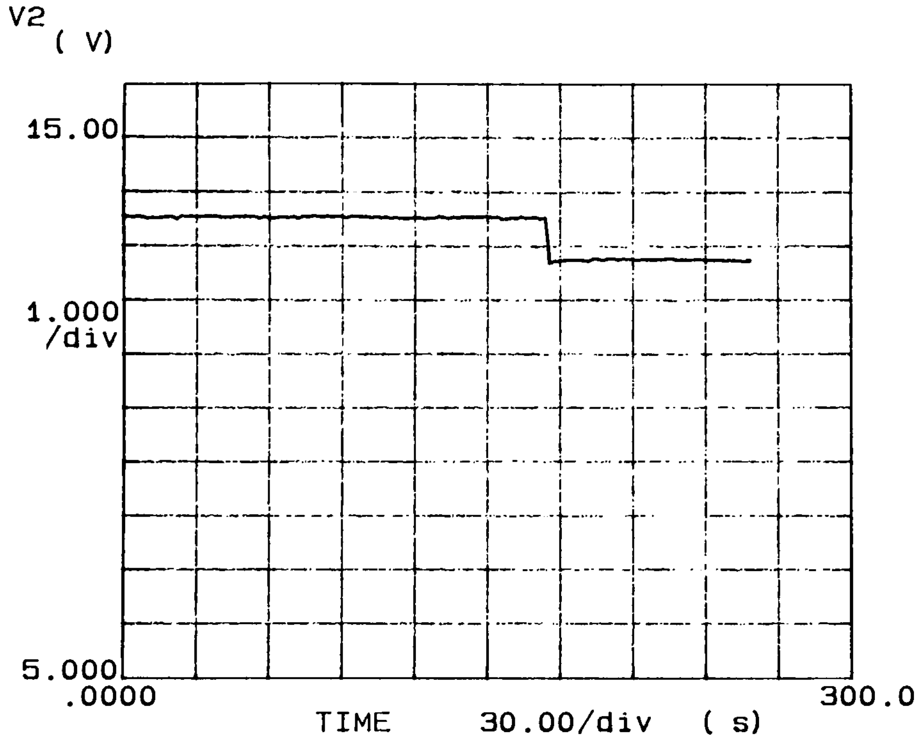
Time:
Wait time .00s
Interval 3.00s
Readings 300

Constants:
V1 -Ch1 .0000V
I2 -Ch2 100.0uA

5500 Å Etch Back Results

****** GRAPHICS PLOT ******

B16, 100K, POLY, WING



Time:	
Wait time	.00s
Interval	2.00s
Readings	250
Constants:	
V1 -Ch1	.0000V
I2 -Ch2	500.0uA